MROD-In Upgrade:

Register Change

Registers 0x00 - 0x0B unchanged.
Moved Registers 0x0C - 0x0F to 0x14 - 0x17
Moved Register 0x10 - 0x19 to 0x19 - 0x22
Inserted NoData Word Pattern and Mask Registers 0x0C - 0x0F
Inserted Error-Code Replace Pattern Register 0x10
Inserted three reserved Registers 0x11 - 0x13
Inserted TDC (Parity) Error Individual Interrupt Mask Register 0x18

Changed Input Link Interrupt IRQ1 Register (was 0x10, now 0x19)

LDERR_n is changed into a parity check on the link. The link is tested by inserting a parity bit in position 26. By default 'odd' parity is chosen, so when the parity is put into bit 26 then all 32 data bits should have odd parity. 'Even' parity can be chosen if Bit 9 of the Test & Input Link Control Status Register is set to '1'.

Register changes:
LDERR Interrupt bit moved from bit 19 to bit 0, now called 'Input Link Parity Error'
LDERR Overrun bit moved from bit 20 to bit 1, now called 'Input Link Parity Error Overrun'
LDOWN_n bit moved from bit 21 to bit 2
Bit 3 always read back as '0'
LDERR_n Mask bit moved from 22 to bit 4, now called 'Input Link Parity Error Mask'
LDOWN_n Mask bit moved from 23 to bit 5

Changed Test & Input Link Control Status Register (was 0x12, now 0x1B)

Input Link Reset bit moved from bit 9 to bit 10
Freeze bit moved from bit 10 to bit 11
LEDs [3..0] moved from bits [14..11] to bits [15..12]
Inserted Parity Check bit 9.

So now these bits are:

Bit 9: '0' (default) 'Odd' Parity Check on the Input Link, '1' for 'Even' Parity Check on the Input Link. Note that bit 26 of the Input Link data is defined as the parity bit.

Bit 10: Taking this bit from '0' to '1' resets the Input Link (edge sensitive).

Bit 11: When this bit is '1' the data pipeline in the FPGA is in 'Freeze' mode. Note that the default mode (after a Rst_n) is Freeze ON.

Bit [15..12]: Four LEDs can be connected to these bits. Writing a '1' puts on the light. These bits can be read back. Only LEDs[1..0] are fed to FPGA pins since

there are no more pins left on the FPGA package to accommodate LEDs[3..2].

Changed Serial Register (was 0x19, now 0x22)

This register is *now 32-bit wide*. Instead of passing only bits 18 and 19 of the separator word, now the whole separator word is passed into this register.

Changed insertion of TDC-ID bits in bits [28..24] when a TDC-Header is signalled.

When a TDC-Header is recognised then bits [28..24] will be replaced by the value of the time slot counter (5 bits). In this way, data of the 18 TDCs can be uniquely identified. Note that the TDC-Header bits [27..24] normally contain the 4-bit TDC-ID as programmed by JTAG into the TDCs.
After TDC-ID replacement the headers of the TDCs will look like:

TDC0	`0xA0yyyzzz`
TDC1	`0xA1yyyzzz`
TDC2	`0xA2yyyzzz`
TDC3	`0xA3yyyzzz`
TDC4	`0xA4yyyzzz`
TDC5	`0xA5yyyzzz`
TDC6	`0xA6yyyzzz`
TDC7	`0xA7yyyzzz`
TDC8	`0xA8yyyzzz`
TDC9	`0xA9yyyzzz`
TDC10	`0xAAyyyzzz`
TDC11	`0xAByyyzzz`
TDC12	`0xACyyyzzz`
TDC13	`0xADyyyzzz`
TDC14	`0xAEyyyzzz`
TDC15	`0xAFyyyzzz`
TDC16	`0xB0yyyzzz`
TDC17	`0xB1yyyzzz`

Notes: ‘`yyy`’ = Event-ID, ‘`zzz`’ = Bunch-ID

Changed insertion of Error-Codes.

When an error is signalled on the incoming data stream from the CSM then the word-ID bits [31..28] of the data word that contains the error is replaced by an Error-Code. The original word-ID bits are moved to bits [27..24] in order to make debugging easier because the original word type can probably still be traced (there is no guarantee however, since the error could have effected on of the word-ID bits).

When a TDC Parity Error was signalled by the CSM (bit 27 of the data word was set to '1' by the CSM) then bits [31..28] will be replaced with the TDC Parity Error-Code bits [31..28] of the Error-Code Replace Patterns Register.
When an Input Link parity check fails (bit 26 of the data word serves as a parity bit over all other 31-bits in the data word) then bits [31..28] will be replaced with the Input Link Parity Check Failure Error-Code bits [15..12] of the Error-Code Replace Patterns Register.
When both errors (TDC Parity Error and Input Link Parity Check Fail) occur at the same time then the Input Link Parity Check Fail is given priority.
Summarizing register 0x10 bits:
bit [31..28] TDC Parity Error, Error-Code Replace bits
bit [27..16] Not used, writing doesn't care, reading yields 0x000
bit [15..12] Input Link Parity Check Failure Error-Code Replace bits
bit [11..0] Not used, writing doesn't care, reading yields 0x000

Change URL [3..0] into TDI, TDO, TMS and TCK

Bit [4..7] of Register 0x1B (Control Status Registers and Test Registers) were used to drive the S-Link User Return Lines (URL [3..0]). The S-Link will be replaced by a Gigabit Optical Link (GOL) which has no return channel so the User Return Lines become meaningless.
The bits are transformed into JTAG signals that can drive the RJ45 connectors on the MROD-Out board.
The table below describes bits [4..7] of register 0x1B:

Register 0x1B Bit	Was	Changed To		
4	URL(0)	TCK	Output by MROD_In	Read/Write
5	URL(1)	TDI	Output by MROD_In	Read/Write
6	URL(2)	TMS	Output by MROD_In	Read/Write
7	URL(3)	TDO	Input to the MROD_In	Read value of TDO/ Write don't care

Changed Registers power up with a default values instead of 0x0:

Register	Function	Default After Reset
0x00	Separator Pattern	0xD0000000
0x01	Separator Control Bit Pattern	0x00000000
0x02	Separator Mask	0xF0000000
0x03	Separator Control Bit Mask	0x00000000

0x04	TDC-Header Pattern	0xA0000000
0x05	TDC-Header Control Bit Pattern	0x00000000
0x06	TDC-Header Mask	0xF0000000
0x07	TDC-Header Control Bit Mask	0x00000000
0x08	TDC-Trailer Pattern	0xC0000000
0x09	TDC-Trailer Control Bit Pattern	0x00000000
0x0A	TDC-Trailer Mask	0xF0000000
0x0B	TDC-Trailer Control Bit Mask	0x00000000
0x0C	No Data Pattern	0x00000000
0x0D	No Data Control Bit Pattern	0x00000000
0x0E	No Data Mask	0xF0000000
0x0F	No Data Control Bit Mask	0x00000000
0x10	Error-Code Replace Patterns	0x5000D000
0x11	Reserved	0x00000000
0x12	Reserved	0x00000000
0x13	Reserved	0x00000000
0x14	MROD Header Pattern	0x89000000
0x15	MROD Trailer Pattern	0x8A000000
0x16	Event Length FIFO	
0x17	Interrupt Control IRQ0	0x00000000
0x18	TDC (Parity) Error Individual Interrupt Mask	0x0003FFFF
0x19	Input Link Interrupt; IRQ1	0x00000000 [1)]
0x1A	Early and Late Event-ID; IRQ2	0x00000000
0x1B	Test & Input Link Control Status Register	0x00000800 [1)]
0x1C	Test Link Data Register	0x00000000
0x1D	Test Link Control Register	0x00000003
0x1E	Maximum Event Size	0x00000400
0x1F	Expected Event-ID	0x00000001
0x20	TDC Mask Register	0x0003FFFF
0x21	Partition Read-out Enable	0x0003FFFF
0x22	Serial Register	0x00000000

Notes: 1) Default value depends on LDOWN_n