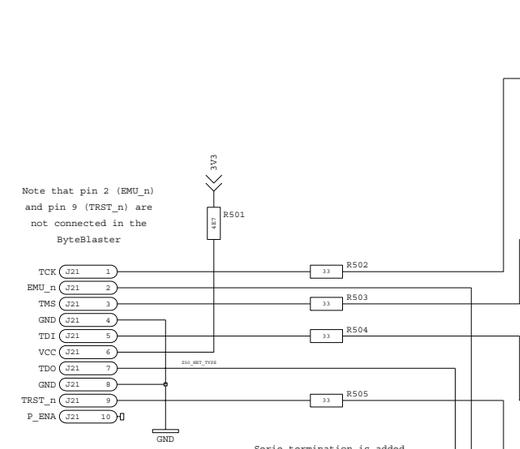
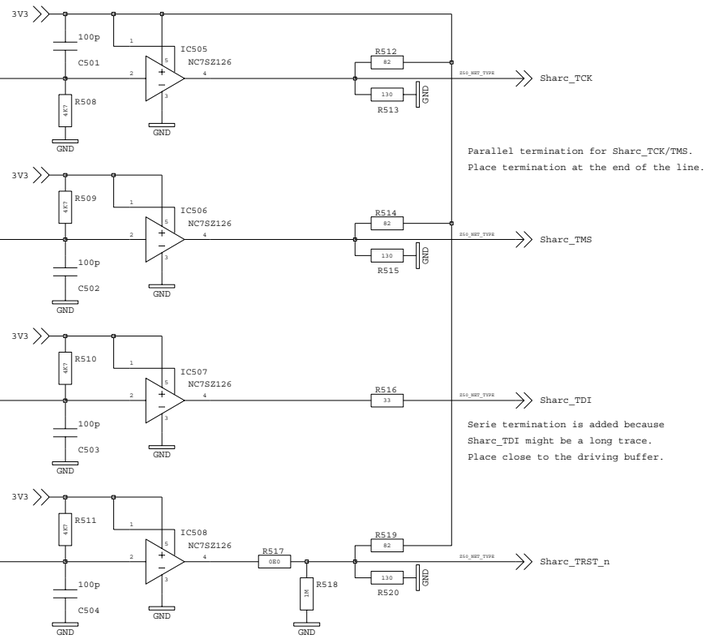
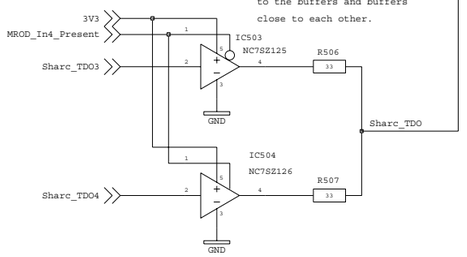
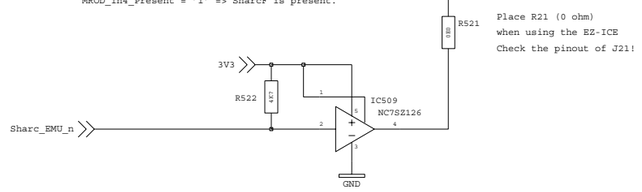
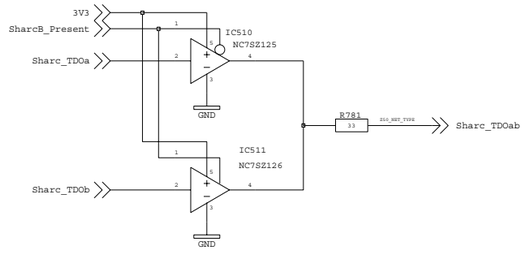
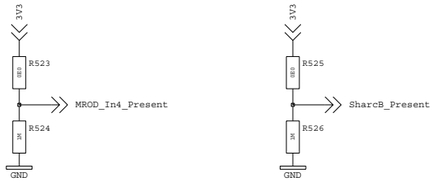




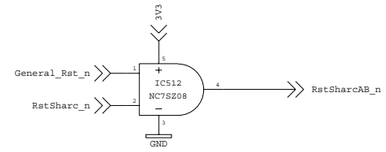


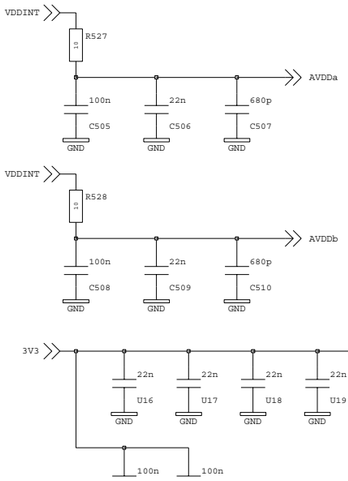


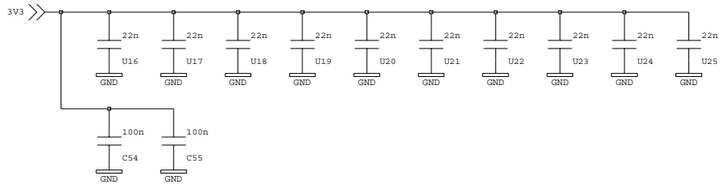




Both Sharcs are reset when there is
a General_Rst_n, or when a reset is
asked via the bit Set/Clr register
in VME64x CSR space.

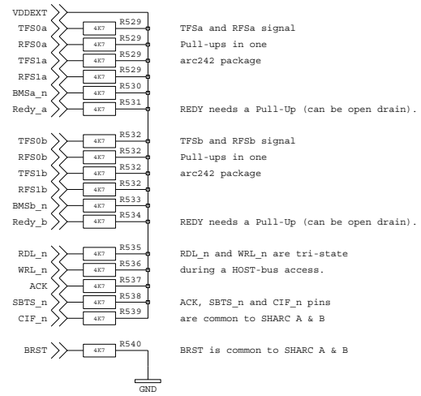






Fiducial501 Fiducial502

Fiducial503 Fiducial504



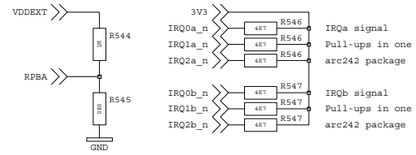
BR_n pins are common to SHARC A & B
Unused BR_n lines need Pull_Up (see datasheet)
Note that BR2_n and BR1_n pull-ups can be installed
when only SHARC A is mounted on the board.

PAGE and PA_n are common to SHARC A & B
No need for Pull-Ups.

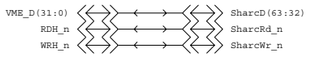
MS0_n .. MS3_n, RDH_n, RDL_n, WRH_n and WRL_n
are common to SHARC A & B and have internal Pull-Ups

HBR_n and HBG_n are common to SHARC A & B
No need for Pull-Ups.
HBR_n is always driven by the FPGA.
HBG_n is always driven by the Bus Master

DMAR1_n and DMAR2_n are common to SHARC A & B
No need for Pull-Ups.
The are always driven by the FPGA.
DMAG1_n and DMAG2_n are common to SHARC A & B
No need for Pull-Ups, they are driven by the Bus Master.



Rotating Priority Bus Arbitration
select is set to "Fixed Priority"
by default (SHARC A has priority).



MROD-Out	Rev V2 3
	Date 7 Feb 2006
SHARC JTAG and Auxiliary connections	Time 1:26:10 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF	Size A3 / 4 1 4 A
© ET-Nikhef Amsterdam	Dim 420 x 297 mm
NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Page 4 of 19