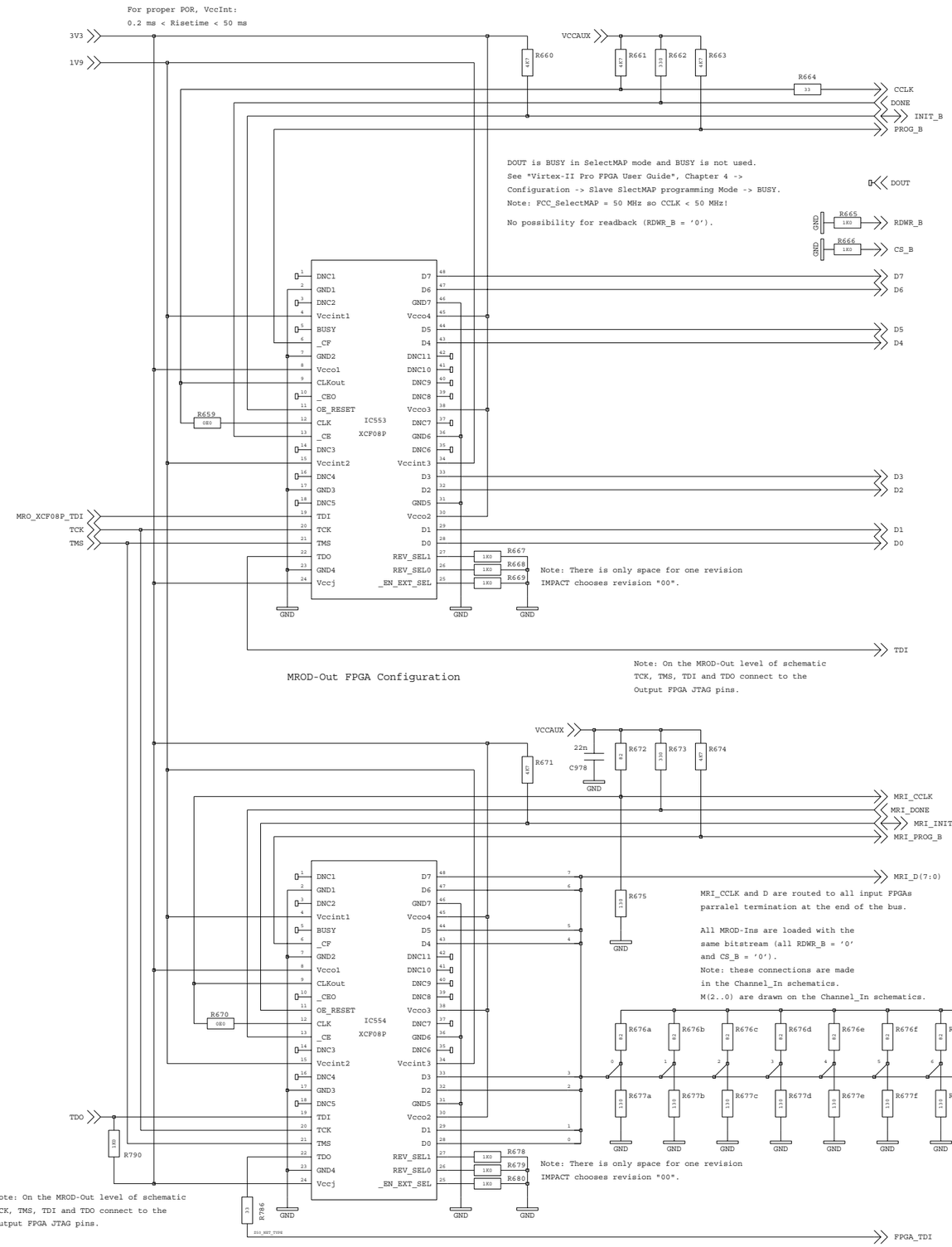
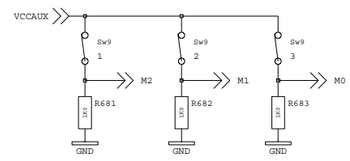
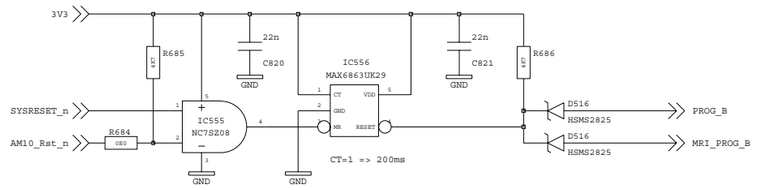




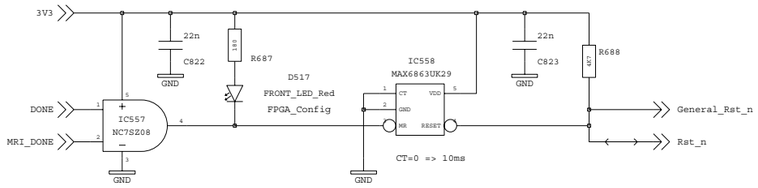
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

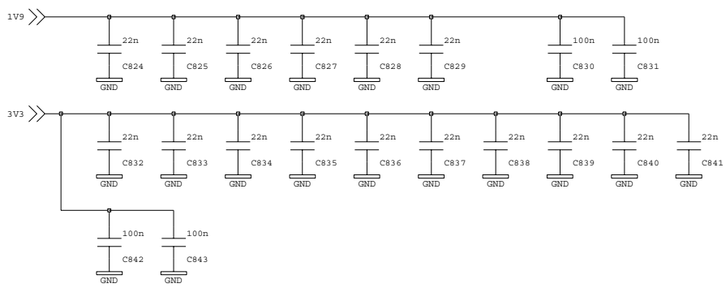
Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap
configuration. See Xilinx PROM Errata,
Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA
to Master SelectMap and all other MROD-In FPGAs
to Slave SelectMap.
Note: MROD-In M(2..0) are drawn on the Channel_In schematics.



A reset also issues a re-configuration of all FPGAs



After re-configuration 'General_Rst_n' is kept active for 10 ms.



MROD-Out		Rev V2 9
		Date 7 Feb 2006
FPGA Configuration And Resets		Time 1:33:23 pm
Proj: MROD-X	Proj.No: 38405	Name Ton van Reen
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 12 of 19