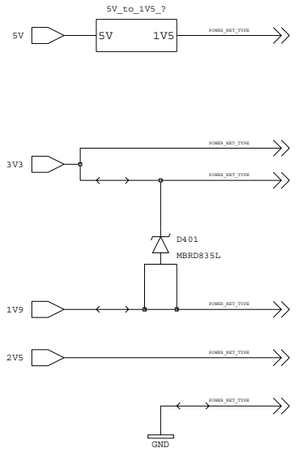


= VCCINT for Xilinx Virtex-II Pro in the
Input Channels, 600 mA per Channel
VCCINT Ramp rate 200 us min. and 50 ms max.

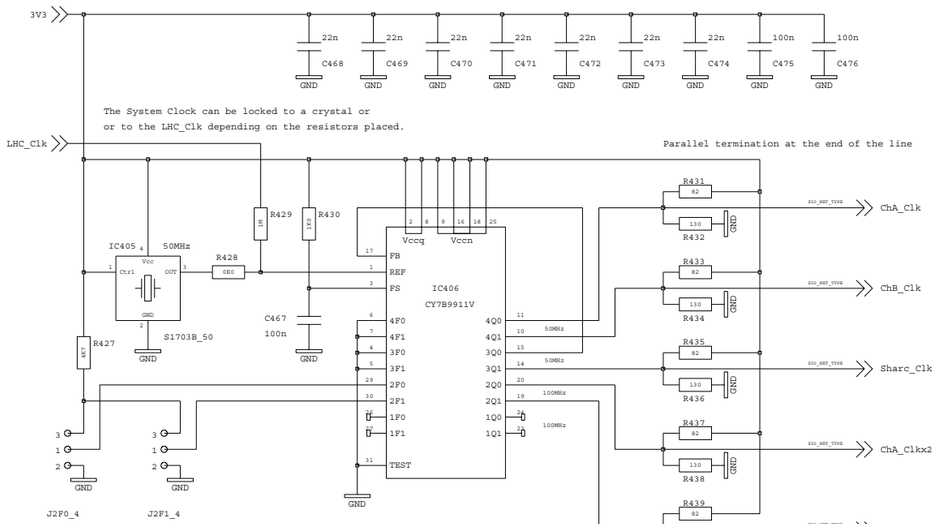
= VDDEXT for the ADSP21160N
100 mA per ADSP21160N

Note ADSP21160N Power-On Sequence!
Time between power-on VDDINT -> VDDEXT
= -50 ms to +200 ms

= VDDINT for the ADSP21160N
960 mA peak per ADSP21160N

= VCCAUX for the Xilinx Virtex-II Pro in the
Input Channel, 250 mA per Channel

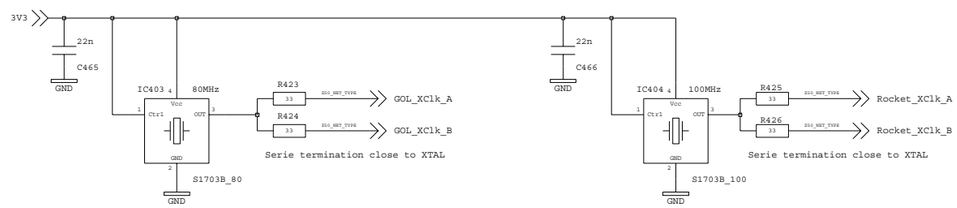
All GND nets on the SHARC need
to be connected to golbal GROUND.



100 MHz Phase Adjust

Fnom = 100 MHz
4F(1:0)= "00" => 100 Divide by 2 = 50 MHz
3F(1:0)= "00" => 100 Divide by 2 = 50 MHz
2F(1:0)= "mm" => 0 tu
1F(1:0)= "mm" => 0 tu

SHARC and Input Channel System Clock



GOL Frequency
80 MHz 16 bit = 40 MHz 32 bit
= 160 MB/s

Rocket-IO Inter-FPGA Link Frequency
100 MHz 16 bit = 50 MHz 32 bit
= 200 MB/s

MROD-In	Rev V2 20
	Date 7 Feb 2006
Power and Clocks	Time 1:47:20 pm
Proj: MROD-X / Proj.No: 38405	Name tonvr
Peter Jansweijer / peterj@nikhef.nl	
NIKHEF — NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA, KRUISLAAN 409, 020-592 2000, 1098 SJ AMSTERDAM NEDERLAND	Size A3 / 4 1 4 A
	Dim 420 x 297 mm
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