

IC301
ADSP21160N

A1	DATA(14)	A2	DATA(13)	A3	DATA(10)	A4	DATA(8)	A5	DATA(4)	A6	DATA(2)	A7	TDI	A8	TRST_n	A9	RESET_n	A10	PPBA	A11	IRQ0_n	A12	FLAG1	A13	TMEXP	A14	NC_A14	A15	NC_A15	A16	TPP1	A17	RFS1	A18	RCLK1	A19	DT0	A20	LOGAT(4)
B1	DATA(22)	B2	DATA(16)	B3	DATA(15)	B4	DATA(9)	B5	DATA(6)	B6	DATA(3)	B7	DATA(0)	B8	TCK	B9	Sharc_BMU_n	B10	IRQ0_n	B11	ChB_Empty	B12	FLAG0	B13	NC_B13	B14	NC_B14	B15	DT1	B16	RCLK1	B17	RFS0	B18	TCLK0	B19	LOGAT(5)	B20	LOGAT(2)
C1	DATA(24)	C2	DATA(18)	C3	DATA(17)	C4	DATA(11)	C5	DATA(7)	C6	DATA(5)	C7	DATA(1)	C8	TMS	C9	TDO	C10	IRQ1_n	C11	ChA_Empty	C12	NC_C12	C13	NC_C13	C14	TCLK1	C15	DT1	C16	DT0	C17	LOGAT(7)	C18	LOGAT(6)	C19	LOGAT(3)	C20	LOGAT(0)
D1	DATA(28)	D2	DATA(25)	D3	DATA(20)	D4	DATA(19)	D5	DATA(12)	D6	VDDINT_06	D7	VDDINT_07	D8	VDDINT_08	D9	VDDINT_09	D10	VDDINT_10	D11	VDDINT_11	D12	VDDINT_12	D13	VDDINT_13	D14	VDDINT_14	D15	TPP0	D16	L1DAT(7)	D17	LOCLK	D18	LOGAT(3)	D19	LOGAT(1)	D20	L1CLK
E1	DATA(30)	E2	DATA(29)	E3	DATA(23)	E4	DATA(21)	E5	VDDINT_05	E6	VDDINT_04	E7	VDDINT_03	E8	VDDINT_02	E9	VDDINT_01	E10	VDDINT_00	E11	GND	E12	VDDINT_15	E13	VDDINT_16	E14	VDDINT_17	E15	VDDINT_18	E16	VDDINT_19	E17	L1DAT(6)	E18	L1DAT(5)	E19	L1ACK	E20	L1DAT(1)
F1	DATA(34)	F2	DATA(33)	F3	DATA(27)	F4	DATA(26)	F5	VDDINT_05	F6	VDDINT_04	F7	GND_07	F8	GND_08	F9	GND_09	F10	GND_10	F11	GND_11	F12	GND_12	F13	GND_13	F14	GND_14	F15	VDDINT_15	F16	VDDINT_16	F17	L1DAT(4)	F18	L1DAT(3)	F19	L1DAT(0)	F20	L2DAT(7)
G1	DATA(38)	G2	DATA(35)	G3	DATA(32)	G4	DATA(31)	G5	VDDINT_05	G6	VDDINT_04	G7	GND_07	G8	GND_08	G9	GND_09	G10	GND_10	G11	GND_11	G12	GND_12	G13	GND_13	G14	GND_14	G15	VDDINT_15	G16	VDDINT_16	G17	L1DAT(2)	G18	L2DAT(6)	G19	L2DAT(4)	G20	L2CLK
H1	DATA(40)	H2	DATA(39)	H3	DATA(37)	H4	DATA(34)	H5	VDDINT_05	H6	VDDINT_04	H7	GND_07	H8	GND_08	H9	GND_09	H10	GND_10	H11	GND_11	H12	GND_12	H13	GND_13	H14	GND_14	H15	VDDINT_15	H16	VDDINT_16	H17	L1DAT(2)	H18	L2DAT(6)	H19	L2DAT(4)	H20	L2CLK
I1	DATA(44)	I2	DATA(43)	I3	DATA(42)	I4	DATA(41)	I5	VDDINT_05	I6	VDDINT_04	I7	GND_07	I8	GND_08	I9	GND_09	I10	GND_10	I11	GND_11	I12	GND_12	I13	GND_13	I14	GND_14	I15	VDDINT_15	I16	VDDINT_16	I17	L1DAT(2)	I18	L2DAT(2)	I19	HBG_n	I20	VDDINT
J1	DATA(48)	J2	DATA(47)	J3	DATA(45)	J4	DATA(44)	J5	VDDINT_05	J6	VDDINT_04	J7	GND_07	J8	GND_08	J9	GND_09	J10	GND_10	J11	GND_11	J12	GND_12	J13	GND_13	J14	GND_14	J15	VDDINT_15	J16	VDDINT_16	J17	L1DAT(2)	J18	L2DAT(2)	J19	HBG_n	J20	VDDINT
K1	CLK_CFG_0	K2	DATA(44)	K3	DATA(45)	K4	DATA(47)	K5	VDDINT_05	K6	VDDINT_04	K7	GND_07	K8	GND_08	K9	GND_09	K10	GND_10	K11	GND_11	K12	GND_12	K13	GND_13	K14	GND_14	K15	VDDINT_15	K16	VDDINT_16	K17	BReq_n	K18	BReq_n	K19	BReq_n	K20	BReq_n
L1	CLKIN	L2	CLK_CFG_1	L3	AGND	L4	CLK_CFG_2	L5	VDDINT_15	L6	VDDINT_14	L7	GND_17	L8	GND_18	L9	GND_19	L10	GND_20	L11	GND_21	L12	GND_22	L13	GND_23	L14	GND_24	L15	VDDINT_15	L16	VDDINT_16	L17	BReq_n	L18	BReq_n	L19	BReq_n	L20	BReq_n
M1	AVDD	M2	CLK_CFG_3	M3	CLKOUT	M4	NC_B4	M5	VDDINT_05	M6	VDDINT_04	M7	GND_07	M8	GND_08	M9	GND_09	M10	GND_10	M11	GND_11	M12	GND_12	M13	GND_13	M14	GND_14	M15	VDDINT_15	M16	VDDINT_16	M17	BReq_n	M18	BReq_n	M19	BReq_n	M20	BReq_n
N1	AVDD	GND	DATA(48)	N4	DATA(51)	N5	VDDINT_05	N6	VDDINT_04	N7	GND_07	N8	GND_08	N9	GND_09	N10	GND_10	N11	GND_11	N12	GND_12	N13	GND_13	N14	GND_14	N15	VDDINT_15	N16	VDDINT_16	N17	L1DAT(5)	N18	L1DAT(6)	N19	L1DAT(4)	N20	L1CLK		
O1	DATA(49)	O2	DATA(50)	O3	DATA(52)	O4	DATA(55)	O5	VDDINT_05	O6	VDDINT_04	O7	GND_07	O8	GND_08	O9	GND_09	O10	GND_10	O11	GND_11	O12	GND_12	O13	GND_13	O14	GND_14	O15	VDDINT_15	O16	VDDINT_16	O17	L1DAT(5)	O18	L1DAT(6)	O19	L1DAT(4)	O20	L1CLK
P1	DATA(17)	P2	DATA(18)	P3	DATA(20)	P4	DATA(23)	P5	VDDINT_05	P6	VDDINT_04	P7	GND_07	P8	GND_08	P9	GND_09	P10	GND_10	P11	GND_11	P12	GND_12	P13	GND_13	P14	GND_14	P15	VDDINT_15	P16	VDDINT_16	P17	L1DAT(2)	P18	L1DAT(1)	P19	L1DAT(3)	P20	L1ACK
Q1	DATA(53)	Q2	DATA(54)	Q3	DATA(57)	Q4	DATA(60)	Q5	VDDINT_05	Q6	VDDINT_04	Q7	GND_07	Q8	GND_08	Q9	GND_09	Q10	GND_10	Q11	GND_11	Q12	GND_12	Q13	GND_13	Q14	GND_14	Q15	GND_15	Q16	VDDINT_16	Q17	VDDINT_17	Q18	L1DAT(5)	Q19	L1DAT(6)	Q20	L1DAT(0)
R1	DATA(21)	R2	DATA(22)	R3	DATA(25)	R4	DATA(28)	R5	VDDINT_05	R6	VDDINT_04	R7	GND_07	R8	GND_08	R9	GND_09	R10	GND_10	R11	GND_11	R12	GND_12	R13	GND_13	R14	GND_14	R15	GND_15	R16	VDDINT_16	R17	VDDINT_17	R18	L1DAT(5)	R19	L1DAT(6)	R20	L1DAT(0)
S1	DATA(56)	S2	DATA(58)	S3	DATA(59)	S4	DATA(63)	S5	VDDINT_05	S6	VDDINT_04	S7	VDDINT_07	S8	VDDINT_08	S9	VDDINT_09	S10	VDDINT_10	S11	VDDINT_11	S12	VDDINT_12	S13	VDDINT_13	S14	VDDINT_14	S15	VDDINT_15	S16	VDDINT_16	S17	L1DAT(3)	S18	L1ACK	S19	L1CLK	S20	L1DAT(4)
T1	DATA(61)	T2	DATA(62)	T3	ADDR(3)	T4	ADDR(2)	T5	VDDINT_05	T6	VDDINT_04	T7	VDDINT_07	T8	VDDINT_08	T9	VDDINT_09	T10	VDDINT_10	T11	VDDINT_11	T12	VDDINT_12	T13	VDDINT_13	T14	VDDINT_14	T15	VDDINT_15	T16	VDDINT_16	T17	L1DAT(3)	T18	L1ACK	T19	L1CLK	T20	L1DAT(4)
U1	ADDR(4)	U2	ADDR(6)	U3	ADDR(17)	U4	ADDR(10)	U5	ADDR(14)	U6	ADDR(18)	U7	ADDR(22)	U8	ADDR(25)	U9	ADDR(28)	U10	ADDR(31)	U11	ADDR(35)	U12	ADDR(39)	U13	ADDR(43)	U14	ADDR(47)	U15	ADDR(51)	U16	ADDR(55)	U17	ADDR(59)	U18	ADDR(63)	U19	ADDR(67)	U20	ADDR(71)
V1	ADDR(5)	V2	ADDR(8)	V3	ADDR(12)	V4	ADDR(15)	V5	ADDR(19)	V6	ADDR(23)	V7	ADDR(27)	V8	ADDR(31)	V9	ADDR(35)	V10	ADDR(39)	V11	ADDR(43)	V12	ADDR(47)	V13	ADDR(51)	V14	ADDR(55)	V15	ADDR(59)	V16	ADDR(63)	V17	ADDR(67)	V18	ADDR(71)	V19	ADDR(75)	V20	ADDR(79)
W1	ADDR(6)	W2	ADDR(11)	W3	ADDR(13)	W4	ADDR(16)	W5	ADDR(20)	W6	ADDR(24)	W7	ADDR(28)	W8	ADDR(32)	W9	ADDR(36)	W10	ADDR(40)	W11	ADDR(44)	W12	ADDR(48)	W13	ADDR(52)	W14	ADDR(56)	W15	ADDR(60)	W16	ADDR(64)	W17	ADDR(68)	W18	ADDR(72)	W19	ADDR(76)	W20	ADDR(80)
X1	ADDR(7)	X2	ADDR(12)	X3	ADDR(14)	X4	ADDR(17)	X5	ADDR(21)	X6	ADDR(25)	X7	ADDR(29)	X8	ADDR(33)	X9	ADDR(37)	X10	ADDR(41)	X11	ADDR(45)	X12	ADDR(49)	X13	ADDR(53)	X14	ADDR(57)	X15	ADDR(61)	X16	ADDR(65)	X17	ADDR(69)	X18	ADDR(73)	X19	ADDR(77)	X20	ADDR(81)
Y1	ADDR(8)	Y2	ADDR(11)	Y3	ADDR(13)	Y4	ADDR(16)	Y5	ADDR(20)	Y6	ADDR(24)	Y7	ADDR(28)	Y8	ADDR(32)	Y9	ADDR(36)	Y10	ADDR(40)	Y11	ADDR(44)	Y12	ADDR(48)	Y13	ADDR(52)	Y14	ADDR(56)	Y15	ADDR(60)	Y16	ADDR(64)	Y17	ADDR(68)	Y18	ADDR(72)	Y19	ADDR(76)	Y20	ADDR(80)

Clock Configuration:
CLK_CFG(3:0) = "0010"
=> Core / CLKIN Ration 2:1

ID = "000"

Booting Mode:
EBOOT = '0', LBOOT = '1', BMS_n = '1' (Input)
=> Link Port Booting

SHARC Power pins:
VDDINT (1V9) 40 pins
VDDEXT (3V3) 43 pins
GND 82 pins
NC 9 pins

MROD- In		Rev	V2	2
		Date	7 Feb 2006	
SHARC		Time	1:46:33 pm	
Proj: MROD-X	Proj.No: 38405	Name	tonvr	
Peter Jansweijer	peterj@nikhef.nl	Size	A3	4 1 4 A
NIKHEF <small>©-Nikhef Amsterdam</small>		Dim	420 x 297 mm	
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<small>NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND</small>				