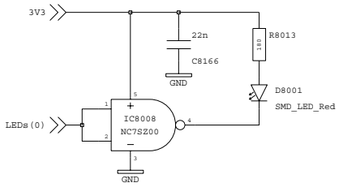
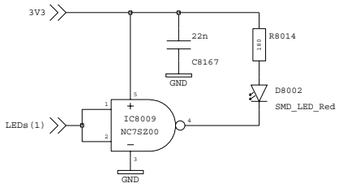
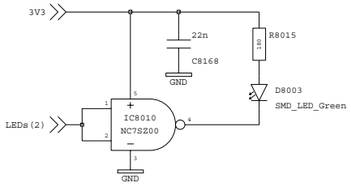
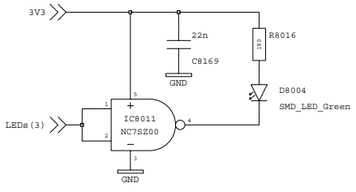
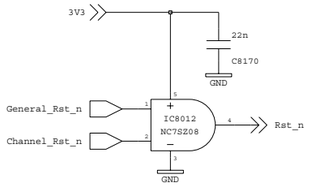


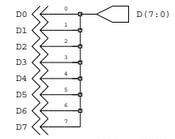


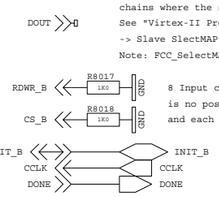






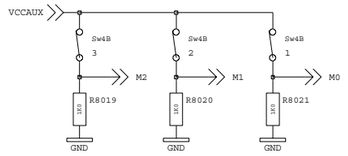
Fiducial8001 Fiducial8002





DOUT is BUSY in SelectMAP mode and BUSY should NOT be used for parallel chains where the same bitstream is loaded into multiple devices.
See "Virtex-II Pro FPGA User Guide", Chapter 4 -> Configuration -> Slave SlectMAP programming Mode -> BUSY.
Note: FCC_SelectMAP = 50 MHz so CCLK < 50 MHz!

8 Input channels are loaded in parallel so there is no possibility for readback (RDWR_B = '0') and each CS_B = '0'



M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

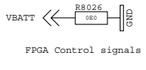
Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

FPGA Configuration Signals

PWRDWN_B is unsupported (should be pulled high)

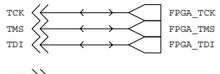
HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

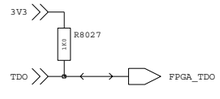
Temperature sensing diode



VBATT is decriptor key memory backup supply

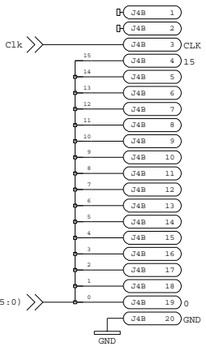
FPGA Control signals



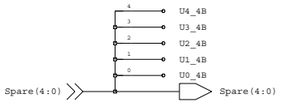


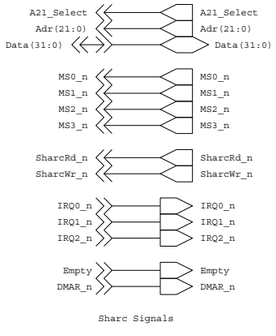
FPGA JTAG Signals

Optinal Test Connector



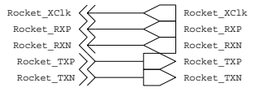
Testpoints force Spare lines to be accessible.





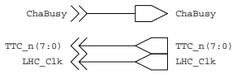
Sharc Signals

Input Channel ID bits



Frontend to Backend

Rocket IO Signals



TTC Signals

Clock Signals

channel_in		Rev V2 2
		Date 7 Feb 2006
		Time 1:53:04 pm
Input FPGA Auxiliary Connections		Name Ton van Reen
Proj: MROD-X	Proj.No: 38405	
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 4 1 4 A
© ET-Nikhef Amsterdam		Dim 420 x 297 mm
		Page 6 of 6