



MRD0-Out	
Rev	23
Date	26 Jan 2005
Time	12:00:26 pm
Proj:	MRD0-X
Proj.No:	38405
Name	petertj
Size	A3
Dim	41 x 4 A
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Output FPGA MGT Pwr Decoupling, Termination
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Series Termination for VME-bus Signals

Series Termination for SDRAM Interface

Series Termination for S-Link Signals

Series Termination for Share Addressbus

Note: V1V8_MGT is common to all MRD0-Ins
 MGT RX Termination (estimated 8 * 11 mA = 88 mA)