

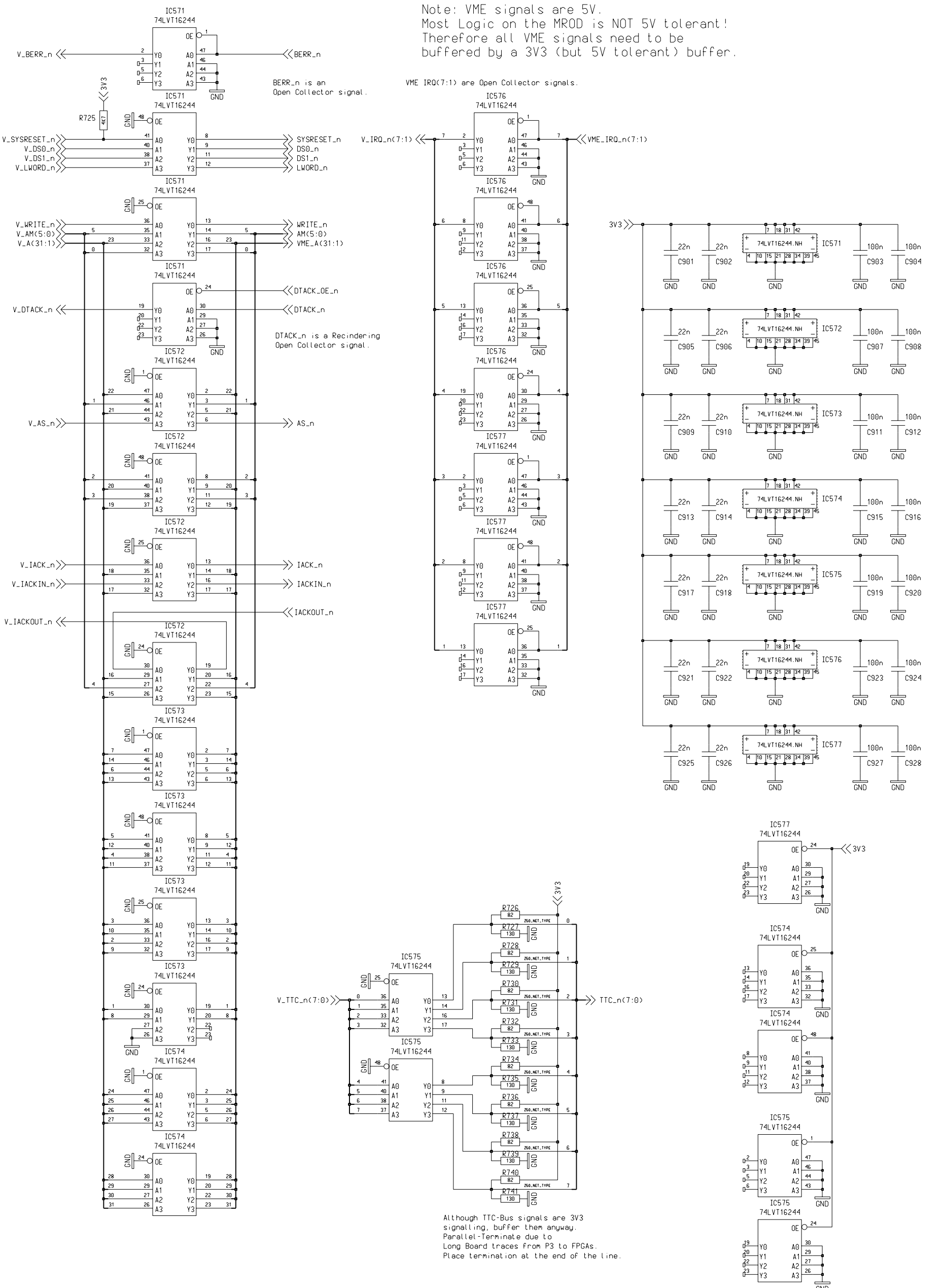
Note: VME signals are 5V.
 Most Logic on the MROD is NOT 5V tolerant!
 Therefore all VME signals need to be buffered by a 3V3 (but 5V tolerant) buffer.

VME IRQ(7:1) are Open Collector signals.

BERR_n is an Open Collector signal.

DTACK_n is a Recirculating Open Collector signal.

Although TTC-Bus signals are 3V3 signalling, buffer them anyway. Parallel-Terminate due to Long Board traces from P3 to FPGAs. Place termination at the end of the line.



MROD-Out		Rev 12
		Date 26 Jan 2005
VME Bus Other Buffers		Time 12:06:41 pm
Proj: MROD-X	Proj.No:	Name Peter Jansweijer
Peter Jansweijer	peter.j@nikhef.nl	
		Size A3 4 1 4 A
NATIONAL INSTITUTE FOR NUCLEAR PHYSICS AND HIGH ENERGY PHYSICS KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND		Dim 297 x 420 mm
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