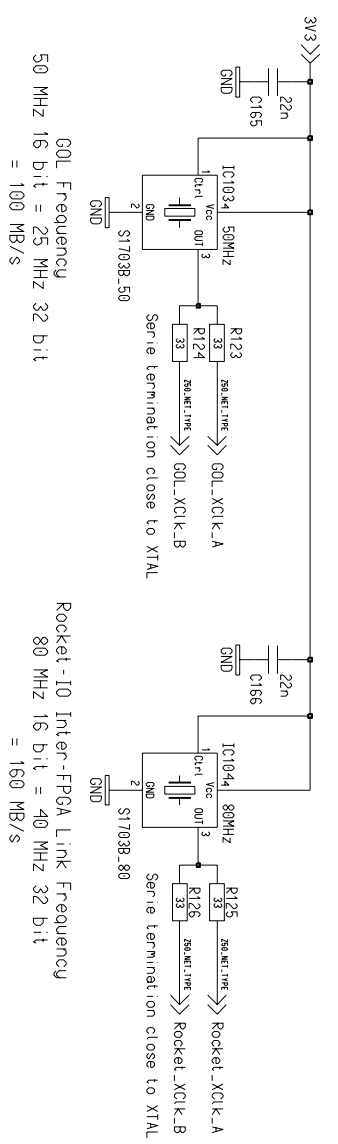
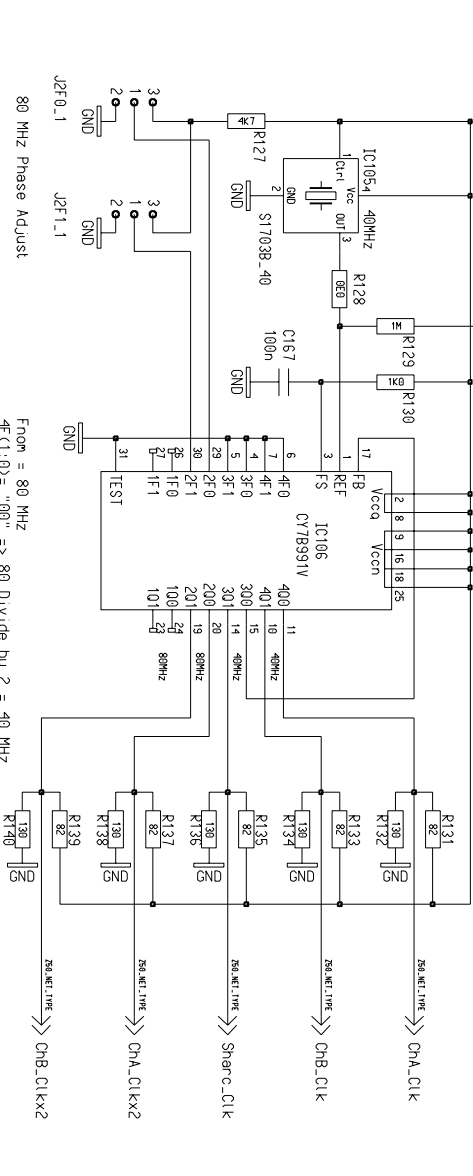


SV\_L0\_11V5\_2  
 1V5 = VCCINT for Xilinx Virtex-II Pro in the Input Channels, 500 mA per Channel  
 VCCINT Ramp rate 200 us min. and 50 ns max.

3V3  
 VDDEXT = VDDEXT for the ADSP21160N  
 100 mA per ADSP21160N  
 Note ADSP21160N Power-On Sequence!  
 Time between power-on VDDINT -> VDDEXT = -50 ns to +200 ns  
 VDDINT = VDDINT for the ADSP21160N  
 950 mA peak per ADSP21160N  
 2V5  
 = VCCAUX for the Xilinx Virtex-II Pro in the Input Channel, 250 mA per Channel  
 All GND nets on the SHARC need to be connected to global GROUND.



3V3  
 The System Clock can be locked to a crystal or to the LHC\_CLK depending on the resistors placed.  
 Parallel termination at the end of the line



MR0D-In		Rev	57
Power and Clocks		Date	26 Jan 2005
Proj: MR0D-X		Time	12:09:03 pm
Peter Jansweijer		Name	peter.j
Proj: MR0D-X		Proj.No:	38405
Peter Jansweijer		Size	A3
NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOOG-ENERGIE-FYSICA KRUISLAAN 409, 020-532 2000 1098 SJ AMSTERDAM NEDERLAND		Dim	420 x 297 mm
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