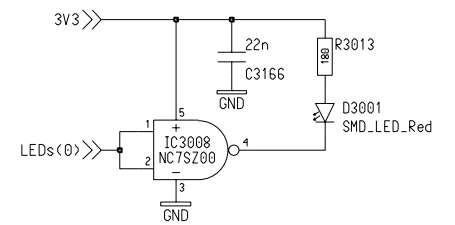
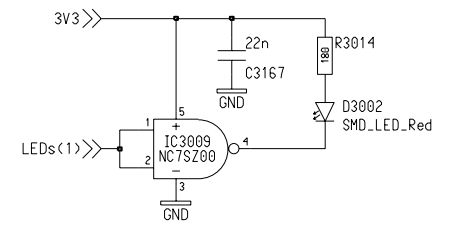
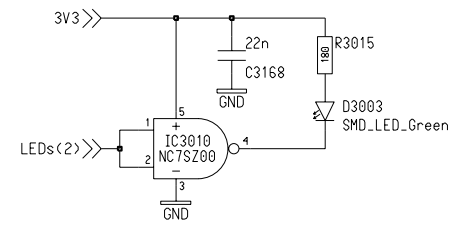
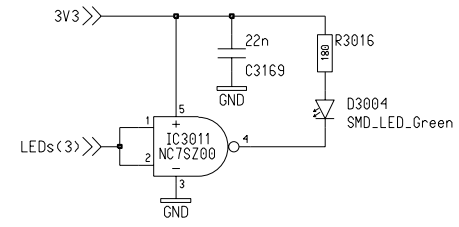
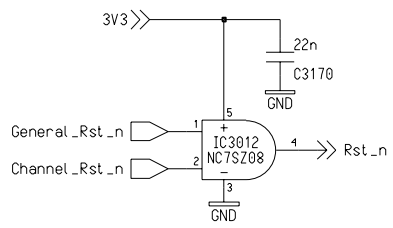


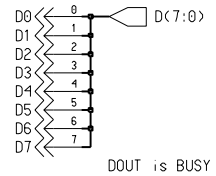


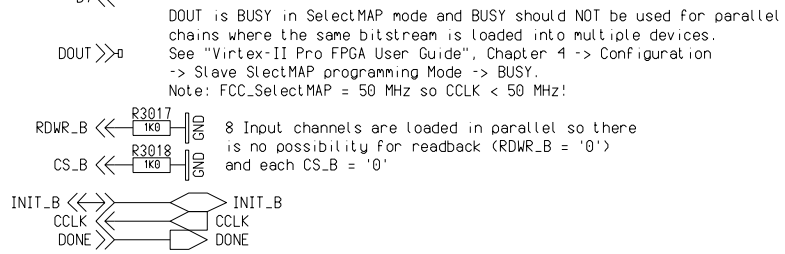


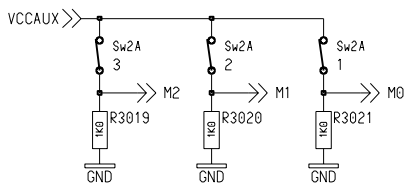




Fiducial3001 Fiducial3002



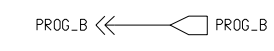




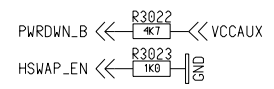
M2 M1 M0
0 1 1 Master SelectMAP
1 1 0 Slave SelectMAP (default)
1 0 1 Boundary scan

'On' = '1', 'Off' = '0'

Default configuration mode will be Slave SelectMAP.
It may be necessary to use Master SelectMap configuration. See Xilinx PROM Errata, Answer Record #18562
In this case set MROD-Out FPGA and one MROD-In FPGA to Master SelectMap and all other MROD-In FPGAs to Slave SelectMap.

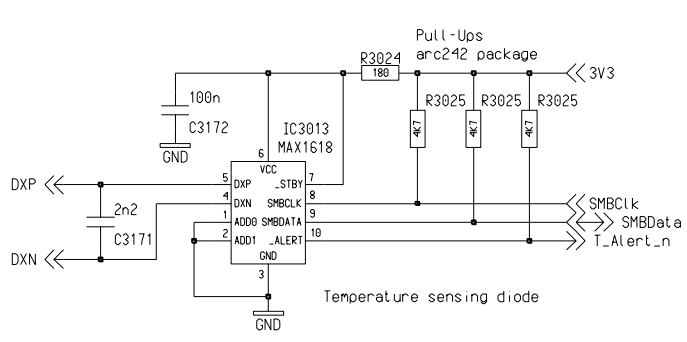


FPGA Configuration Signals

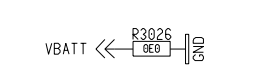


PWRDWN_B is unsupported (should be pulled high)

HSWAP_EN = '0' => User IOs have pull-up resistors during configuration

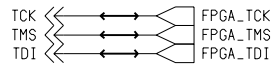


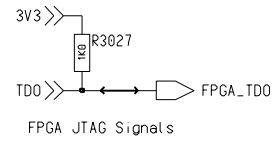
Temperature sensing diode



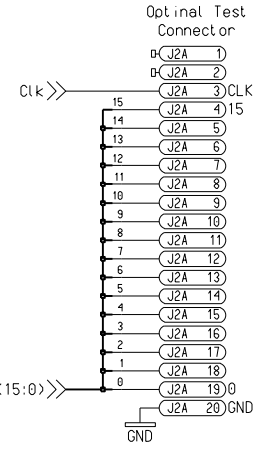
VBATT is decriptor key memory backup supply

FPGA Control signals

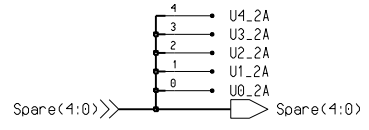


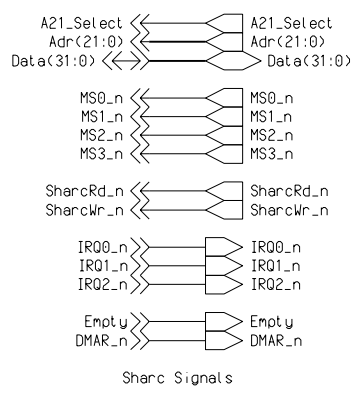


FPGA JTAG Signals

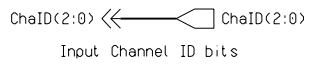


Testpoints force Spare lines to be accessible.

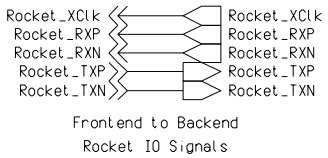




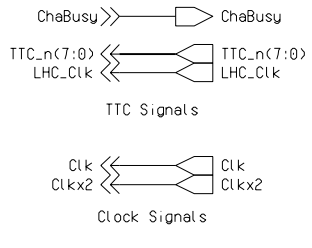
Sharc Signals



Input Channel ID bits



Frontend to Backend
Rocket IO Signals



TTC Signals

Clock Signals

channel_in		Rev 80
		Date 26 Jan 2005
Input FPGA Auxiliary Connections		Time 12:11:01 pm
Proj: MROD-X	Proj.No:38405	Name Peter Jansweijer
Peter Jansweijer	peterj@nikhef.nl	
NIKHEF ©ET-Nikhef Amsterdam	NATIONAAL INSTITUUT VOOR KERN-FYSICA EN HOGE ENERGIE-FYSICA KRUISLAAN 409, 020-592 2000 1098 SJ AMSTERDAM NEDERLAND	Size A3 / 4 1 4 A
		Dim 420 x 297 mm
		Page 6 of 6