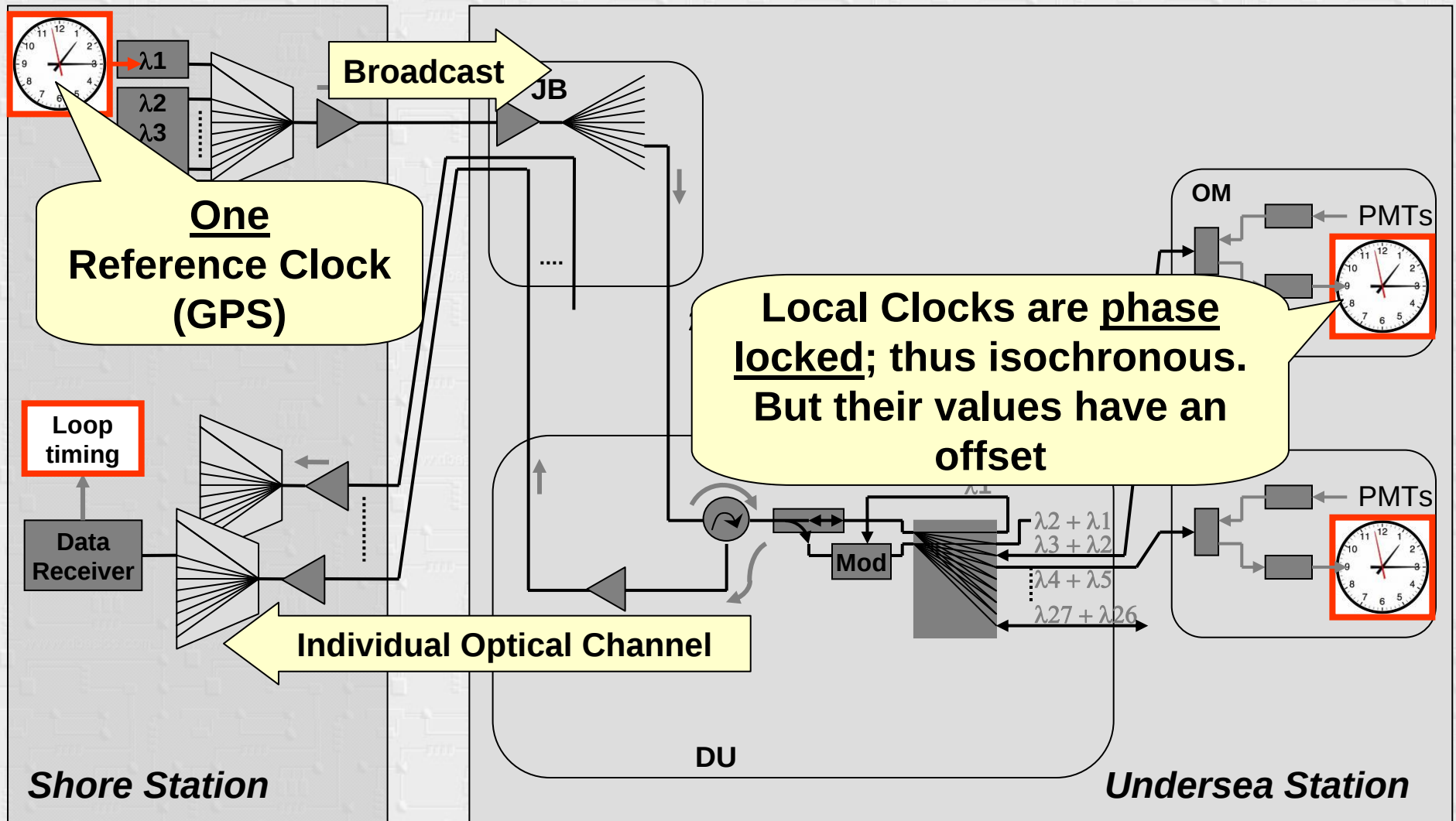
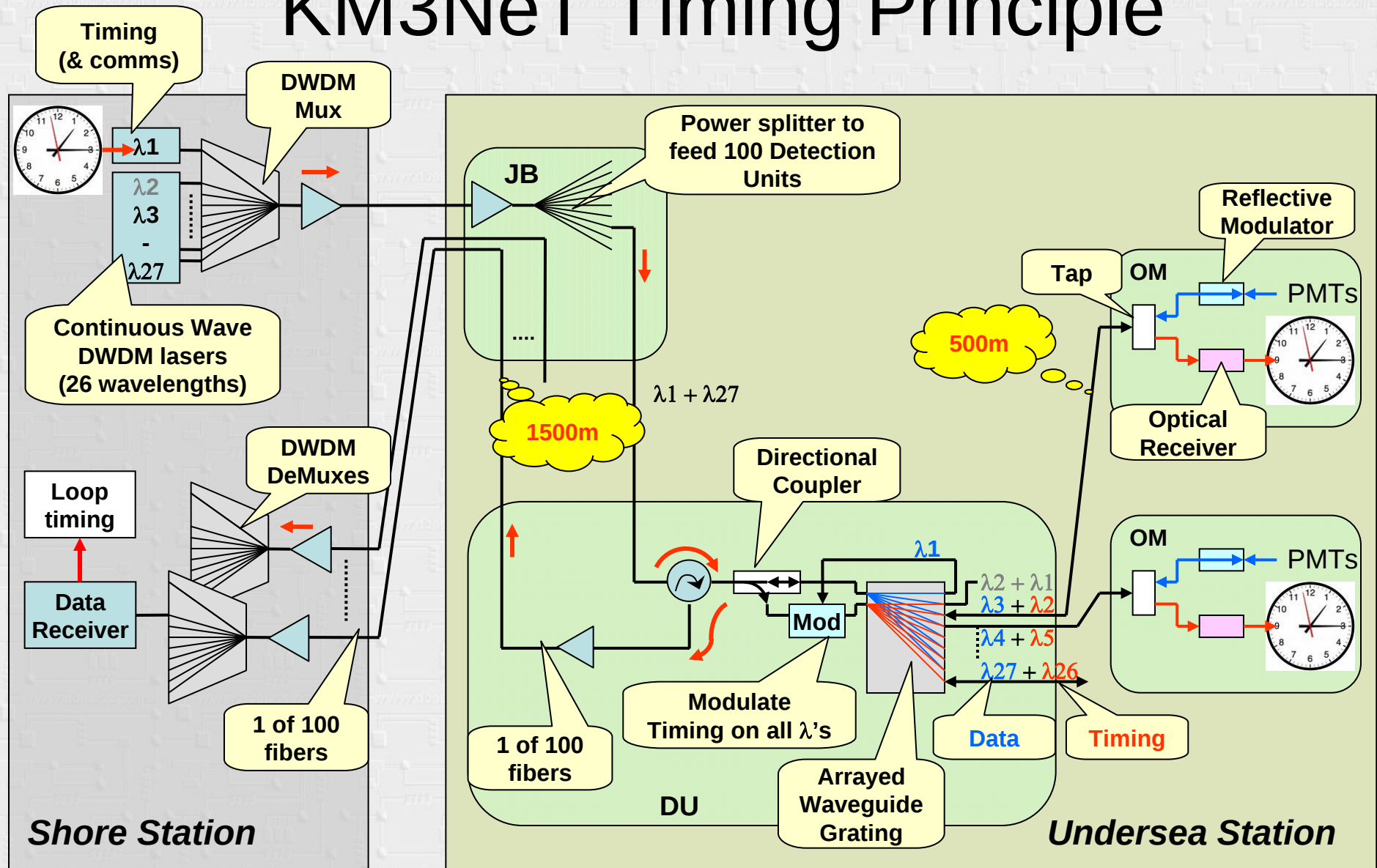


Transfer exact timing using a coded data communication channel

KM3NeT Timing Principle

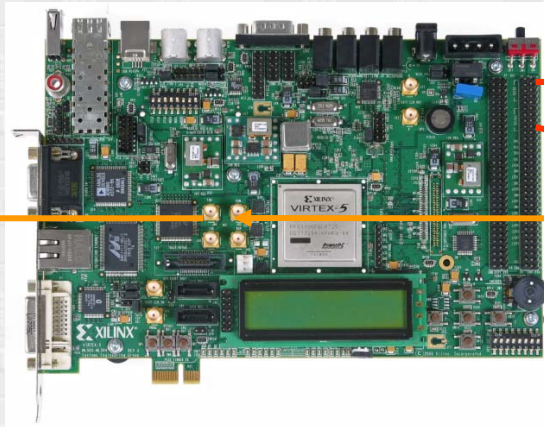


KM3NeT Timing Principle

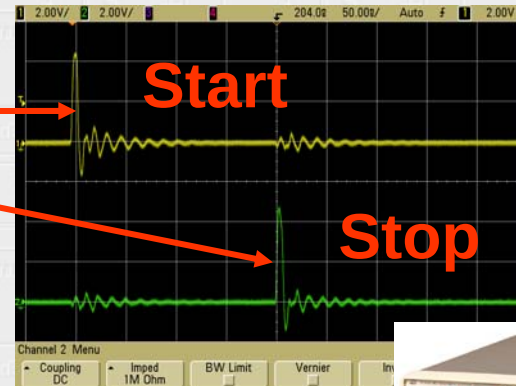


Timing over 8B10B Test Setup

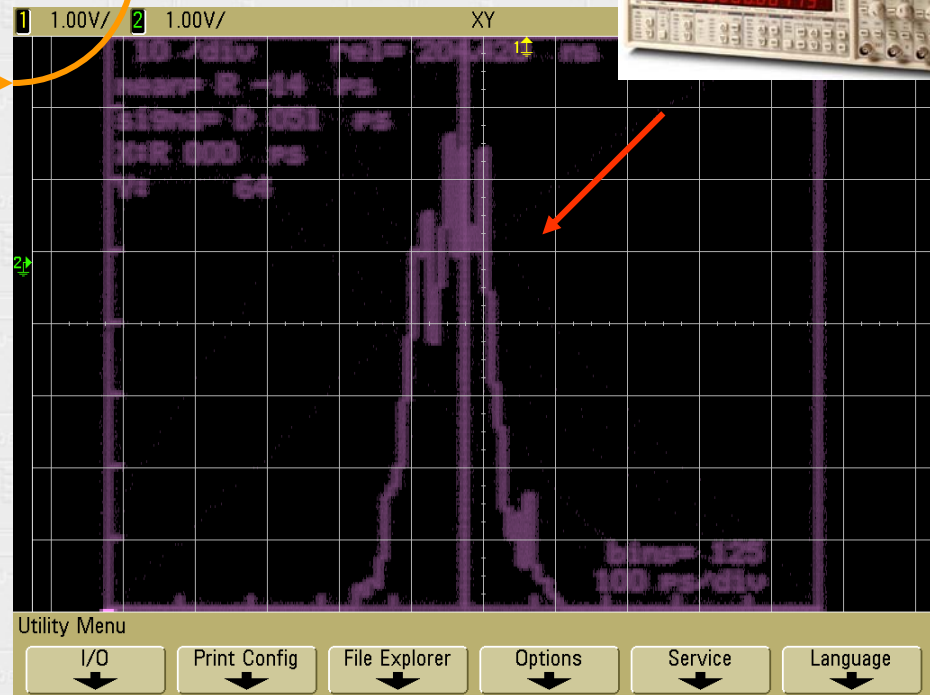
Tx
8B/10B
Encoded



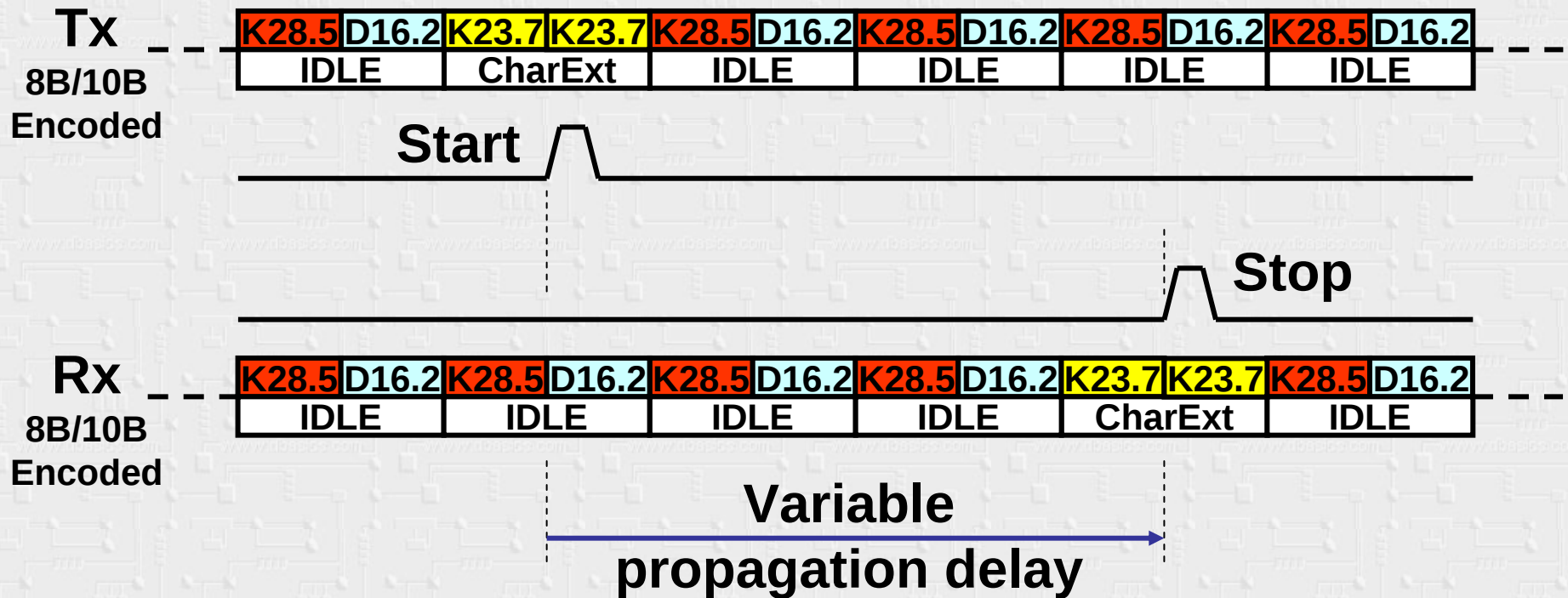
Rx
8B/10B
Encoded



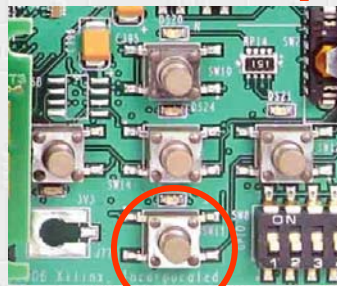
**Constant Impedance
Trombone Line**
 $0 \rightarrow 2 \times 10 \text{ cm} = 0 \rightarrow 700 \text{ ps}$



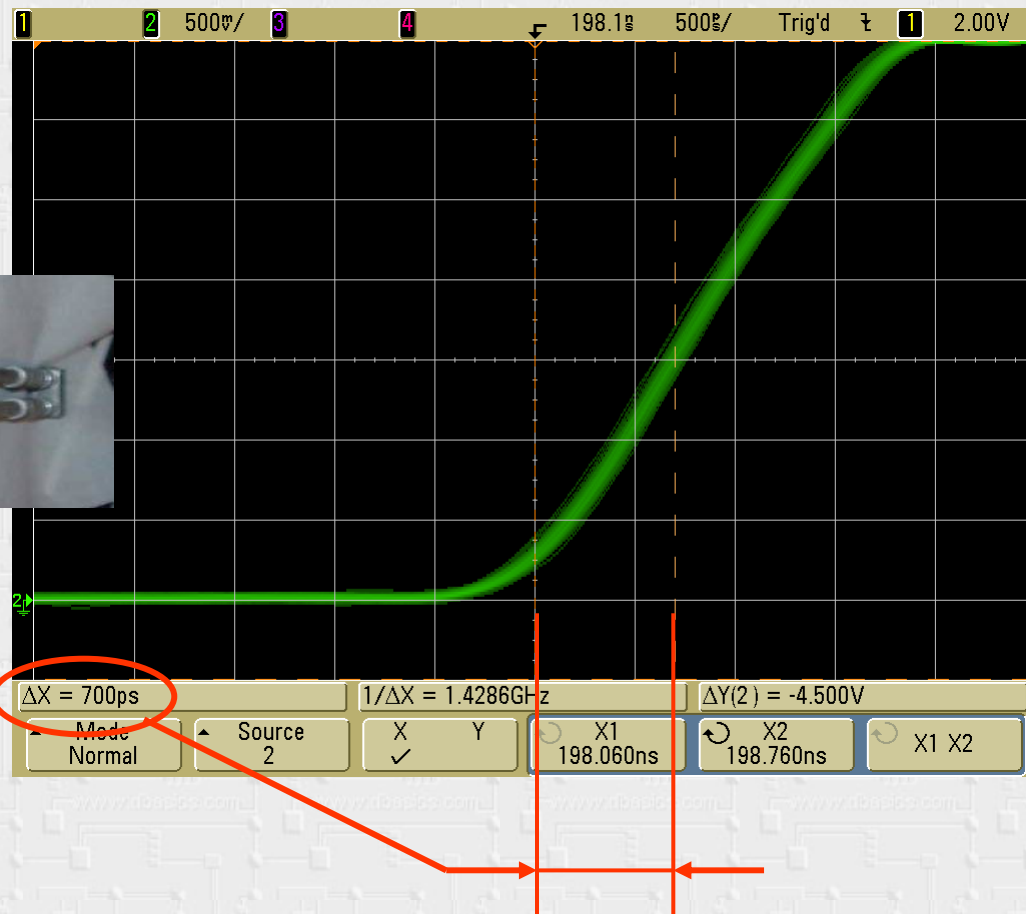
Timing over 8B10B



Variable Propagation Delay...

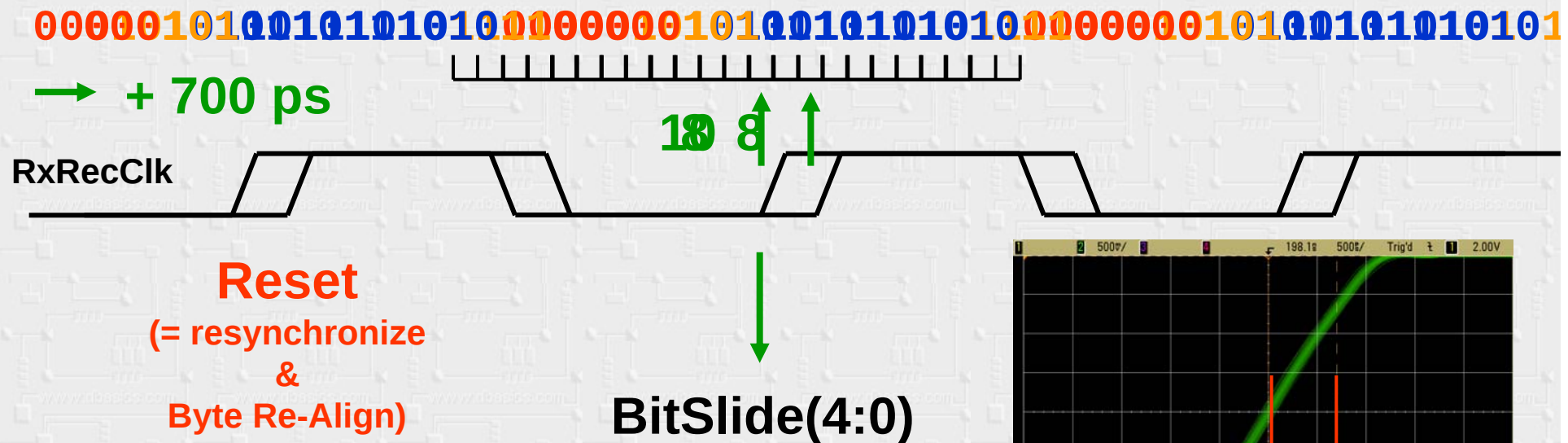


Reset
(= resynchronize)



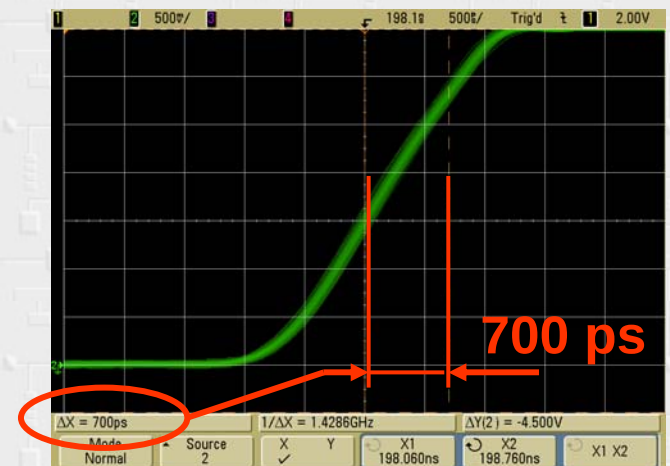
What is happening???

Closer Inspection...

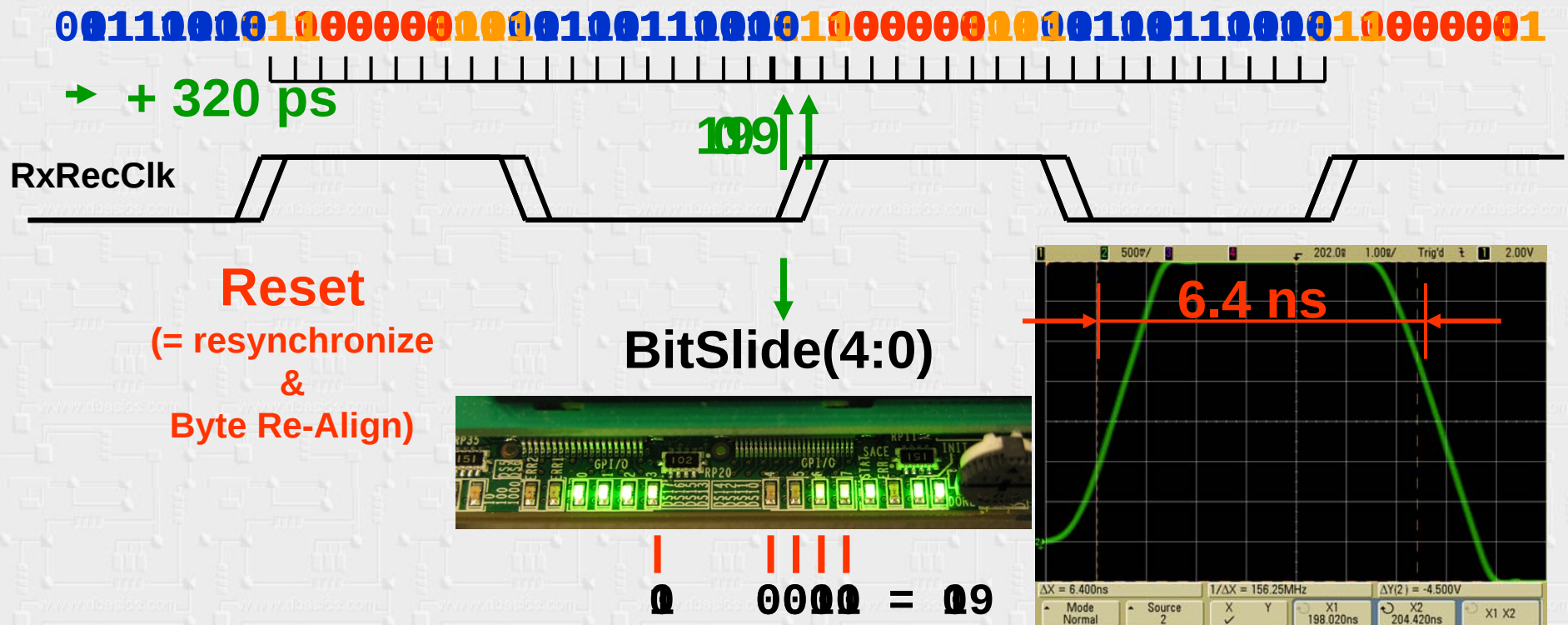


At 3.125 Gbps:

Absolute timing is determined by “Start/Stop” delay
(in 20 bit steps of 6.4 ns) **plus**
BitSlide fine delay (20 steps of 320 ps)



Demo: "On the edge"...



Conclusion

- Timing information is distributed inherent over a serial data channel **and can be used**
- Timing resolution is equal to a **Unit Interval** (= bit time; at 3.125 Gbps = 320 ps)
- Receivers in Optical Modules are all **phase locked** (thus *isochronous*) to one master clock (GPS) on shore

For the skeptic...

Does this work from board to board?

**Yes it
does!**

**Coarse time
(6.4 ns Steps)**

**3.125 Gbps via
Constant Impedance
Trombone Line**

**Receiver
Xilinx Virtex-5**

**Transmitter
Lattice LFSCM25**

**Receiver locked to
Transmitter
Oscillator**

**Transmitter
Crystal
Oscillator**

**Fine time
(320 ps Steps)**

Oct 14, 2008

PeterJ



Slide 10

Oct 14, 2008

PeterJ



Slide 11