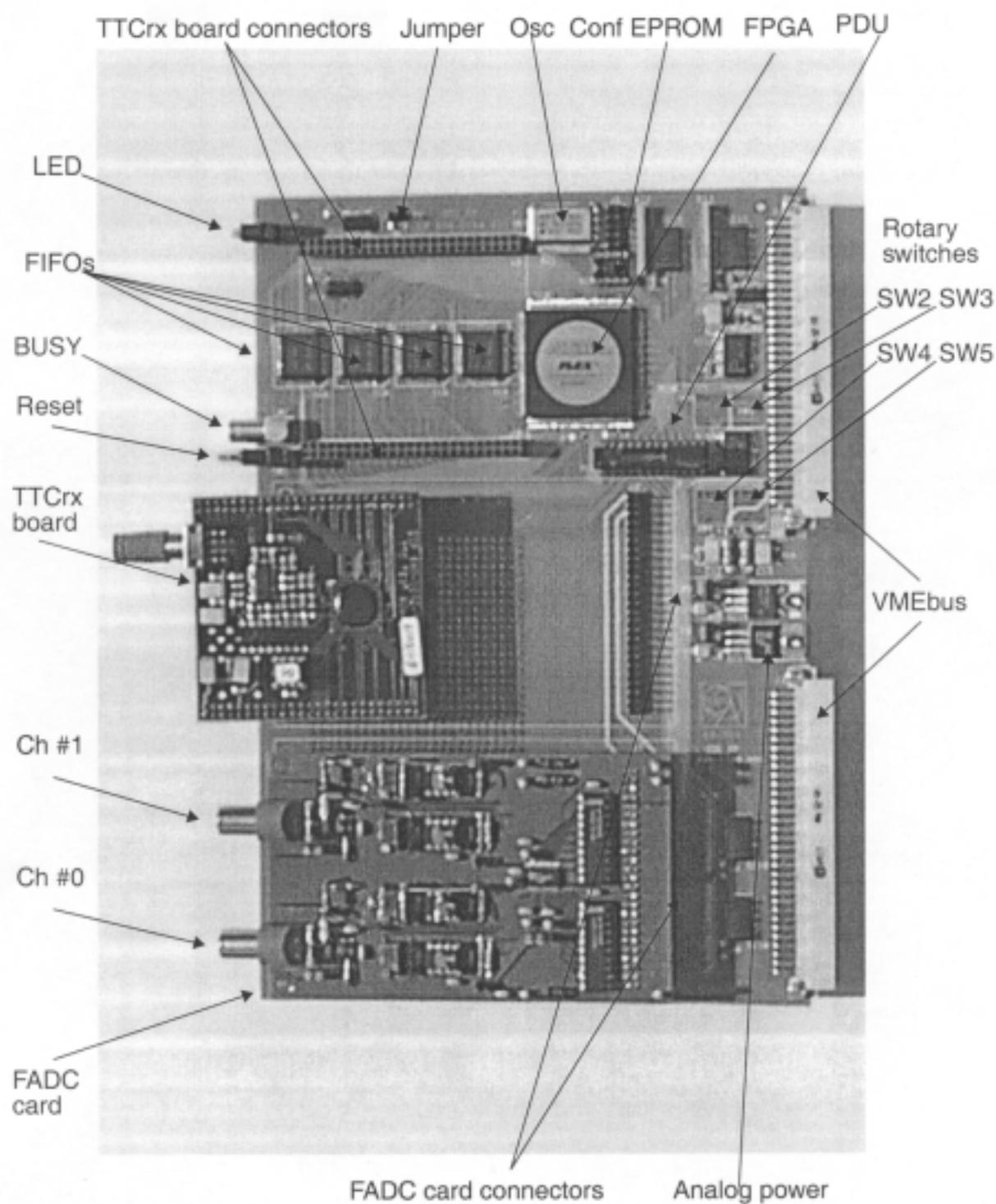
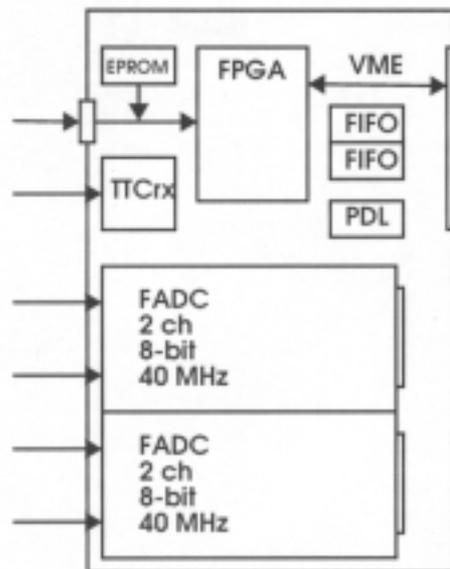


Second ODE prototype(ODE-PP)

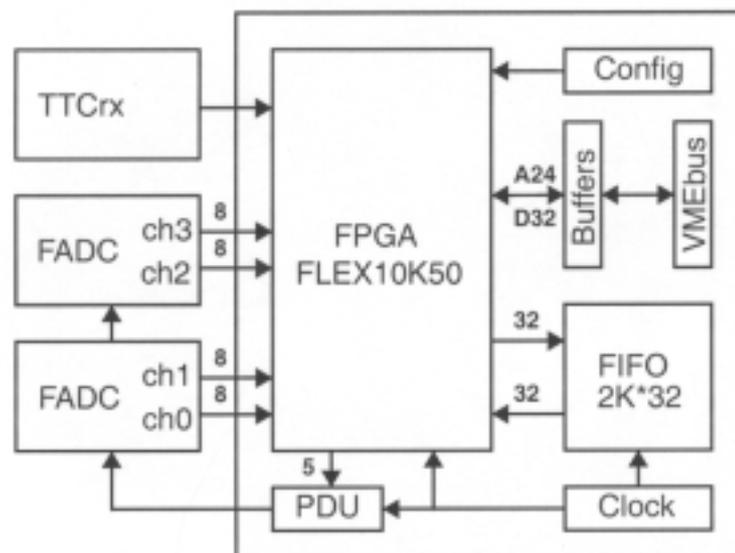


Second ODE prototype (ODE-PP)

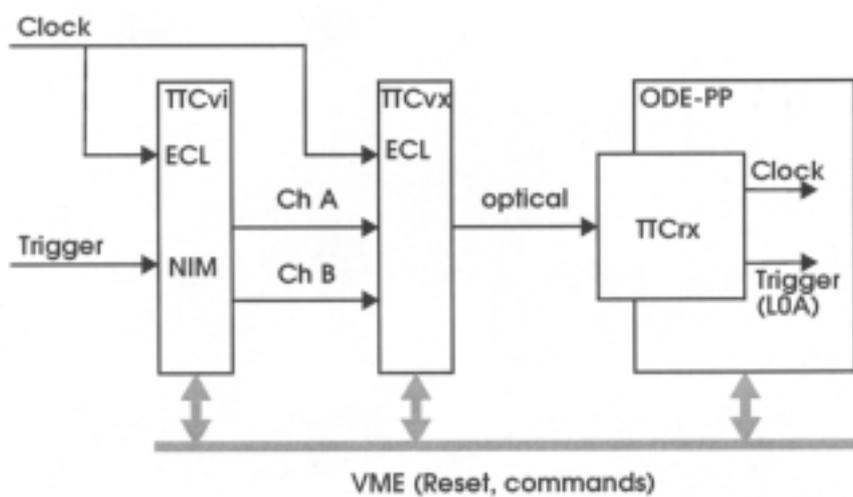
1999



- Form factor: 6U VME
- Fast control: TTCrx (Clk, L0A)
- FADC: 4 ch 8-bit 40 MHz
- Phase control: PDL (9+31*1 ns)
- FPGA: 1 FLEX 10K50-240
 - VME interface, control
 - FADC data capture
 - Synchronisation
 - FE emulator
- L1 buffer: SyncFIFO 2K*32
- Slow control: VME A24:D32
- FPGA config: EPROM (EPC1) download cable



TTC for ODE-PP



Test Set-up

