Straw Tube Drift Chamber for the LHCb Tracking System

Beijing (Tsinghua University), 18-11-2002

Outline:

Detector Design and Test-beam Results:
- LHCb Tracking & OT Design
- OT Modules & Straw Tubes
- Gas Mixture & Drift Time

Module Construction:
- Straw Material
- Injection Molding
- Module Design & Prototypes
- Station Frames

Electronics:
- FE Layout and TFC Distribution
- HV Boards
- OTIS TDC
LHCb Tracking System

B-production strongly “forward”-peaked ⇒ LHCb ~ “forward” spectrometer

- charged particles “analyzed” through magnet tracked with:
  - high-flux region (2%):
    - Si detector (Inner Tracker)
  - remaining area (98%):
    - straw drift-tubes (Outer Tracker)
Tracking System Functions

- measure charged-particles momenta:

- link VErtex LOcator ⇔ CAL/μ system

- provide angular info (with sufficient resolution) to Particle-IDentification system (RICH)
Tracking System Performance

- **high resolution:**
  10 MeV in \( B_s \rightarrow D_s K \) invariant mass
  \( \Rightarrow \delta p/p \sim 0.4\% \)

- **high efficiency (multi-particle f.s.):**
  80% rec. eff. \( B_s \rightarrow D_s (KK\pi) K \)
  \( \Rightarrow 95\% \) tracking efficiency
The Outer Tracker Design

B-Field vertical ⇒ measure \(x\)-coordinate

OT Station consist of 4 layers:
- \(XUVX\) (\(\theta_{u,v} = \pm 5^\circ\) sufficient to reduce combinatorial)

modular design:
layers are composed of modules
The Outer Tracker Design (cont’d)

**IT/OT Boundary** optimized on the basis of **occupancy** studies:

*require average occupancy < 10%*
OT Module Design

Straw Tubes packed in double-layered modules

- 64-cells wide
- only ~0.7% of 1 $X_0$:
  - “light” panels
    (honeycomb core with carbon skins)
  - “light” straws
Straw Tubes

Cell diameter ~5mm:
- reasonable occupancy
- sufficiently fast signal collection time
  - $T \leq 25\text{ns}$, unrealistic
  - $T \leq 50\text{ns}$, workable

(Contamination of events from neighboring bunch crossings)
Gas Mixture and Drift Time

$T \leq 50\text{ns} \Rightarrow$ fast drift gas: add $\text{CF}_4$ to basic $\text{Ar/CO}_2$ mixture

Drift-time spectra measured …

…and reproduced with GARFIELD simulation
Test Beam Results

Ar(75)/CO₂ (10)/CF₄ (15) selected as baseline

Measured t-r relation, coordinate resolution (~0.2mm), efficiency (~96%), etc.
CF$_4$ presence $\Rightarrow$ chose polymer as straw material:

- 0.040 mm thick Kapton XC (25\% volume doping with Carbon),
  $(370 \, \Omega/cm^2 \Leftrightarrow \sim 12 \, K\Omega/m)$

- Passed extensive ageing tests

- two windings ensure sufficient gas tightness
The cathode (straw) material determines the level of analog (straw-to-straw) cross-talk.

I.e. different choices of the outer winding material:

- 0.025mm Aluminum $\Rightarrow$ 0.5% analog cross talk
- 0.040mm Kapton XC $\Rightarrow$ 1.8% analog cross talk

Baseline solution: outer winding of pre-laminated Kapton XC (0.025mm)/Aluminium (0.012mm) foil

(Straw winding material budget $\sim$0.12 of 1$X_0$)
Injection-Molded Parts

For the construction of the OTR modules a large number (~400000) of “small” pieces is required:

- **wire locators**: inserted in the straw to support the wire every 80 cm
- **middle- and end-blocks**: support wire at straw ends and define counting-gas volume

This large number of small parts can be produced with injection-molding techniques, without compromising the **tight local tolerances** (0.02⁻⁰.⁰5mm).
Detailed Design of Detector Modules
Module Prototypes

OT Module Prototype (2.5m long) built at NIKHEF
Module Prototypes (cont’d)

OT Module Prototype (1m long) built at Heidelberg
OT Electronics

FE Electronics:
- wire feed-through, HV, preamp, TDC

FE Electronics:
- Data serializer

FE Electronics:
- Control & Bias, Monitor,…

L1 Electronics

⇒ DAQ and L1 Farm

On-Detector

Counting Room
OT Electronics (cont’d)

In total: 53.8 k channels
1680 TDC chips
432 GOL chips

8B/10B (Gbit Ethernet, 1.6Gbit/s)

BCXO (40MHz)

OTIS

3 x 144 = 432 optical links

L1 Buffer
FE Electronics Components
FE Electronics Mock-up Models

Needs modeling to assess mechanical details
HV Boards

Not just a bunch of capacitors! **Strict demands:**

- **signal** \((2\text{fC/10ns} \times 300\Omega = 0.06 \text{ mV})\) and **HV** \((\sim 1500\text{V})\) separation

- **good transmission of fast** \((\sim 10\text{ns})\) **signal** \(\Rightarrow\) **GND plane all along signal path**

- **noise level** \(<<\) **signal** \((2\text{fC/10ns} = 200 \text{ nA})\)

- **compact design:** 5mm channel pitch and small-space constraints
  - \((\sim 40\text{mm for the whole thickness of the FE box})\)

- **high reliability:** 10 years operation with scarce possibilities of access for repair
HV Boards Design

Main design ingredients:

- high-quality capacitors JOHANSON 302R29W331KV4E
- capacitors “buried” inside the PCB

First prototypes unsuccessful:
after 4 weeks test, 19 broken channels
out of 10x32 (6 out of 10 boards with
at least one broken channel)!

- air gap under capacitors
- remains of cleaning “slurry”
- inaccurate hand-placing of capacitors
HV Boards Production

Improved production procedure (19 HV boards):

- carried out under vacuum
- pick-and-place glueing avoids air-gap under capacitors
- accurate (robot) placement of capacitors
- soldering area cleaned with plasma (instead of slurry)

First tests: $I_{TOT}(608\text{chans}) < 50\text{nA}$, up to HV=$+2.5\text{kV}$ and $T=80^\circ\text{C}$

Long-term tests of ~1000 channels forthcoming…
OTIS TDC

- Drift time measurement
- Mounting on detector
- Approx. 50,000 channels
- 4 TDC (32 channels each) gets serialised and transmitted optically (1.28GBit/s)

OTIS TDC designed at ASIC Heidelberg
(Harald Deppe, Uwe Stange, Ulrich Trunk, Ulrich Uwer)

Chip Requirements:
- ≤1ns resolution (6 bit)
- 40MHz, clock driven design
- up to 10% occupancy
- radiation hard design
- drift times of up to 50ns
- 1.1MHz L0 trigger rate
- 4µs trigger latency
  (pipeline length: 160)
First prototype with basic functionality
~700,000 transistors
5100µm x 6000µm
Tape out: 15/04/2002
Delivery: 29/07/2002
Small test PCB with possibility to connect ASD and GOL chips
OTIS v1.0 (cont’d)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Status</th>
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<tbody>
<tr>
<td>PowerUp Reset</td>
<td>as expected</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>550mW</td>
</tr>
<tr>
<td>DLL: Lock Time</td>
<td>≤ 1µs</td>
</tr>
<tr>
<td>Lock Lost</td>
<td>not observed</td>
</tr>
<tr>
<td>DAC</td>
<td>as expected</td>
</tr>
<tr>
<td>Slow Control</td>
<td>as expected</td>
</tr>
<tr>
<td>Fast Control: Memory and Trigger Management, Data Output, Debug Features</td>
<td>no errors found</td>
</tr>
<tr>
<td>Memory Selftest</td>
<td>problems</td>
</tr>
<tr>
<td>Drift Time Encoding</td>
<td>not yet understood</td>
</tr>
</tbody>
</table>

**OUTLOOK**
- Further investigations concerning drift time encoding
- More chips, performance tests, random trigger tests, ...
- Operation with detector prototype
- Commissioning of the read out chain including TTCrx
Station Frames

Proposal contained in the OT TDR…

- Modules mounted with **dowel pins** onto Al **precision strips** defining the module positions
- 4 layers of each station mounted on Al frames
- Each frame consists of two halves

...a mock-up module for study was also built at NIKHEF
Working group to revise frame-design constraints and solutions:

- Collaborate with ITR group for common solution
- Revise global strategy:
  - Stations should move independently
  - Positioning accuracies and reproducibility
- Krakow group producing a case study

Global Movement (TDR)  
Independent Movements (Krakow)
Project Milestones