The DCS system in the Atlas muon chamber

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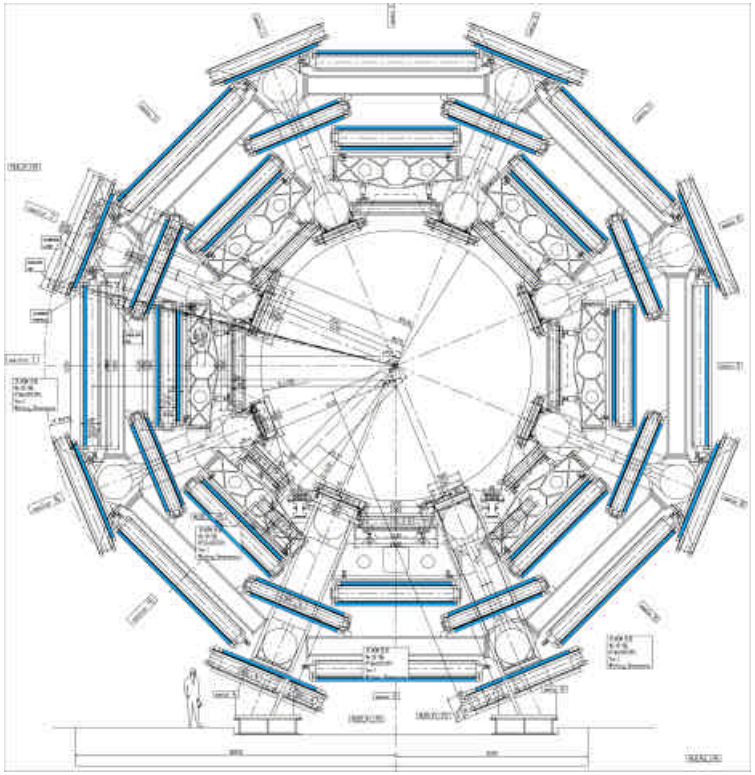
Atlas RPC muon system location

	Zmin (cm)	Zmax (cm)	Rmin (cm)	Rmax (cm)
BMF	63.1	872.2	839.1	847.1
BML	15	966	750.6	758.6
BMS	13.5	945.5	839.1	847.1
BOF	60.8	1267.9	1035.5	1043.5
BOL	15	1225.2	985.3	993.3
BOS	1	1383.2	1025.8	1033.8



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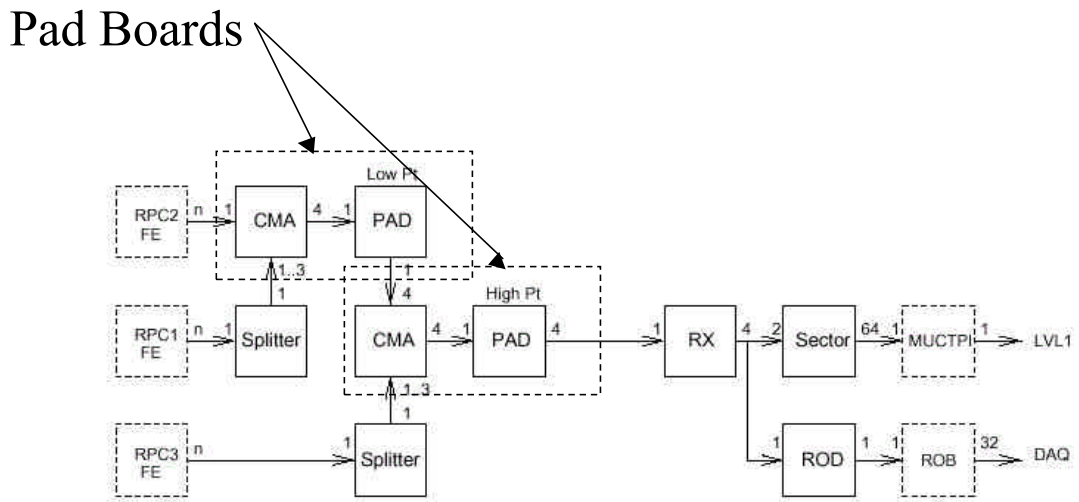
Location of the PAD boards in the LVL1 muon Trigger



There are 832 PAD board each one with an ELMB CAN node.

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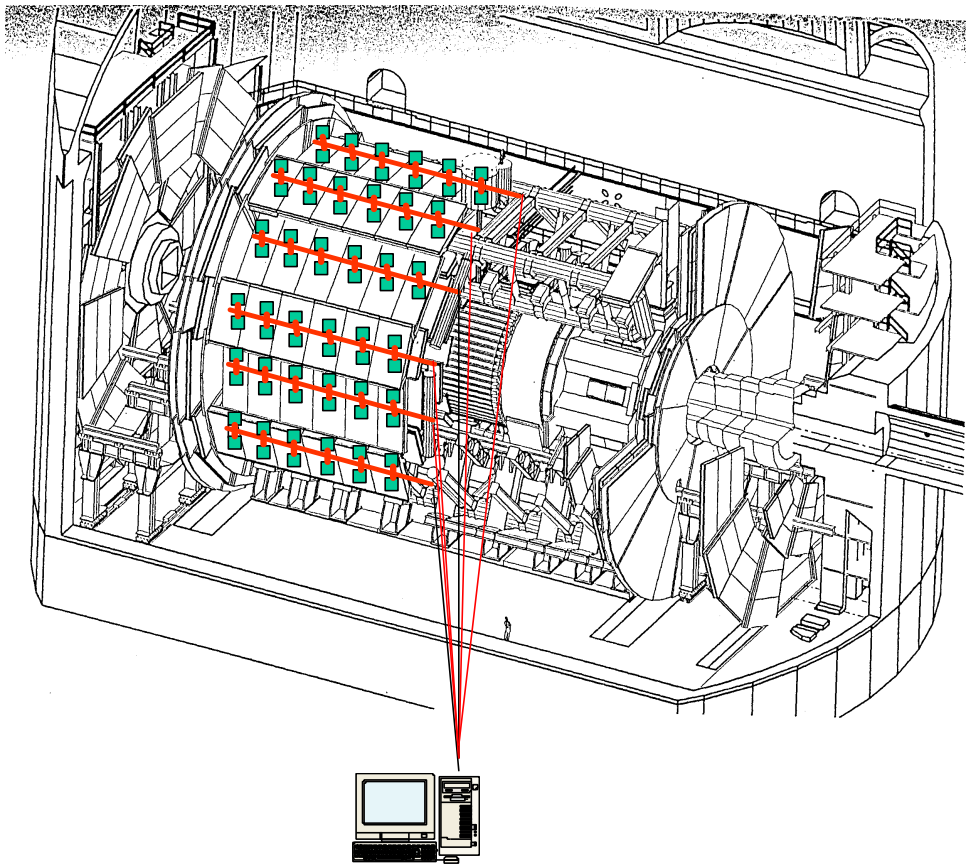
Can branches in Atlas muon detector

832 CAN Nodes
Divided in chain of:
6x2 =12 nodes
7x2=14 nodes
8x2=16 nodes

about 65 branches

or 34 if branches grouped in max 32 nodes.



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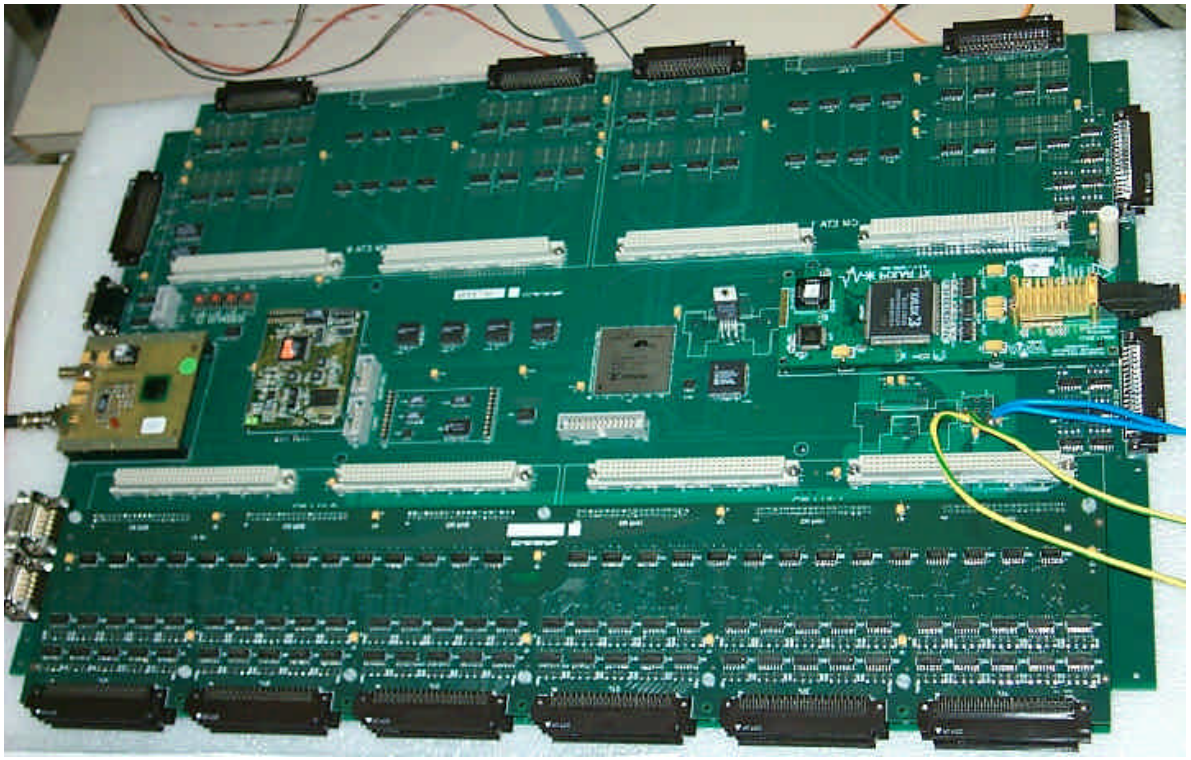
PAD board with TTCrx ELMB XCV200 and Optical Link



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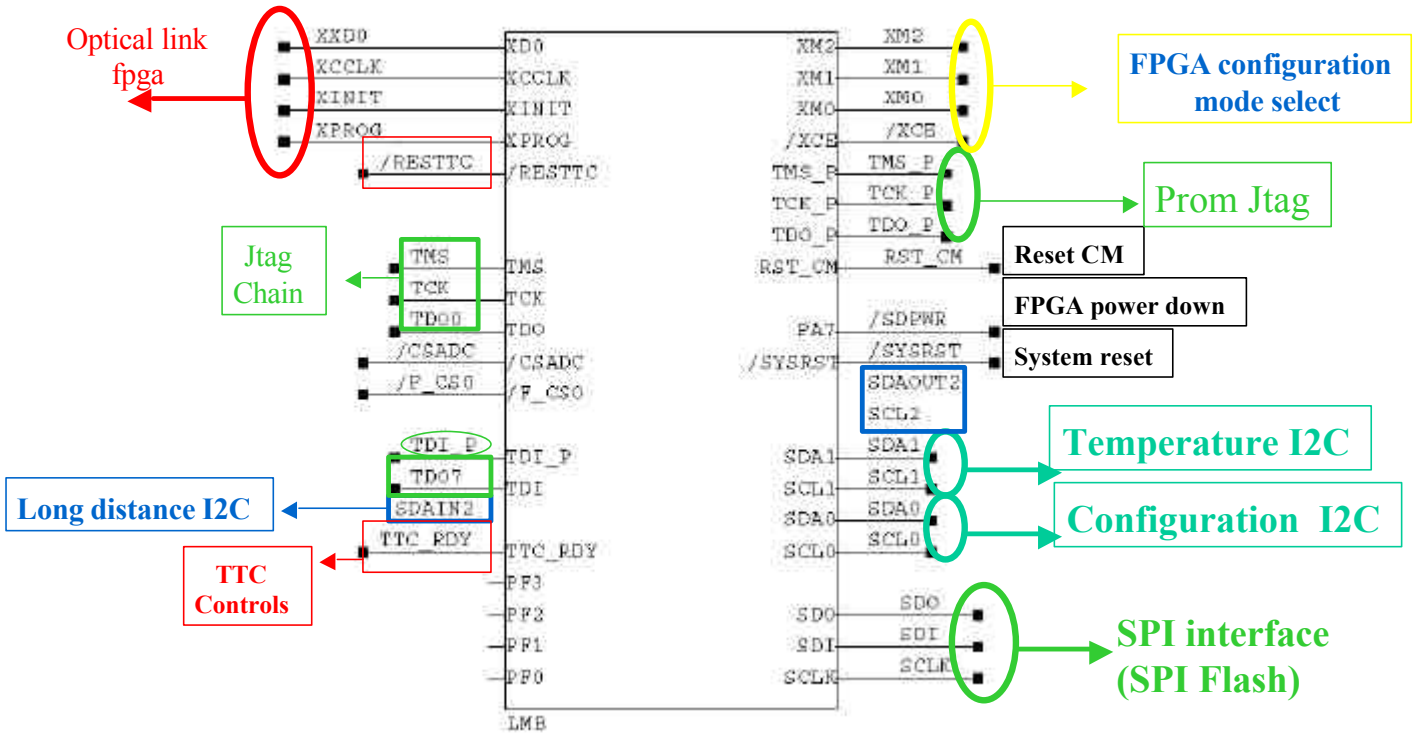
PAD ELMB signals



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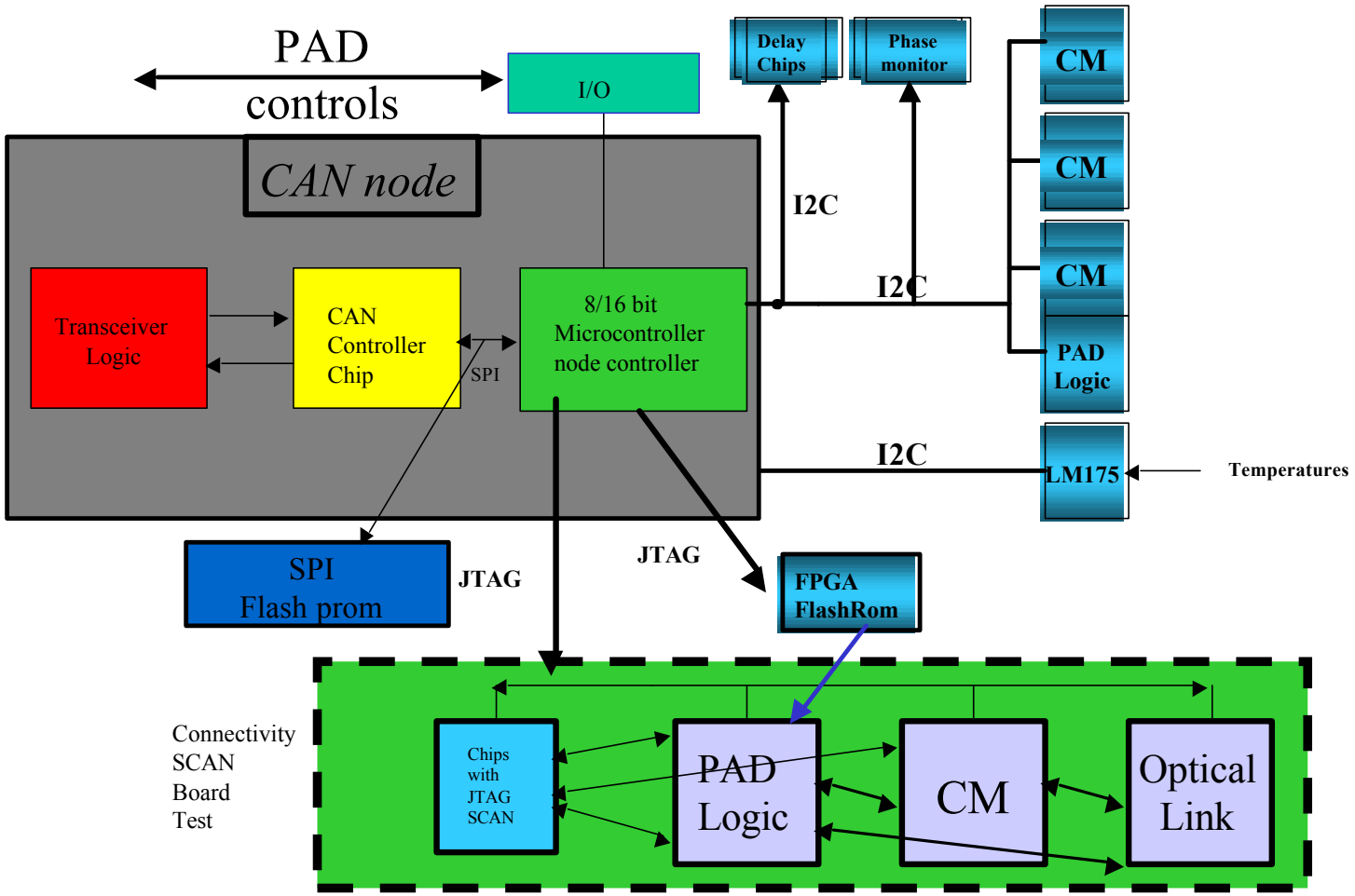
CAN node connections



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Pad devices controlled by ELMB

I2C devices network ID assignement

Device	A6	A5	A4	A3	A2	A1	A0	Address	Device
LM75 Splitter	**1**	**0**	**0**	**1**	1	1	0	4Eh	LM75 Split
LMB								Master	LMB
LM75 PAD	**1**	**0**	**0**	**1**	1	0	1	4Dh	LM75 PAD
LM77 on Link	**1**	**0**	**0**	**1**	0	0	0	4Ch	LM77 on Li
LM75 CME1	**1**	**0**	**0**	**1**	0	1	1	4Bh	LM75 CME
LM75 CME0	**1**	**0**	**0**	**1**	0	1	0	4Ah	LM75 CME
LM75 CMF1	**1**	**0**	**0**	**1**	0	0	1	49h	LM75 CMF
LM75 CMF0	**1**	**0**	**0**	**1**	0	0	0	48h	LM75 CMF
PCF8575 Link	**0**	**1**	**0**	**0**	1	0	0	20h	PCF8575 L
LMB								Master	LMB
PAL	1	0	0	0	1	0	1	45h	PAL
PAD	1	0	0	0	1	0	0	44h	PAD
CME1	1	0	0	0	0	1	1	43h	CME1
CME0	1	0	0	0	0	1	0	42h	CME0
CMF1	1	0	0	0	0	0	1	41h	CMF1
CMF0	1	0	0	0	0	0	0	40h	CMF0
TTC	0	0	1	0	1	0	**X**	15h ÷ 14h	TTC
PRODE3	**0**	0	1	0	0	**X**	**X**	13h ÷ 10h	PRODE3
PRODE2	**0**	0	0	1	1	**X**	**X**	0Fh ÷ 0Ch	PRODE2
PRODE1	**0**	0	0	1	0	**X**	**X**	0Bh ÷ 08h	PRODE1
PRODE0	**0**	0	0	0	1	**X**	**X**	07h ÷ 04h	PRODE0
LMB								Master	LMB
AD7418	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**28h**	AD7419

JTAG daisy chain device assignement

PAD	7								PAD
CME1	6								CME1
CME0	5								CME0
CMF1	4								CMF1
CMF0	3								CMF0
LINK	2								LINK
TTC	1								TTC
LMB	Master			***JTAG ctrl network***					LMB
EEPROM	1								EEPROM
LMB	Master			***JTAG prom network***					LMB

- I2c Temperature sensors
- TTC
- Delay chips
- FPGA
- Flash prom FPGA
- Flash prom SPI
- I2c I/O registers
- Coincidence maxtrix
- Optical link controls

Initialization parameters used in the LVL1 Muon Barrel system.

(Some are not reloaded every run)

item	data-base name	type	number per		bits/chan	destination device	agent	R/W	number of devices	number of channels	total bytes
on-detector											
CMA channel masking to 0 for trigger		bits	6	CMA	32	CMA	I2C	RW	3328	19968	79872
CMA channel masking to 1 for trigger		bits	6	CMA	32	CMA	I2C	RW	3328	19968	79872
CMA channel masking to 0 for readout		bits	6	CMA	32	CMA	I2C	RW	3328	19968	79872
CMA input pipeline depth		bits	24	CMA	4	CMA	I2C	RW	3328	79872	39936
CMA mode register		bits	1	CMA	32	CMA	I2C	RW	3328	3328	13312
CMA coincidence windows threshold 0		bits	64	CMA	32	CMA	I2C	RW	3328	212992	851968
CMA coincidence windows threshold 1		bits	64	CMA	32	CMA	I2C	RW	3328	212992	851968
CMA coincidence windows threshold 2		bits	64	CMA	32	CMA	I2C	RW	3328	212992	851968
CMA overlap window sizes		bits	1	CMA	32	CMA	I2C	RW	3328	3328	13312
TTCRx configuration register		bits	1	TTCRx	69	TTCRx	I2C	RW	832	832	7176
TTCRx control register		bits	1	TTCRx	8	TTCRx	I2C	RW	832	832	832
TTCRx coarse delay register		bits	1	TTCRx	8	TTCRx	I2C	RW	832	832	832
TTCRx fine delay register		bits	1	TTCRx	8	TTCRx	I2C	RW	832	832	832
link TX configuration		bits	1	TX	16	CANnode	IO bits	R	416	416	832
link Temperature probe		ADC	1	TX	8	CANnode	IO bits	R	416	416	416
PAD FPGA configuration string		bits	1	PAD FPGA	1335872	Flash mem	JTAG	RW	416	416	69465344
PAD delay chip configuration		bits	1	PRODE	5	PRODE	I2C	RW	2496	2496	1560
PAD temperature sensors		ADC	1	I2C T sensor	8	T sensor	I2C	RW	4160	4160	4160
PAD voltage sensors		ADC	1	I2C T sensor	8	T sensor	I2C	RW	4160	4160	4160
off detector											
RX board registers											
Sector logic EnaTCcheck registers		bits	2	SL	32	SL	VME	RW	64	128	512
Sector logic SetTCcheck registers		bits	48	SL	32	SL	VME	RW	64	3072	12288
Sector logic EnableOPLcheck registers		bits	1	SL	32	SL	VME	RW	64	64	256
Sector logic SetOPLcheck registers		bits	8	SL	32	SL	VME	RW	64	512	2048
Sector logic other registers											
ROD registers											

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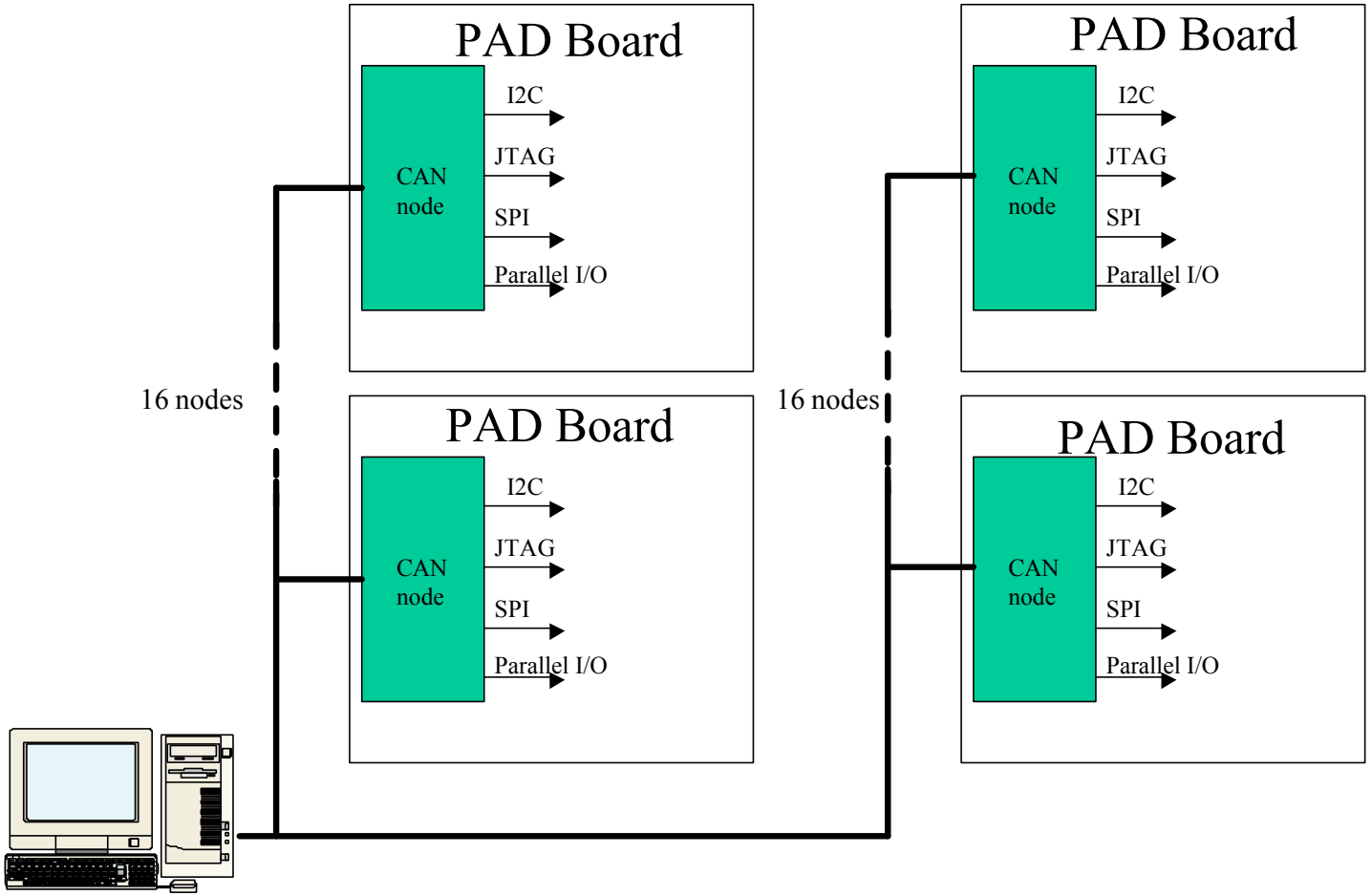
Connection of CAN bus nodes



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Tools we use:

- ELMB board
- IXXAT 165 PCI CANBUS board
- Ixxat CAN Analyzer
- IXXAT canopen Client
- Ixxat Tincan interface PCMCIA
- Virtual Can Interface Library (VCI)
- CAN open Master API

Software development:

- We start to write new software for ELMB using ICCAVR.
- As guideline the document from Henk B&B
  we integrate I2C in the CAN node.
- Software for readback written for AVR evaluation board.
- We write new ccan.c and ccan.h to interface ixxat boards
  (*available to the collaboration on request).
- we use the ELMBldr from Henk B&B using the our Ixxact ccan.c .h .

PVSS II:

- We wait for collaboration decision about final PCI boards.
- PVSS II now working in NI boards
- Is it NI final boards ??
- Is it OPC server portable for other boards ?
- We want to start with PVSS II in 2002 is it NI the only choice.

ELMB in the final system:

- We need about 1000 boards including spares for the final system.
- We have now enough boards also for 2002 .
- It is time to start to think about the structure of the final system. how many PC ?
- how many CAN node for each PC ?