The use of ELMB for FPGA checking

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Working group:

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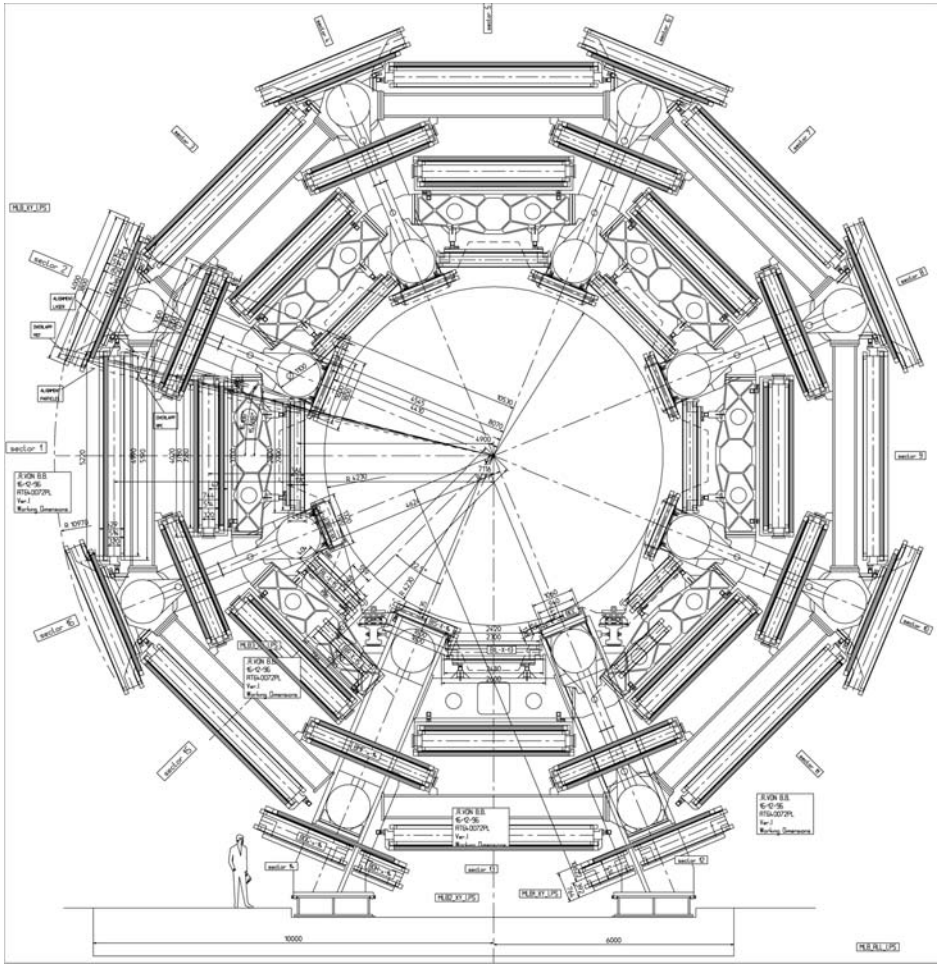
(A)Hardware
(B)Software
(C)System
(D)Radiation test.

Atlas RPC muon system location and radiation levels

	Zmin (cm)	Zmax (cm)	Rmin (cm)	Rmax (cm)
BMF	63.1	872.2	839.1	847.1
BML	15	966	750.6	758.6
BMS	13.5	945.5	839.1	847.1
BOF	60.8	1267.9	1035.5	1043.5
BOL	15	1225.2	985.3	993.3
BOS	1	1383.2	1025.8	1033.8

	SRL_{tid} (Gy $10y^{-1}$)	SRL_{see} (>20 MeV h cm^{-2} $10y^{-1}$)
BMF	3.02E+00	4.69E+09
BML	3.04E+00	5.65E+09
BMS	3.03E+00	4.73E+09
BOF	1.19E+00	4.08E+09
BOL	1.33E+00	4.21E+09
BOS	1.26E+00	4.10E+09



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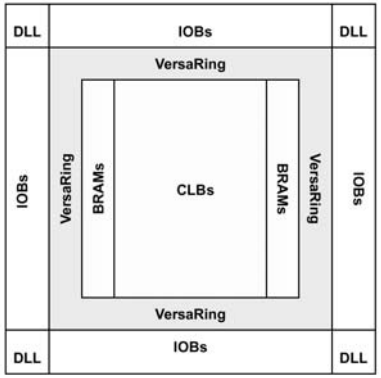
Xilinx Virtex 2.5V device



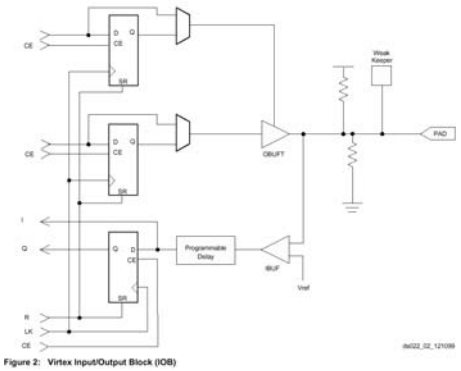
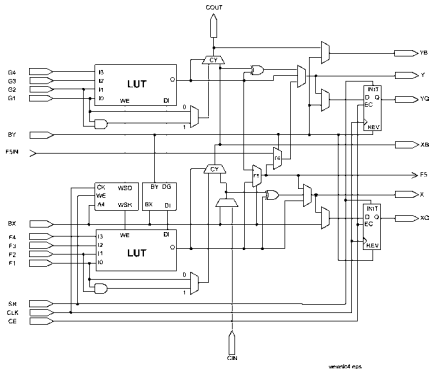


Figure 2: Virtex Input/Output Block (IOB)

Fast, high-density Field-Programmable Gate -
- System performance up to 200 MHz
Built-in clock-management circuitry
- Four dedicated delay-locked loops (DLLs) for advanced clock control
- Four primary low-skew global clock distribution nets,



Each Block SelectRAM is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port .The data widths of the two ports can be configured independently.
=> built-in bus-width conversion.
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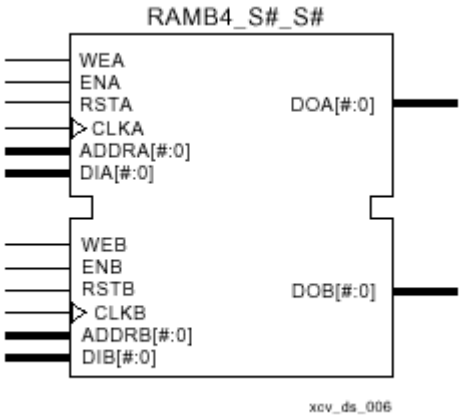


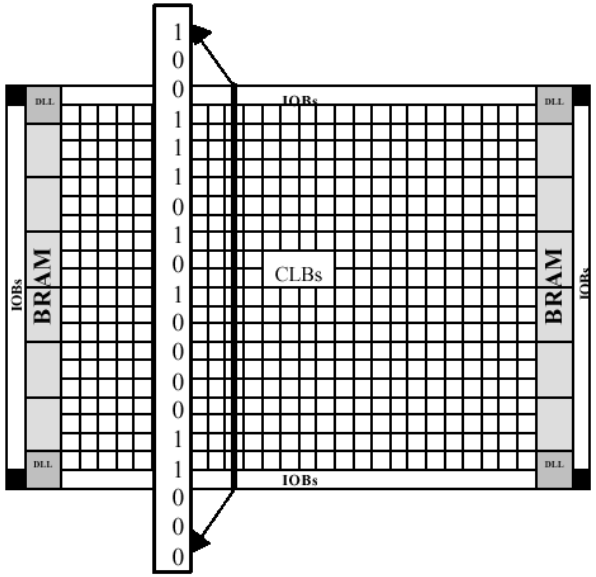
Table 5: Virtex Block SelectRAM Amounts

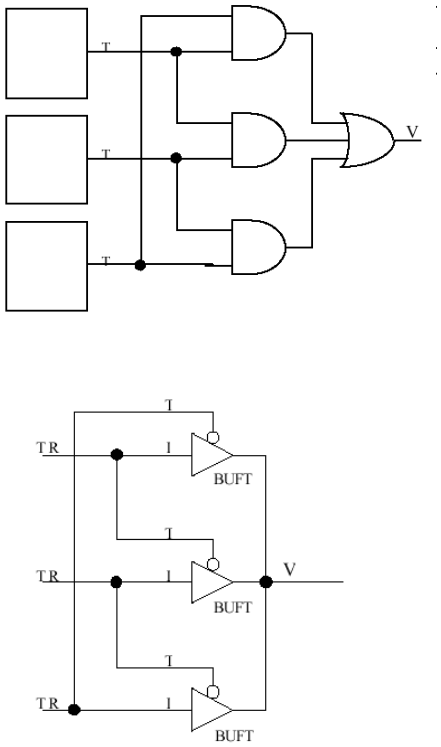
Virtex Device	# of Blocks	Total Block SelectRAM Bits
XCV200	14	57,344

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Maximum SelectRAM+™ Bits
XCV200	236,666	28x42	5,292	284	57,344	75,264

SEU in FPGAs devices

Asic FPGA
1flip-flop -> 30 flip-flop

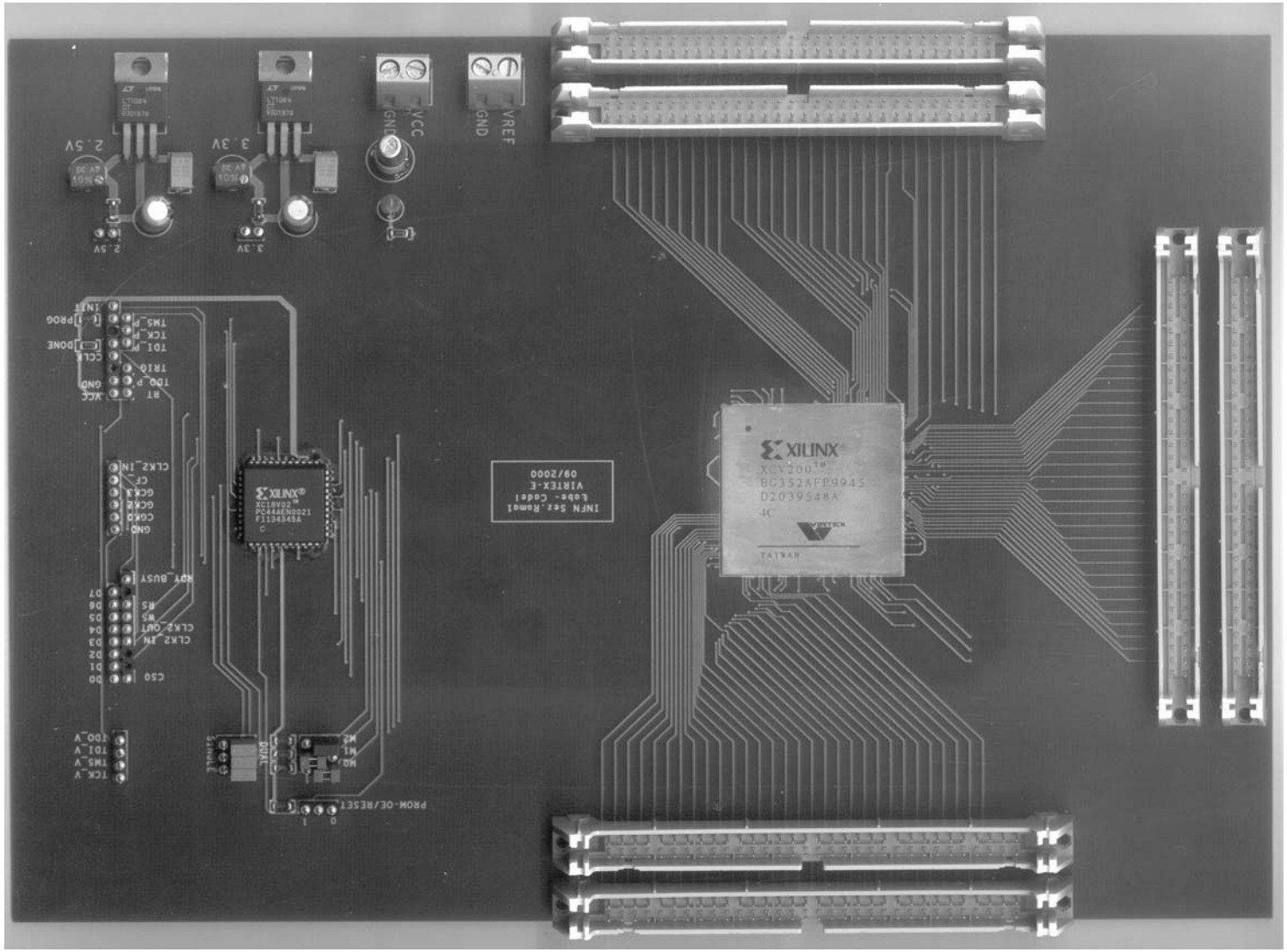




Mitigation circuits for SEU

- FPGA logic cross section.
- FPGA configuration cross section.
- FLASHProm SEU cross section.

Xilinx XCV200 and Flashprom 18V02 Louvain Test Board



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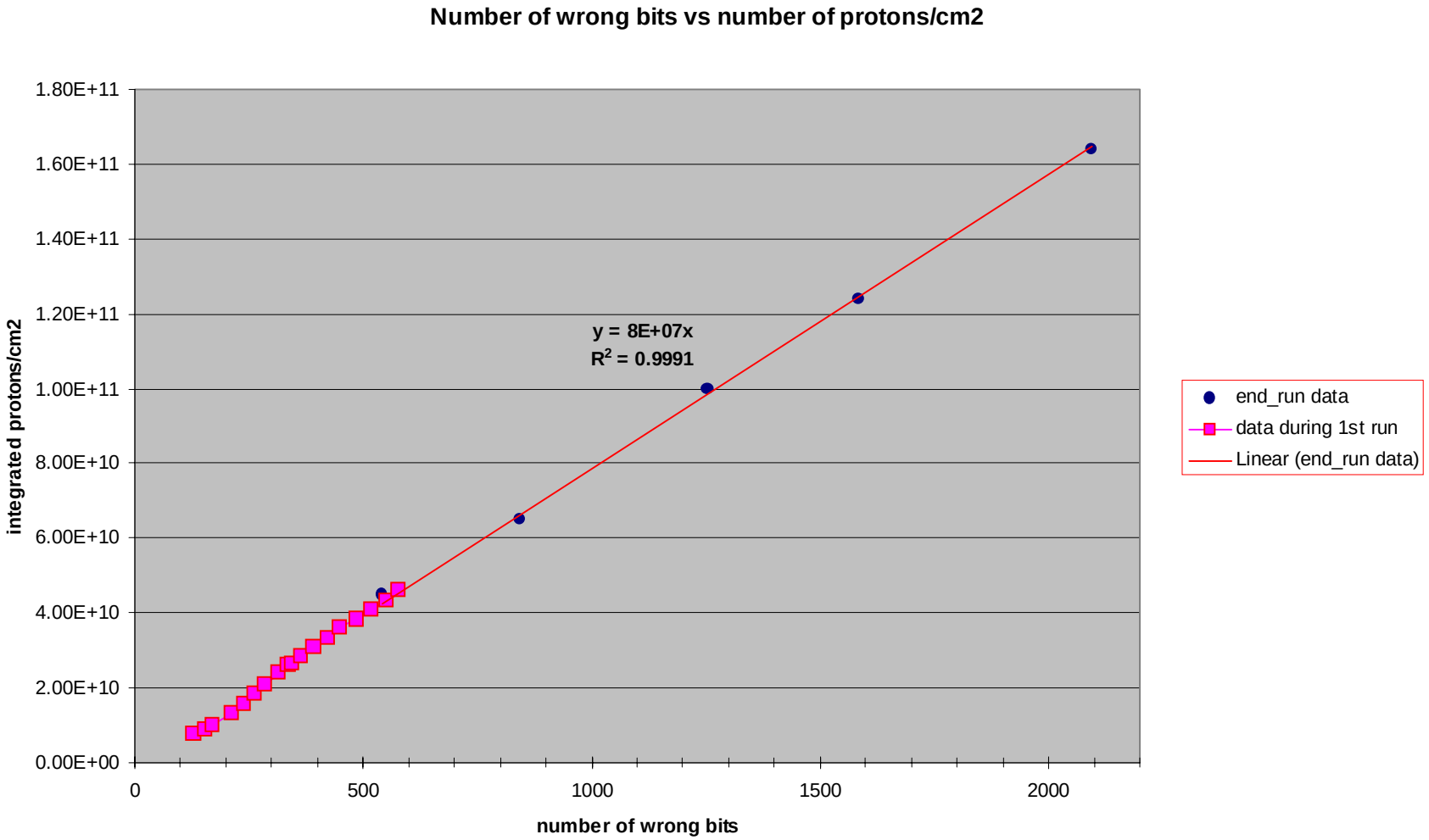
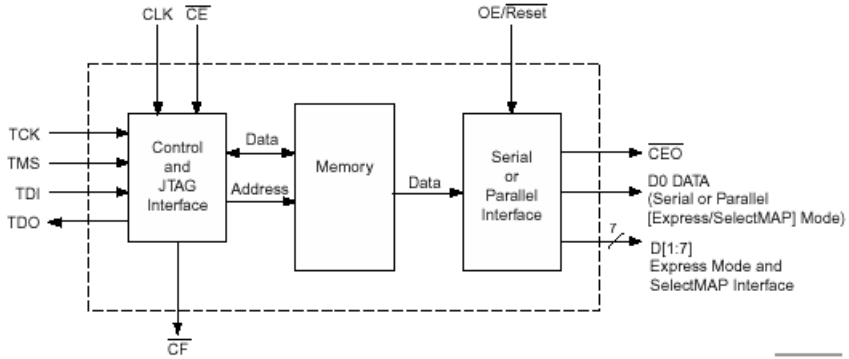
Test results from second Louvain campaign



FlashProm SEU test



Xilinx 18v02 FlashPROM:

Features

• In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
- Endurance of 10,000 program/erase cycles
- Program/erase over full commercial/industrial voltage and temperature range
• IEEE Std 1149.1 boundary-scan (JTAG) support
• Simple interface to the FPGA; could be configured to use only one user I/O pin
• Cascadable for storing longer or multiple bitstreams
• Dual configuration modes
- Serial Slow/Fast configuration (up to 33 MHz)
- Parallel (up to 264 MHz)
• Low-power advanced CMOS FLASH process
• 5V tolerant I/O pins accept 5V, 3.3V and 2.5V signals.
• 3.3V or 2.5V output capability
• Available in PC20, SO20, PC44 and VQ44 packages.
• Design support using the Xilinx Alliance and Foundation series software packages.
• JTAG command initiation of standard FPGA configuration.

After an integrated flux over 4 devices of $8*10^{11}$ protons/cm^2@ 60 Mev

We did not observe any SEU.

At about $2*10^{11}$ protons (28 Krad) the programming feature does not work .

Xsection/bit < $1.25 * 10^{-18}$ cm^2

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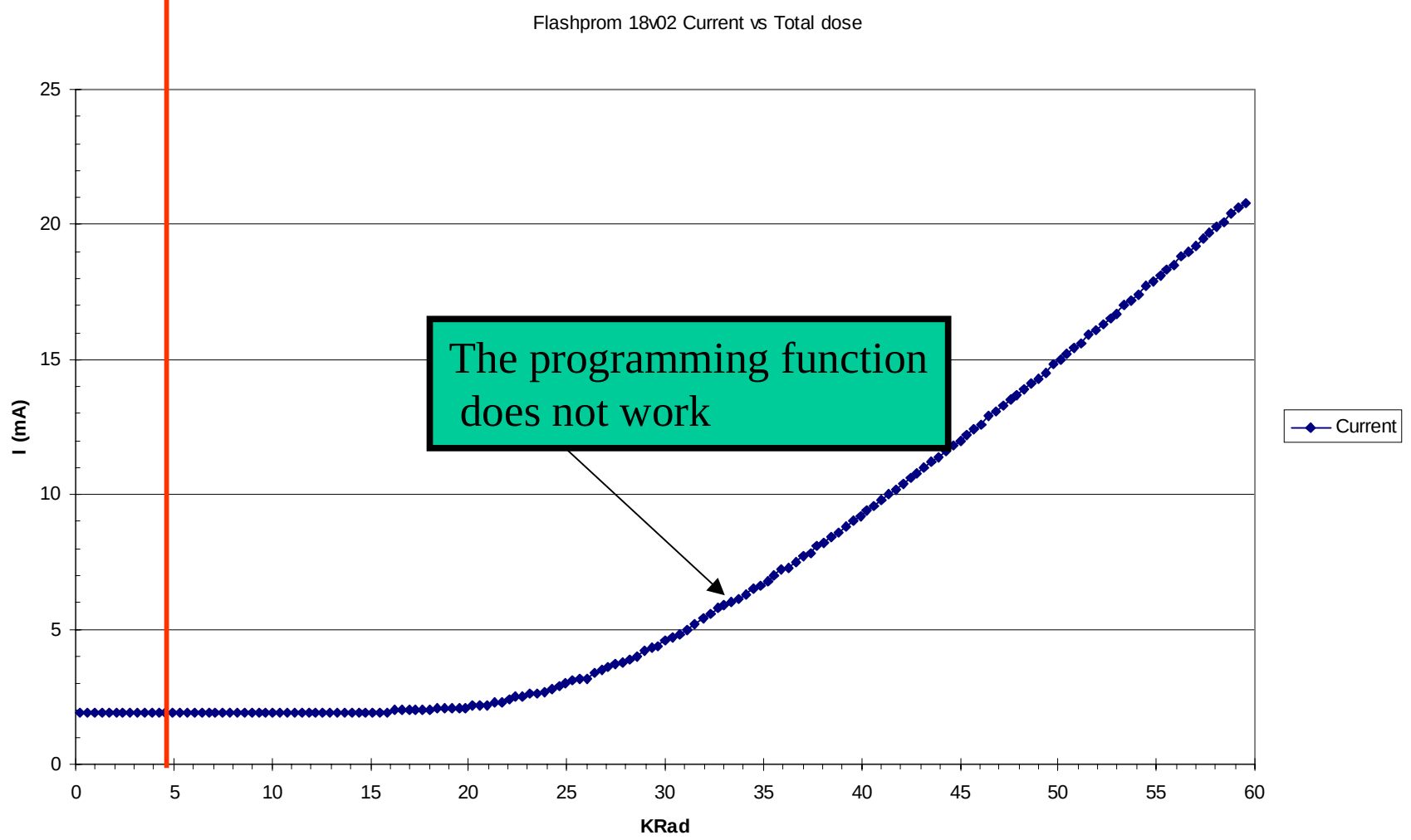
Flashprom 18V02 Co_{60} irradiation

Atlas RPC worst case total dose including safety factors
4.2Krad=302 Rad*4(SF_{sim})*3.5(SF unknown batch)



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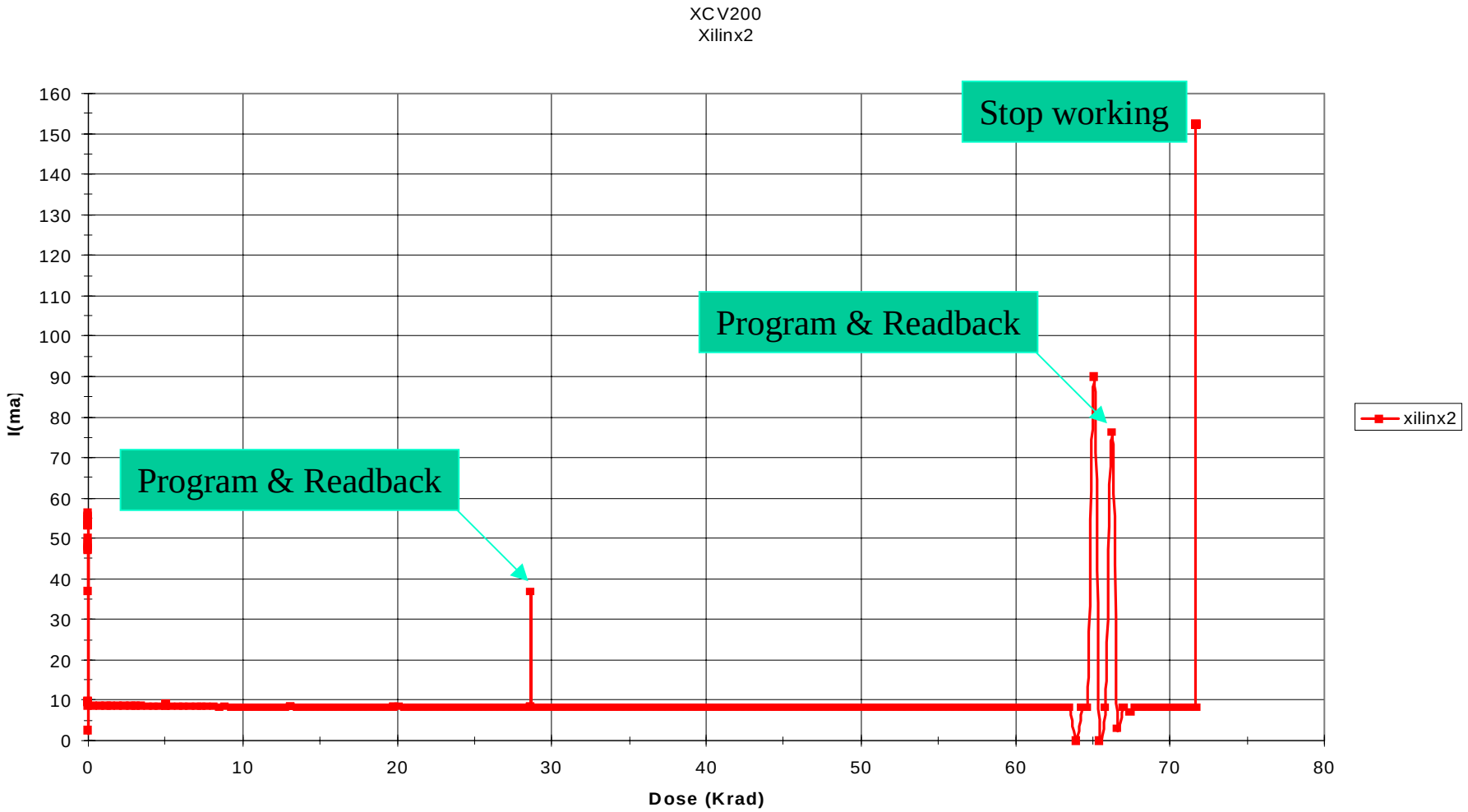
XCV200 Co_{60} irradiation



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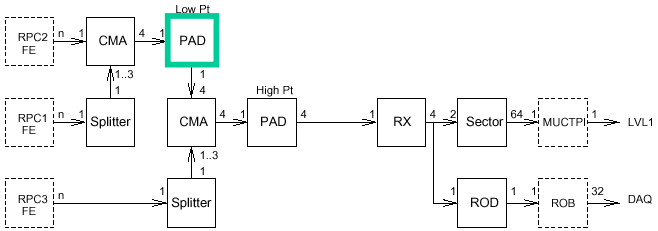
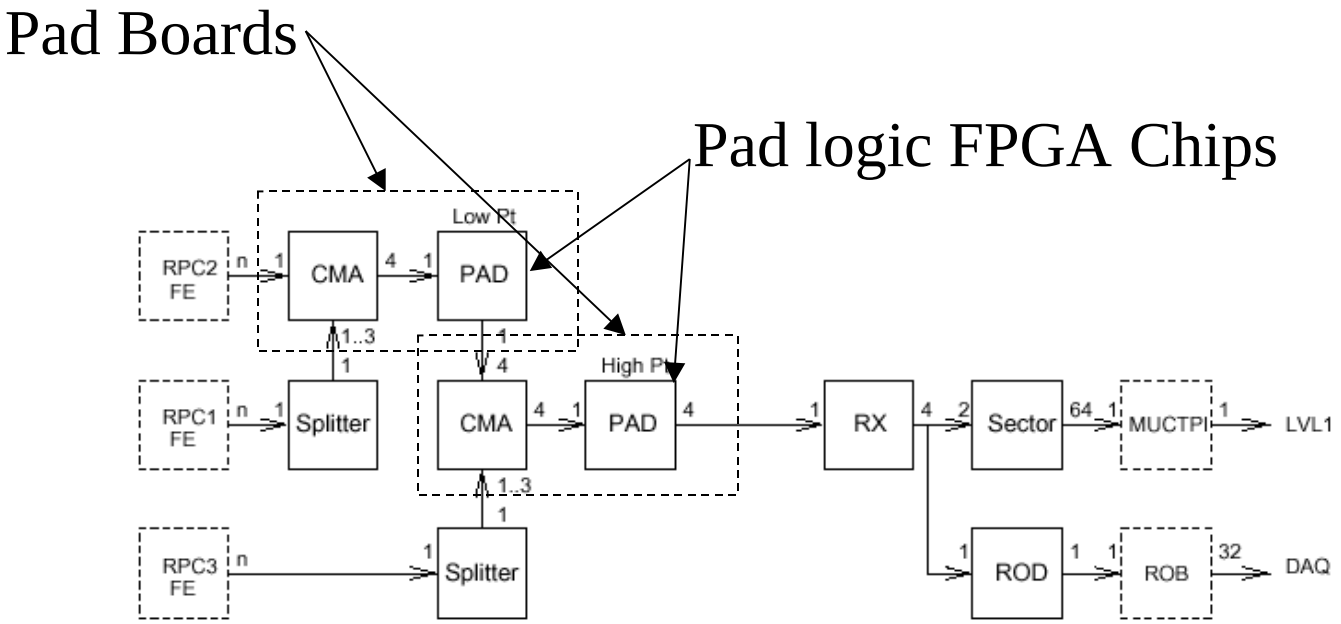
Low p_T PAD board

- Pad logic chip, which covers a region $\Delta\eta x\Delta\phi$ = 0.2x0.2, associates muon candidates with a region $\Delta\eta x\Delta\phi$=0.1x0.1 (RoI);
- It selects the higher triggered track in the Pad;
- Pad logic chip solves overlap inside the Pad;
- The information of two adjacent CMAs in the η projection, and the corresponding information of the two CMAs on the ϕ projection, are combined together in the low-p_T Pad logic board;
- The four low-p_T CM boards and the corresponding PAD logic board are mounted into a single PAD box, on the outermost side of the RPC2 detector;



Location of the XCV200 inside the LVL1 muon Trigger



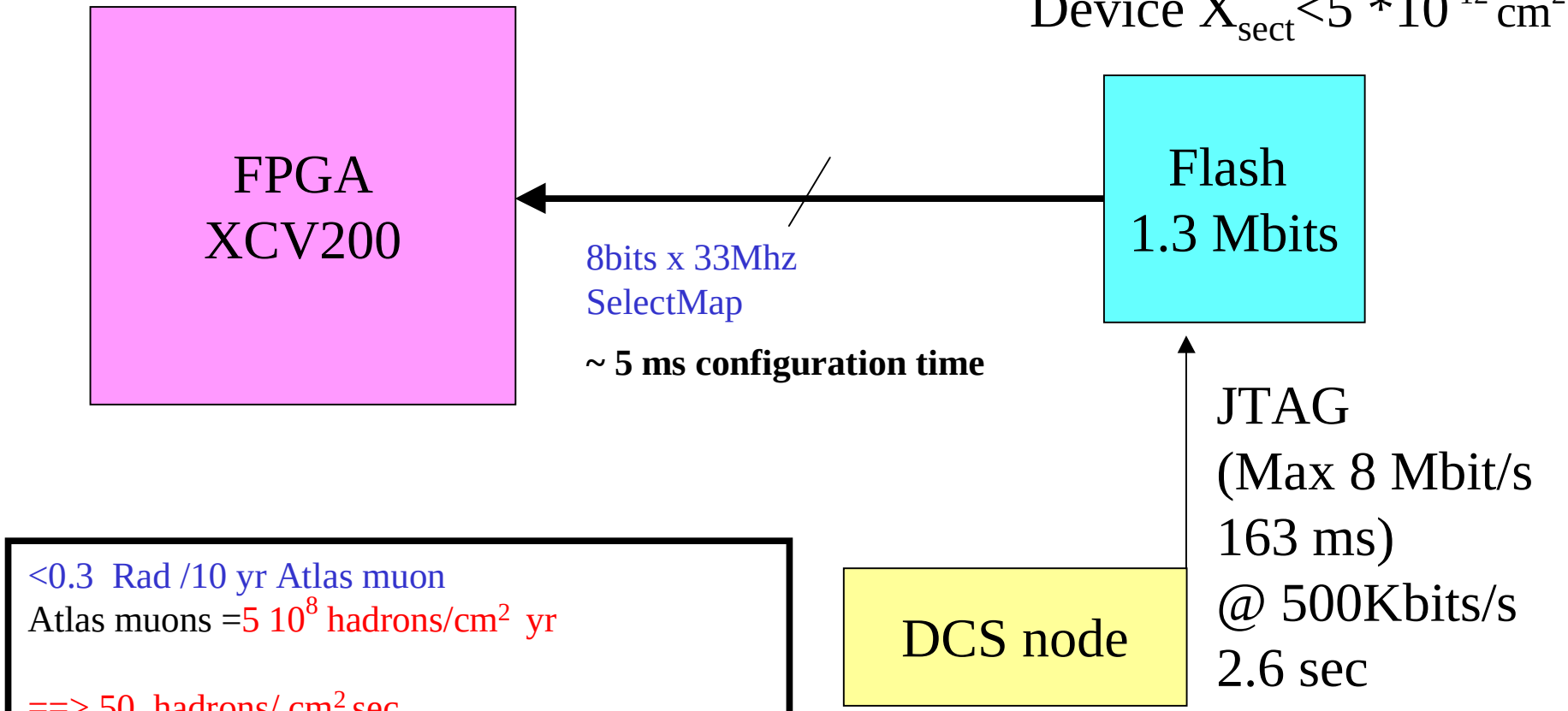
XCV200 in Atlas muon enviroment

Device $X_{sect}=1.25*10^{-8}$ cm^2

6.25 SEUs in one year

SEU with SF=6.25*5(SF_{sim})*4(SF_{lot})=125 in one year

Device $X_{sect}<5*10^{-12}$ cm^2

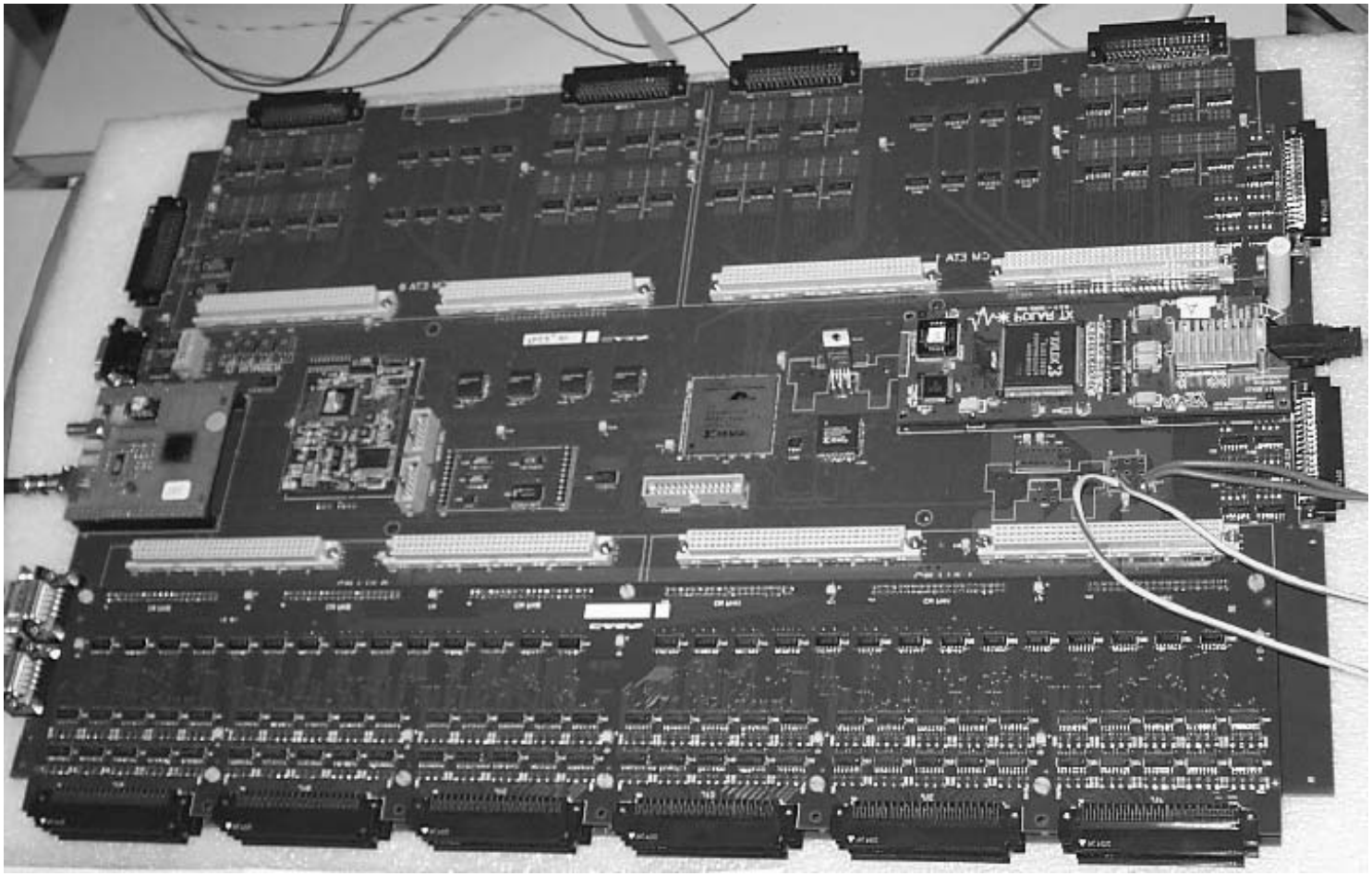


<0.3 Rad /10 yr Atlas muon

Atlas muons =5 10^8 hadrons/cm^2 yr

==> 50 hadrons/ cm^2 sec

PAD board with TTCrx ELMB XCV200 and Optical Link



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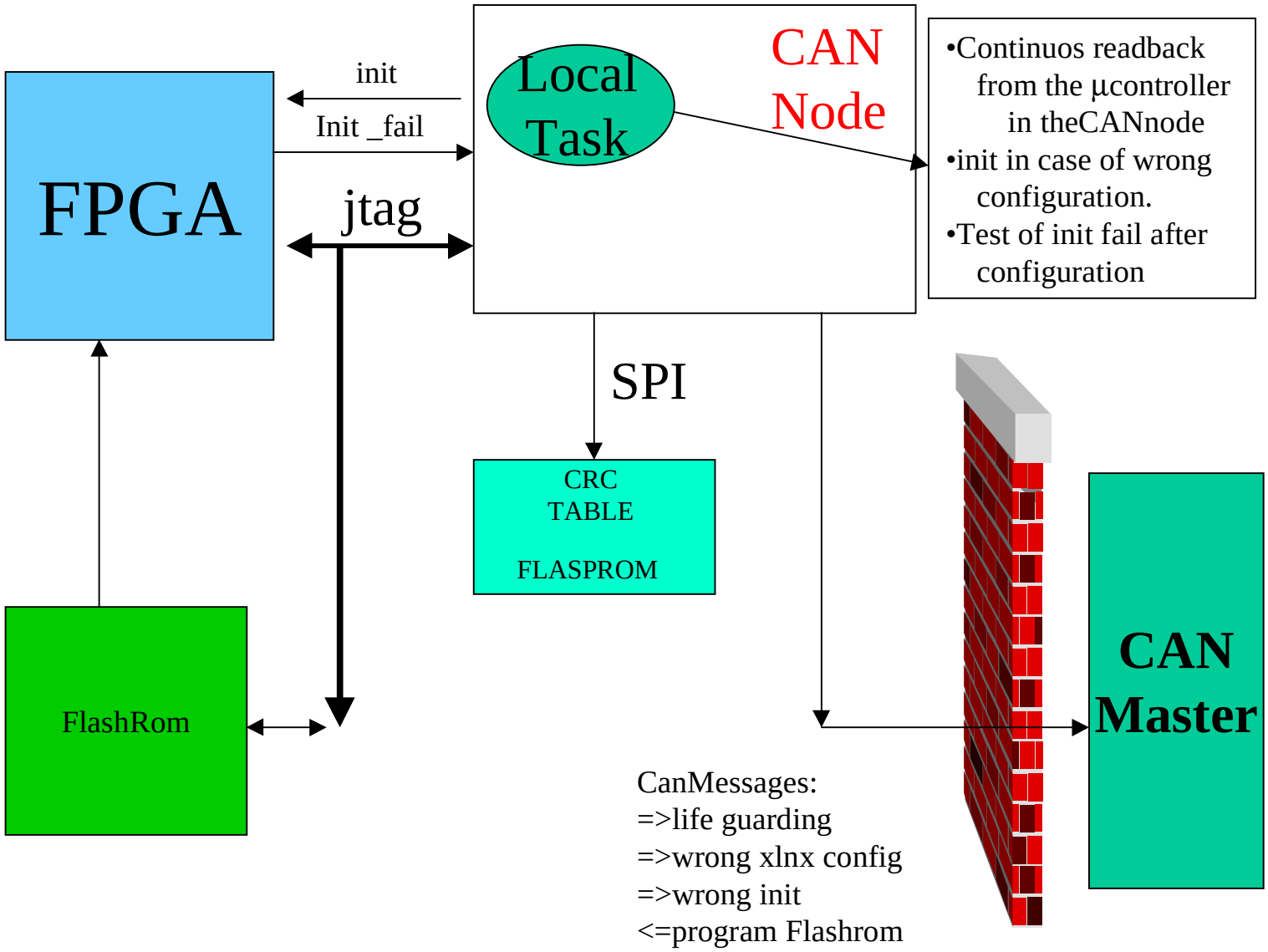
Configuration SEU recovery system



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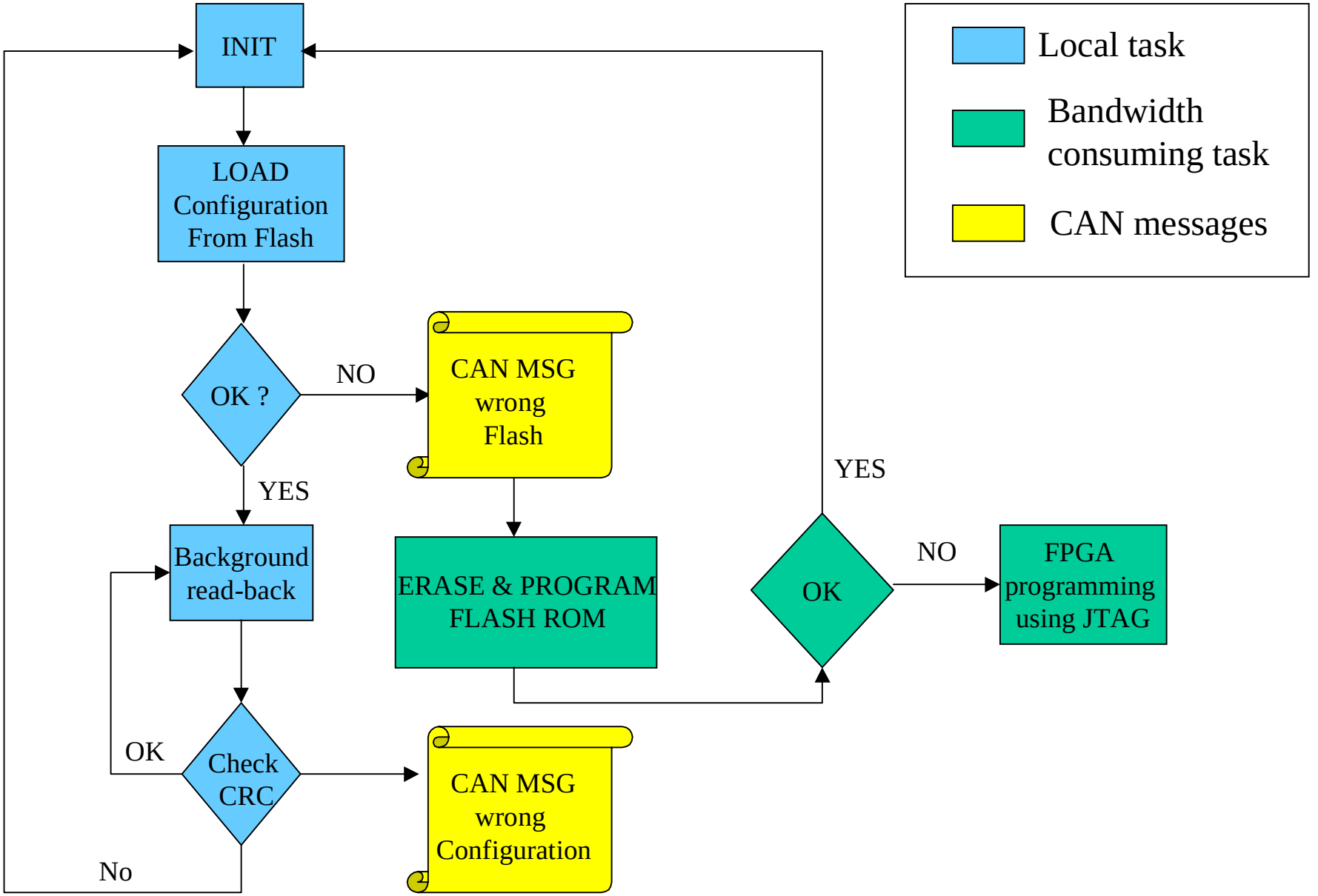
FPGA initialization



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Readback data structure

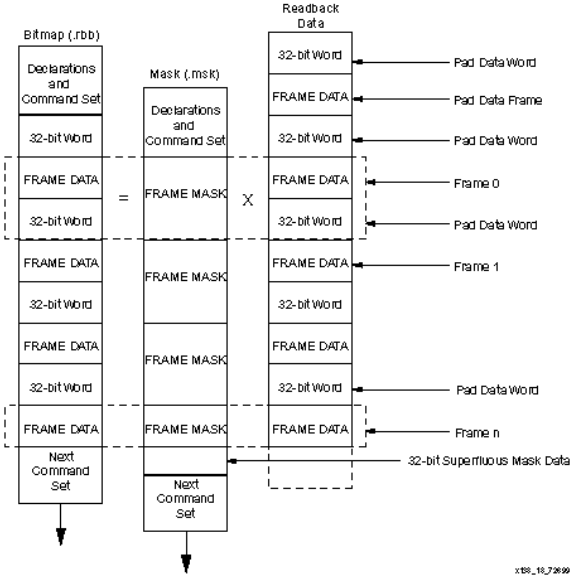


Figure 18: **Readback Data Stream Alignment**

- Readback and mask
  single frame (2186 frames in XCV200)
- CRC computation and comparison
  with the stored value in the SPI Flashrom
- Estimated time needed to check all frames
  <30 sec

Device	CL Frames	Bytes per Frame	Frame Bytes	Pad Bytes	Readback Bytes
V200	2186	68	148648	8816	157464

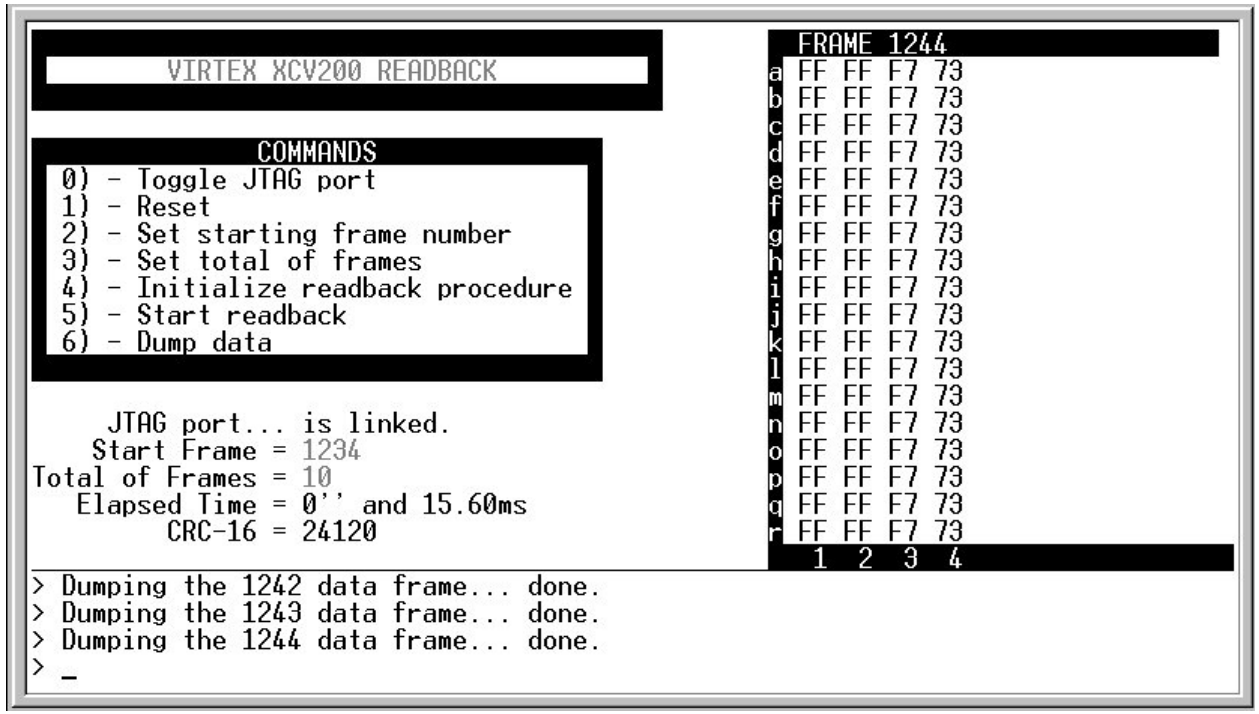
JTAG functions

FUNCTIONS
* =========
* JTAG_reset() - Resets all TAPs => TEST_LOGIC_RESET.
* JTAG_init() - hardware init of the MCU AVR.
* JTAG_countTaps() - count the length of the jtag .
*
* JTAG_ST_sendCmd() - Load the IR.
* JTAG_ST_getRegData() - Read IR.
* JTAG_ST_loadRegData() - LOAD DR.
*
* JTAG_MT_countBSRcells() - count BSR cells.
* JTAG_MT_sendCmd() - Load the IR to one or all the taps.
.
* JTAG_MT_getRegData() - Read IR from a single TAP.
.
* JTAG_MT_loadRegData() - LOAD DR of one specific TAP .
*
* JTAG_XV_sendCmd() - Load the Virtex IR.
* JTAG_XV_getIDcode() - Read the Vitex ID-CODE.

Example of Readback Code

```
/* ----- Costanti per i comandi di readback ----- */
#define XCV200_FRAME_WORD 0x00000012L /* 18 word da 32 bits */
#define ALL_XCV200_FRAMES 0x000099C6L /* 39366 word da 32 bits */
#define HEADER_TYPE_2 0x48000000L
#define WRITE_IN_FLR_REGISTER 0x30016001L
#define XCV200_FRAME_LENGTH 0x00000011L
#define WRITE_IN_FAR_REGISTER 0x30002001L
#define WRITE_IN_CMD_REGISTER 0x30008001L
#define RCFG_COMMAND 0x00000004L
#define READ_FROM_FDRO_REGISTER 0x28006000L
#define FLUSH_PIPELINE_DATA 0x00000000L

// Per il readback di tutti i CLB
#define DEFAULT_START_FRAME_ADDR 0x00000000L
#define DEFAULT_WORD_COUNT (HEADER_TYPE_2 | (XCV200_FRAME_WORD * 2))

  ULONG clb_rbackCommandSet[] = { // Buffer per i comandi di readback
  WRITE_IN_FLR_REGISTER,
  XCV200_FRAME_LENGTH,
  WRITE_IN_FAR_REGISTER,
  DEFAULT_START_FRAME_ADDR, /* index = 3 */
  WRITE_IN_CMD_REGISTER,
  RCFG_COMMAND,
  READ_FROM_FDRO_REGISTER,
  DEFAULT_WORD_COUNT, /* index = 7 */
  FLUSH_PIPELINE_DATA
  };
  // ReadBack procedure
  JTAG_XV_sendCmd( CFG_IN );
  JTAG_gotoState( SHIFT_DR );

  // -----load readback command
  JTAG_ST_loadRegData( sizeof(clb_rbackCommandSet)/sizeof(ULONG),
  clb_rbackCommandSet );
  JTAG_XV_sendCmd( CFG_OUT );
  JTAG_gotoState( SHIFT_DR );
  _pulseJtagClk();

  // Radback
  JTAG_ST_getRegData( (ALL_XCV200_FRAMES*4, NULL );
```

XFRAME program:



- Run on Atmel ATmega103 evaluation board.
- Use rs232 serial line with VT100 terminal control character.
- Give the possibility to read compute the CRC
  of single or multiple XCV200 readback frame.

Conclusions

- After the radiation test we demonstrate the feasibility of the use FPGA in our environment.

- The immunity of Flashprom technology to SEU can be used for fast reprogramming of Xilinx configuration on board.

- The availability of CPU power from DCS node can be used to continuously check the Xilinx program.

- We need to integrate the readback process inside the CAN node software