TGC DCS Progress and Plans
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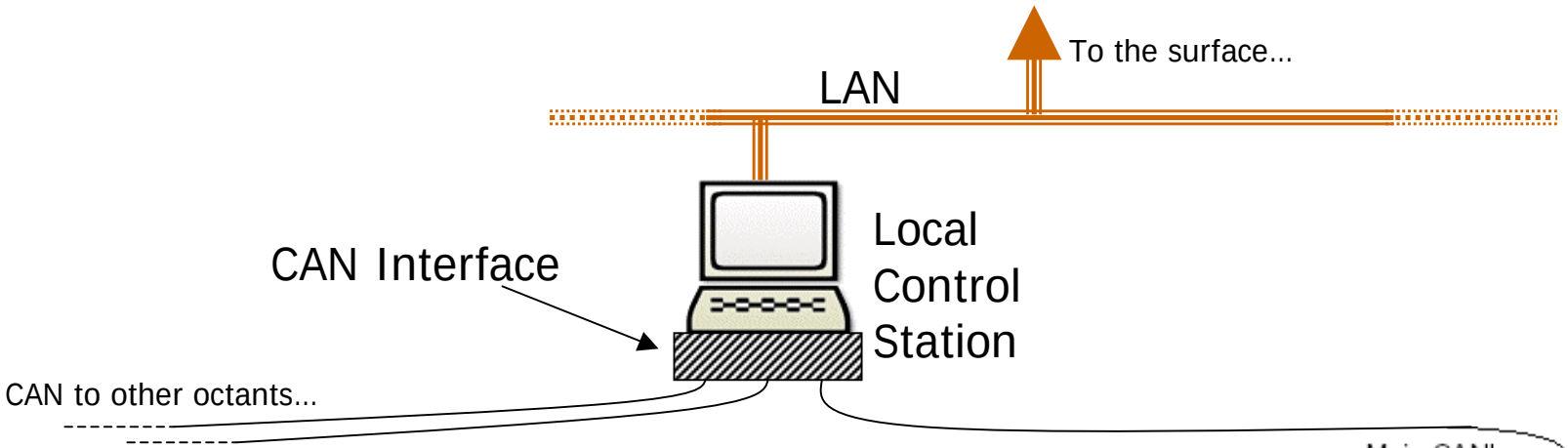
Talk Contents

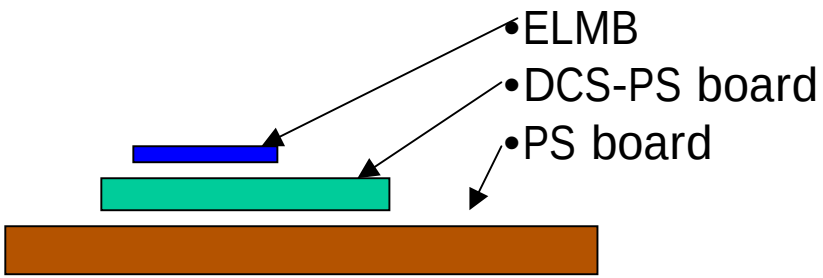
- The TGC DCS system
- Hardware (N.Lupu)
- Software
  - LCS (A. Harel)
  - ELMB (R. Lifshitz)
- Test results
- TGC electronics slice test plans
- More plans for 2002+

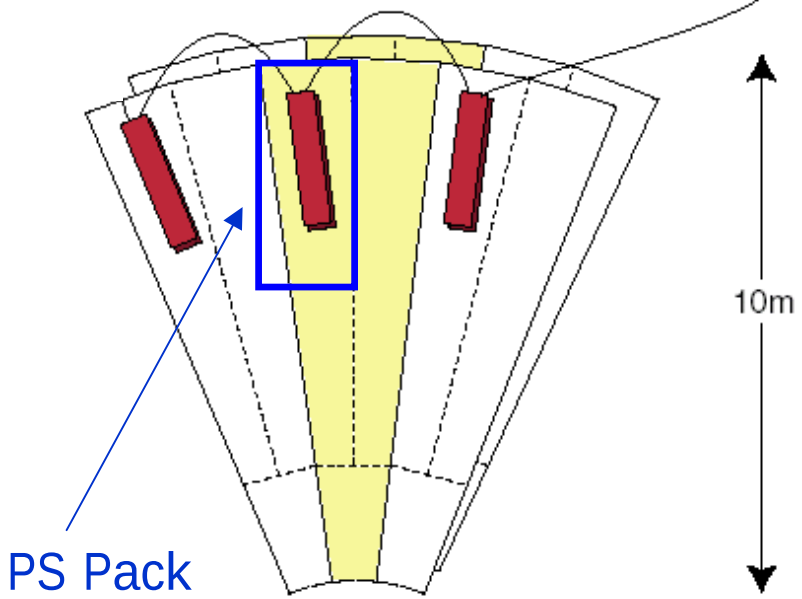
What's required from TGC DCS?

- The target of the TGC DCS is:
  - Setting, monitoring and logging parameters
    - voltages, temperatures, gas flow, alignment, etc.
    - ASIC programmable parameters
  - Implementing autonomous actions
    - integrity checks, diagnostics, chamber charge measurement
  - Triggering alarms or emergency actions
- A SCADA system, PVSS, is provided by ATLAS DCS.
- TGC DCS runs PVSS on the LCS which controls TGC and reports to ATLAS DCS.
- ELMB CANnodes are used as FE element, complemented by in-house-design electronics

Introduction to TGC DCS layout







Thin Gap Chambers

LL08V01

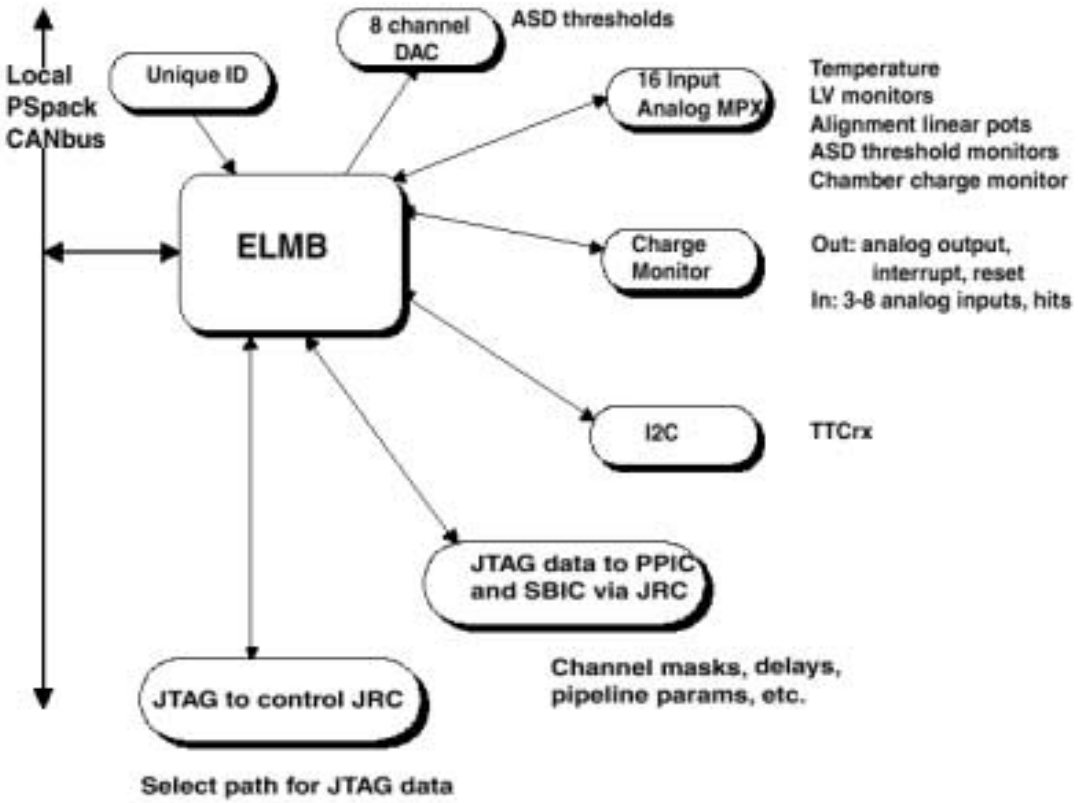
TGC DCS HW (talk by N. Lupu)

- Three DCS boards planned:
  - DCS-PS on each PS board
    - 1555 boards
    - First prototype tested
  - DCS-SPP on the service patch panel
    - 100 boards
    - Design in progress
  - DCS-HSC in the H-PT/SSW crate
    - 50 boards
    - Layout in progress

DCS CAN node: The Embedded Local Monitor Board

ELMB utilized as:

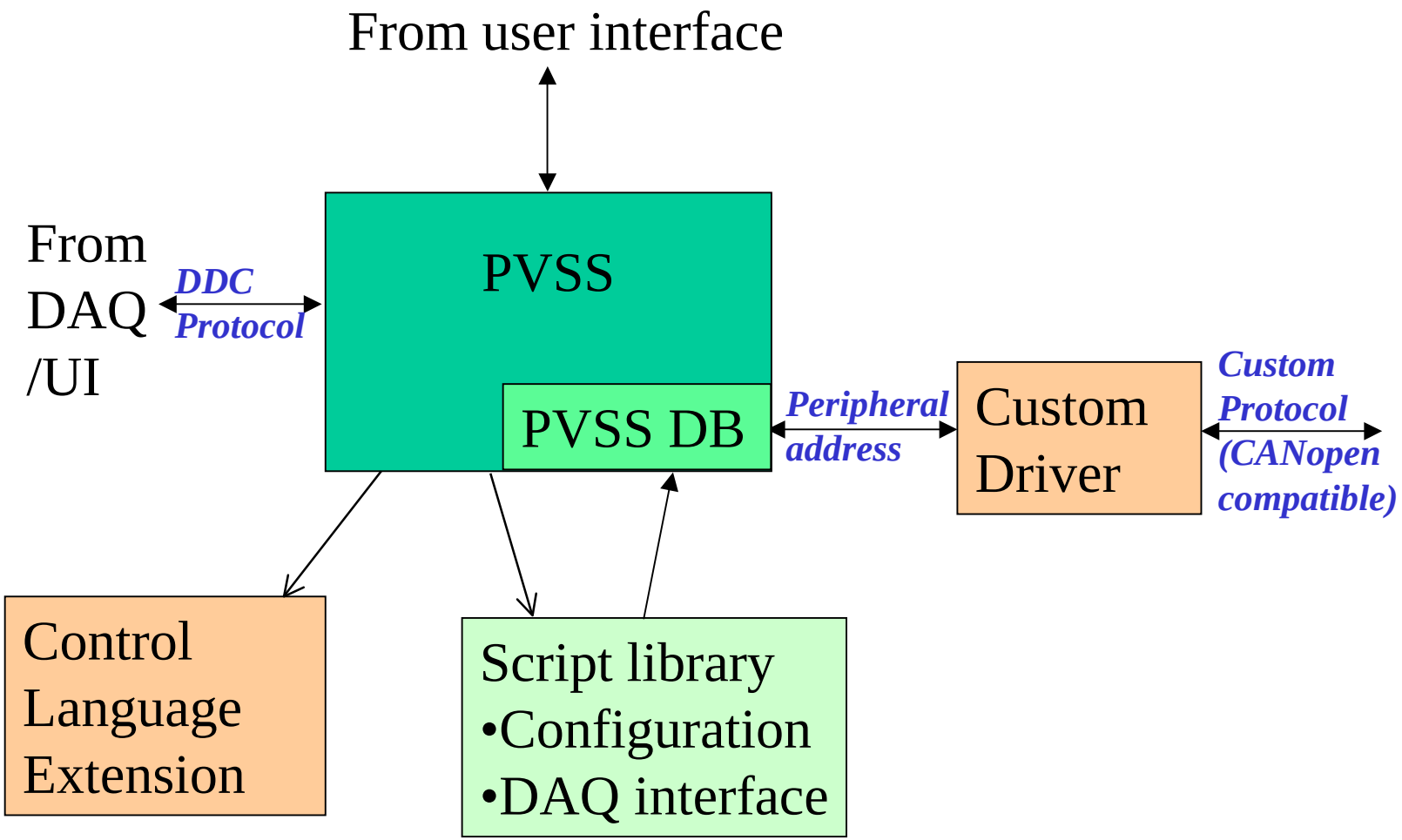
- **a simple point to point channel to sensors**
- **an intelligent control unit, capable of performing complicated tasks (minimizes load on bus).**



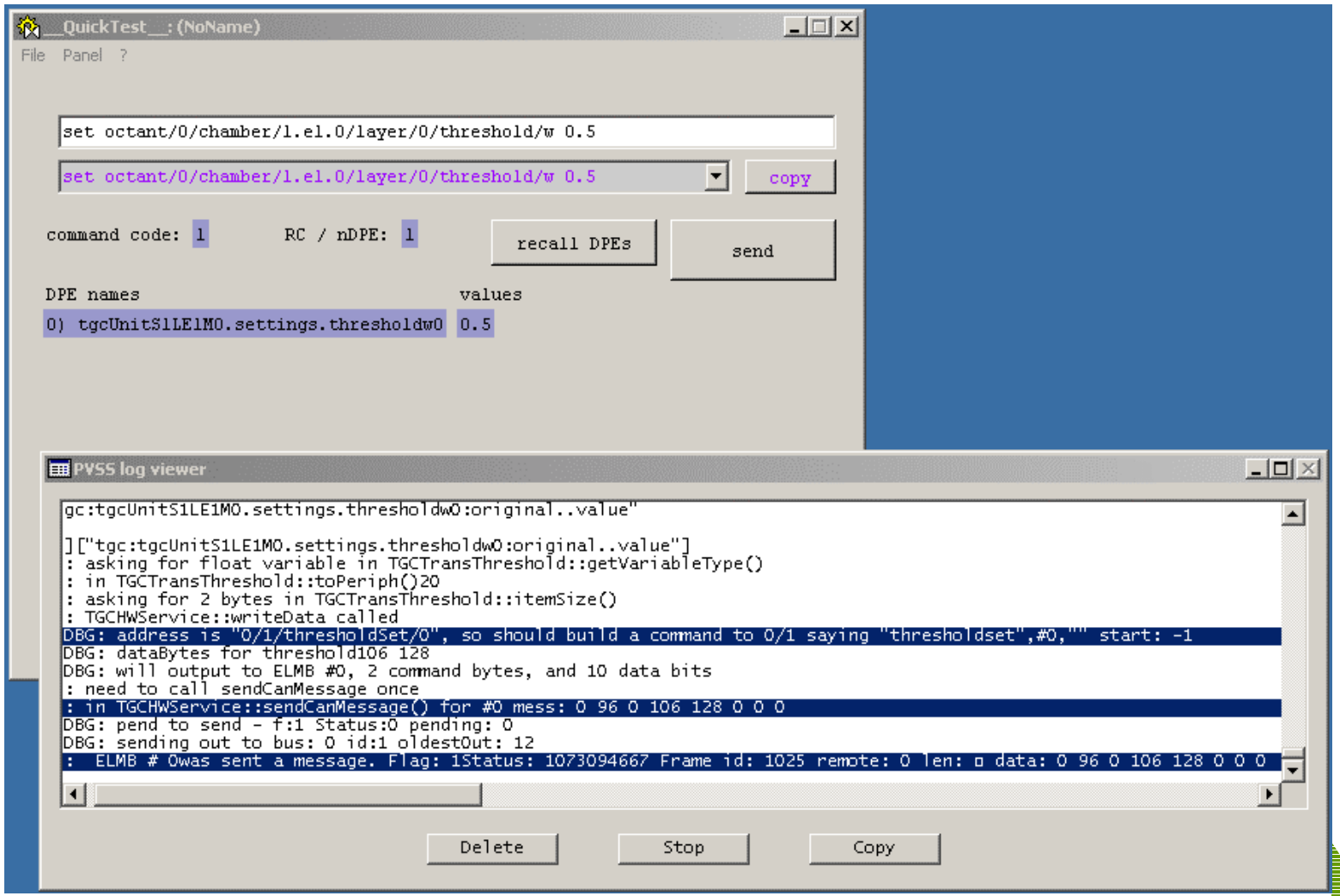
DCS Software

- The DCS software is divided into the following components:
  - The ATLAS DCS is being written using a commercial SCADA system (PVSS) using a common framework developed at CERN.
  - The TGC LCS SCADA customization will allow interaction with ATLAS as well as local needs
  - The TGC LCS will offer UI for installation, setup, calibration and diagnostics of TGC also in stand alone mode.
  - Hardware control software is resident in the CAN node ELMB that communicates with the attached hardware devices using appropriate protocols such as JTAG and I^2C.

LCS SW Overview (A.Harel)



DAQ interface

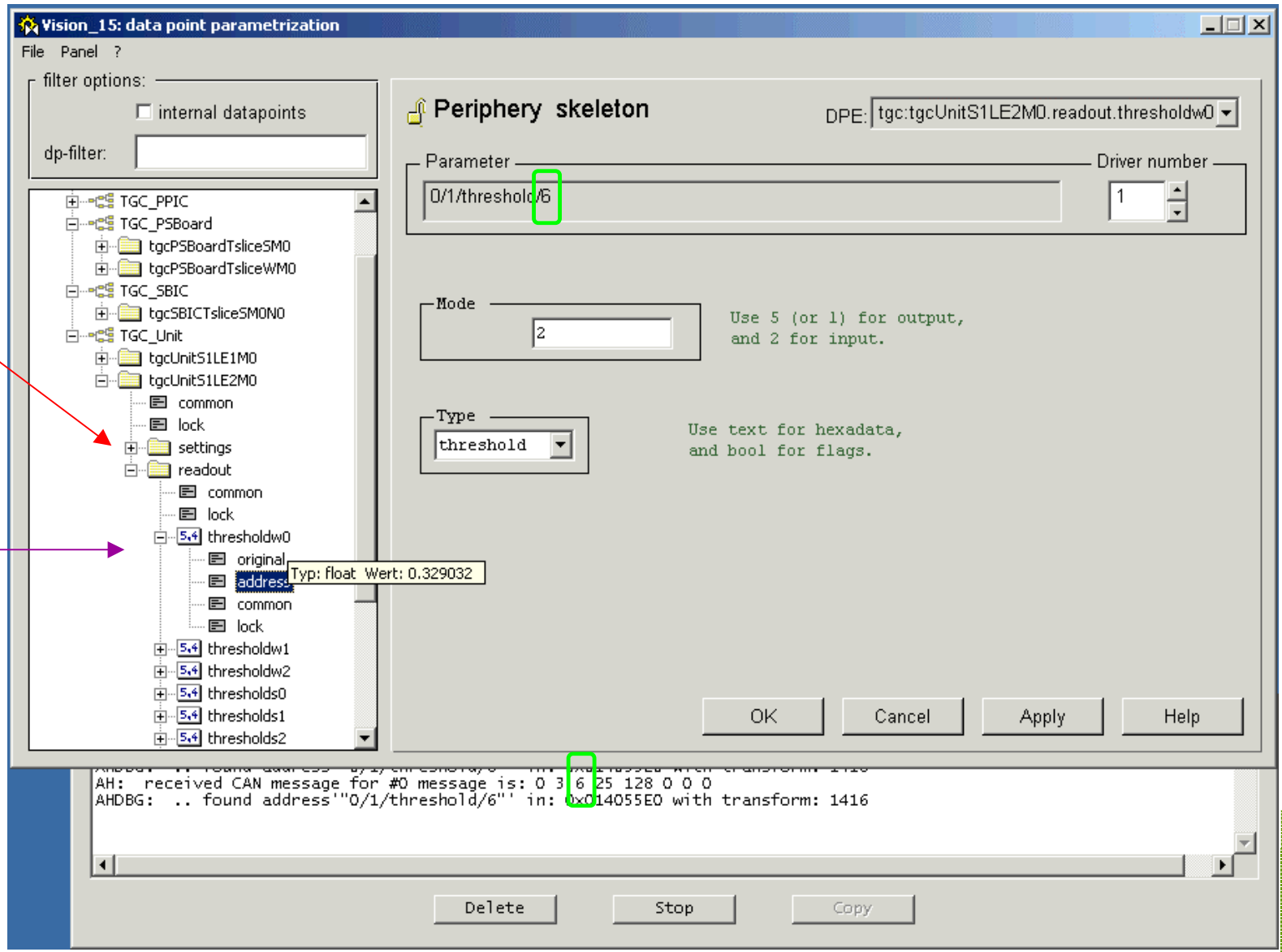


extract octant/0/Psboard/*/PPIC/*/signal_del from named configuration goodDelays20011131
read octant/0/unit/2.f.2/Alignment/1

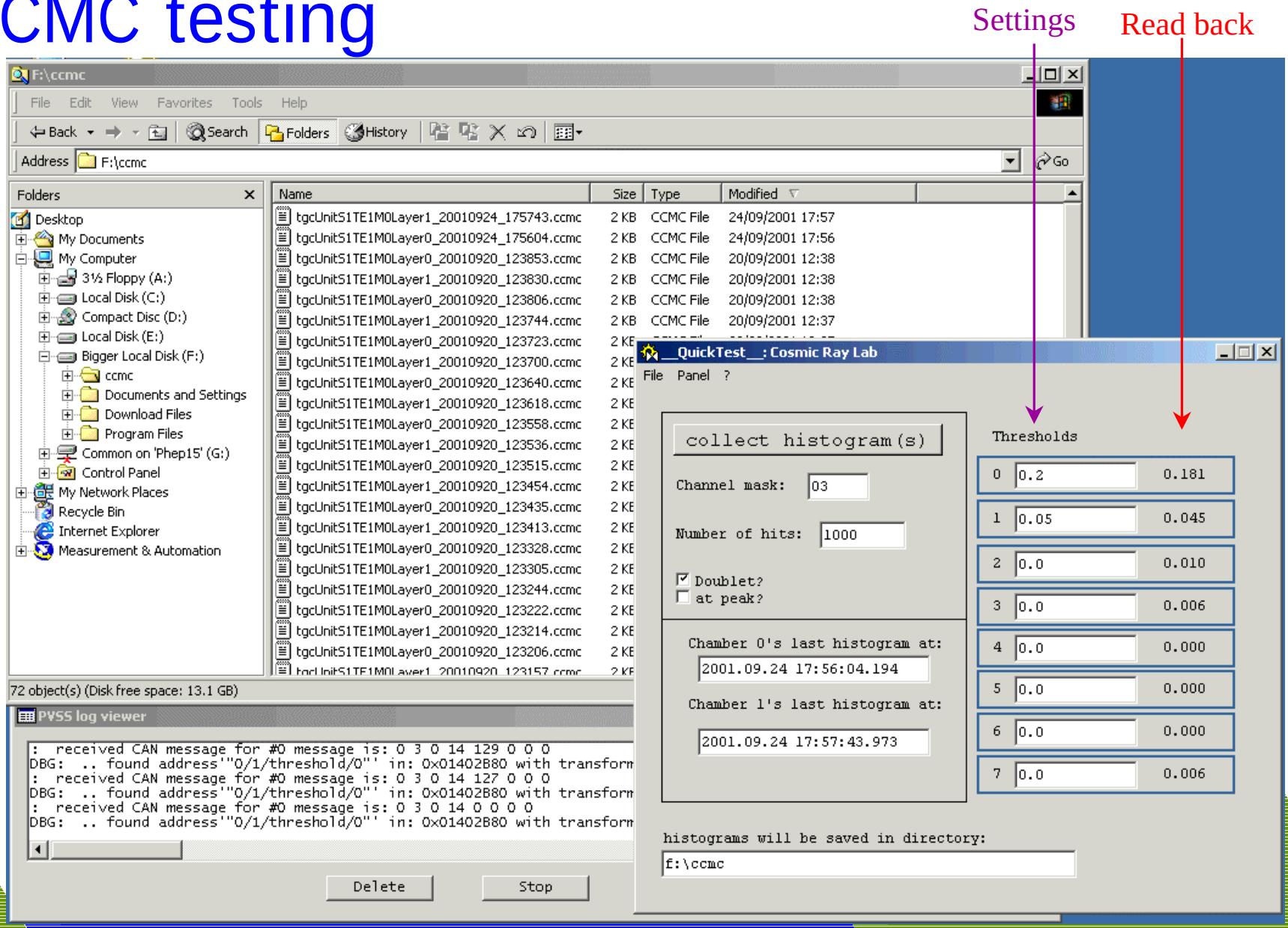
Data Points

Outgoing DPE (commands)

Incoming DPE (readout)



CCMC testing



ELMB software (talk by R.Lifshitz)

- The ELMB software will be downloaded from the LCS.
- It contains a real-time kernel that manages the bi-directional message flows
  - done by ATLAS DCS (Henk B&B).
  - Additional features by TGC DCS.
- The ELMB:
  - receives configuration, control and monitoring commands from the LCS
  - distributes the commands to the attached devices
  - assembles responses and transmits them back to LCS.
- Node program implements JTAG, simple diagnostics etc.

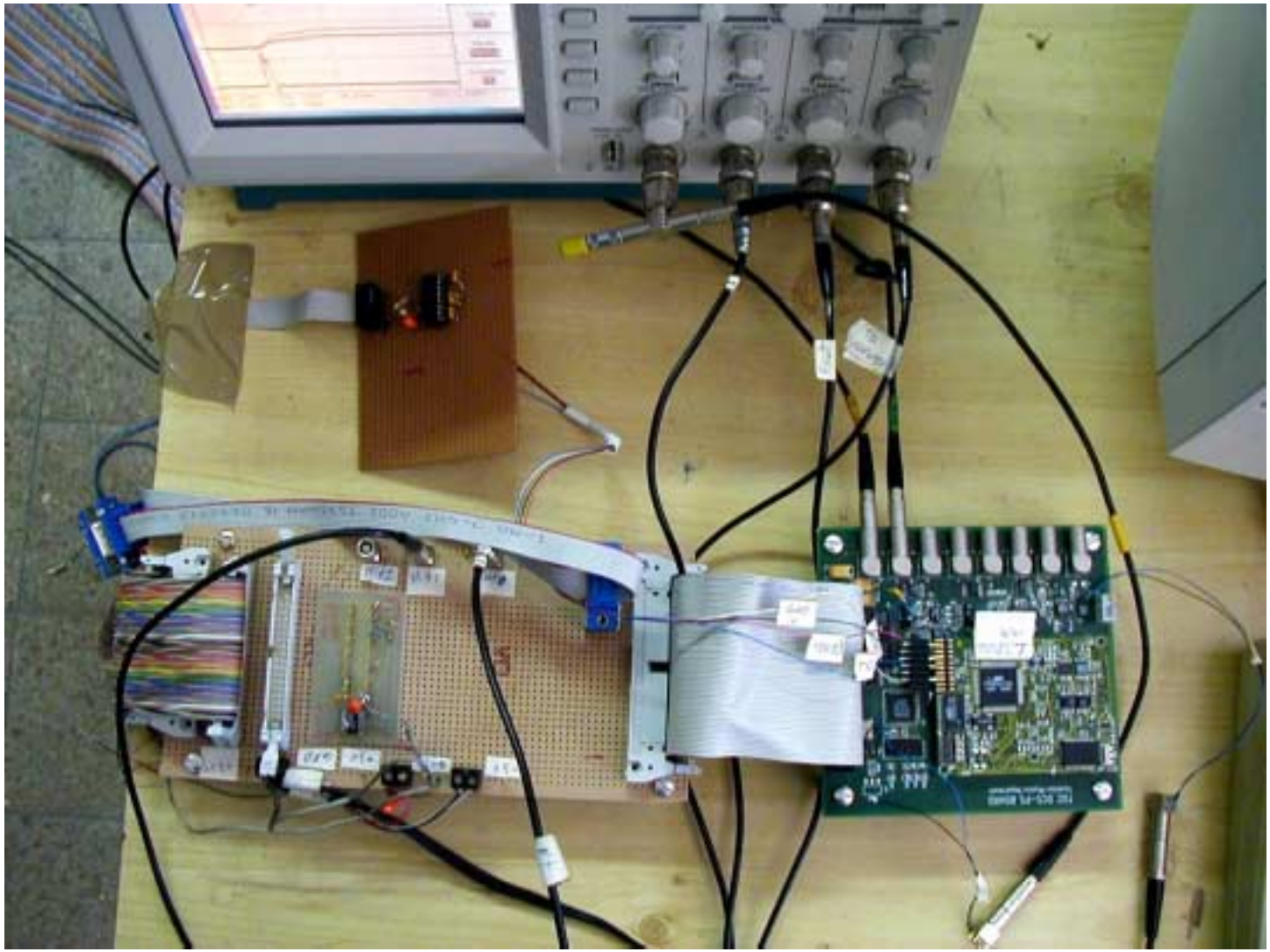
DCS Testing

- DCS-PS board prototype 0 was produced.
  - Will be mounted directly on PS board as mezzanine board
  - Serves as motherboard for ELMB
  - All functions: Charge, Temperature, Alignment, LV, Thresholds (+read back), JTAG, I2C, ID.
- Extensive testing done using this board
  - Hardware
  - ELMB SW
  - LCS SW

} integration

Setup in Test Lab

The DCS Hardware



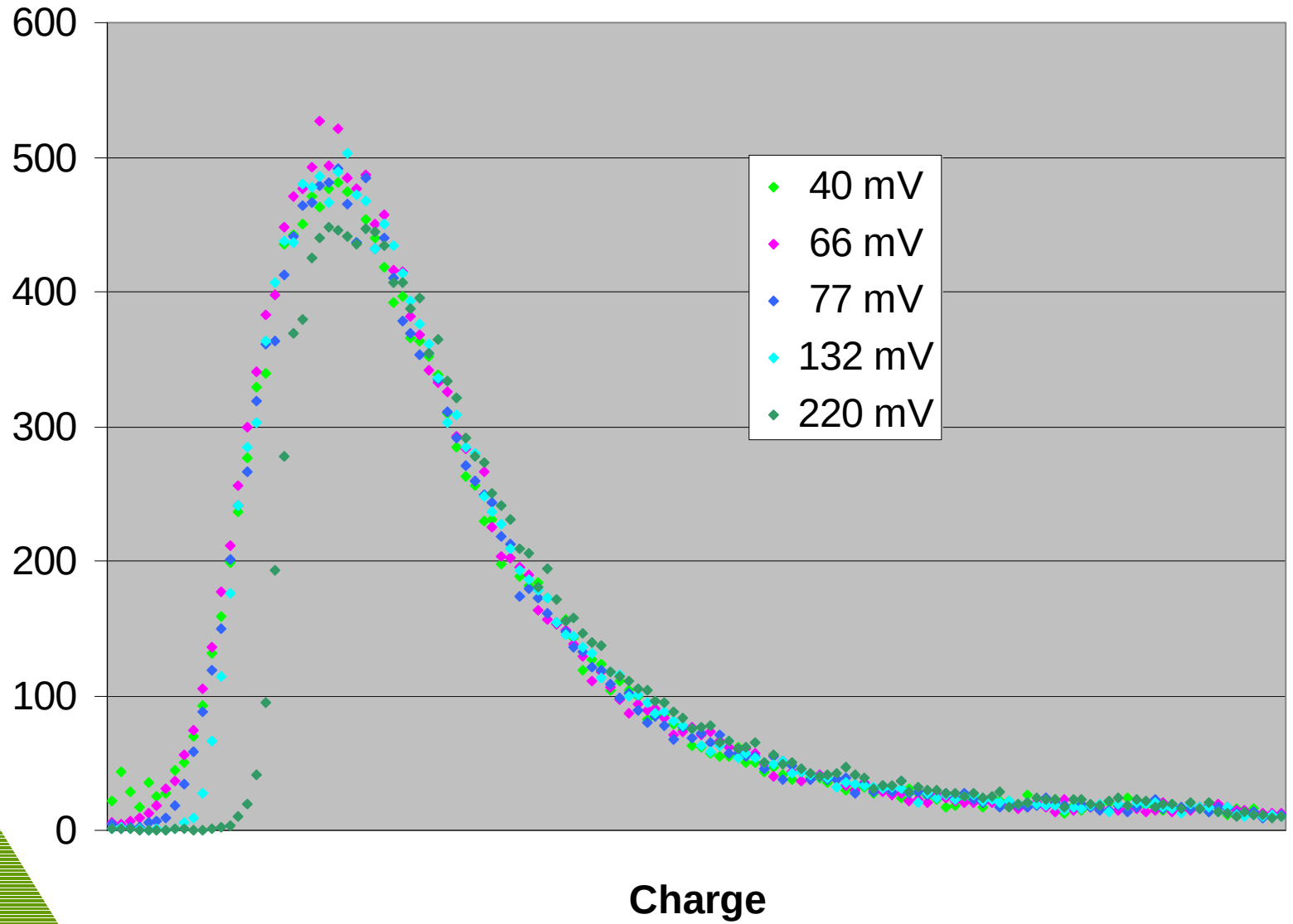
Tests (1)

- A test of reading chamber charge:
  - By LCS in response to UI commands
    - LCS parses the command and identifies ELMB and datapoint.
    - LCS sends command to ELMB
    - ELMB
      - selects specified channel – operates the CCMC
      - takes data and concentrates in histo for specified #events
      - sends the data to the LCS
    - The LCS receives the data and stores it
  - Autonomous background process by ELMB: Go around active channels
    - LCS tells ELMB which channels are active (bit mask)
    - ELMB
      - selects a channel – collects histogram with specified # events
      - sends histo to LCS – moves to next channel

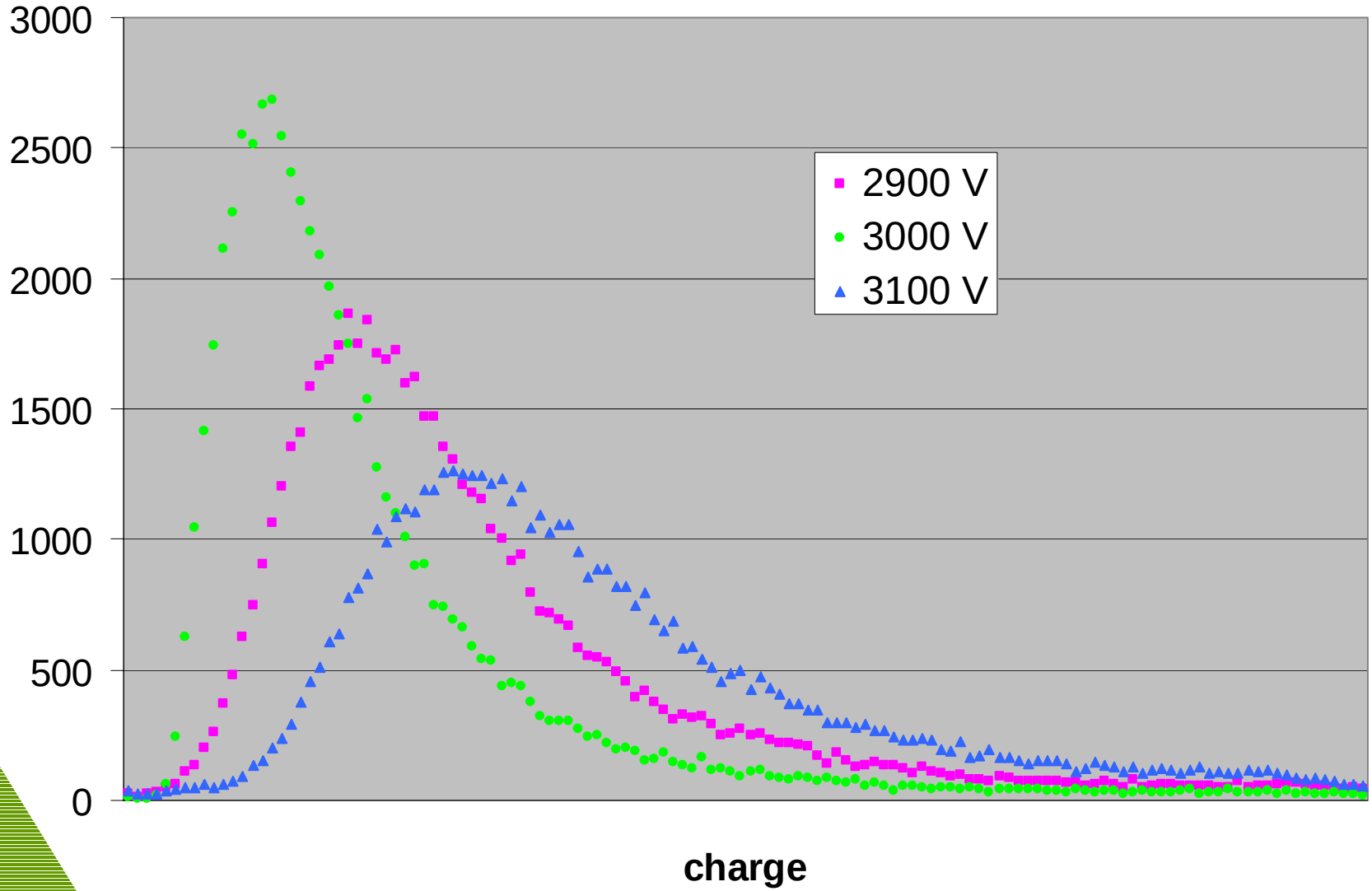
Tests (2)

- DAC and ADC operations
  - Change ASD thresholds in response to operator or DAQ commands
  - Read the threshold back
  - ELMB periodically monitors the threshold and sets it again (if not at set value)
  - Check for corresponding changes in histogram contents

TGC charge - different ASD thresholds



TGC charge - different HV



Tests (3)

- Configuration of ASICs via JTAG
  - PPIC JTAG emulation board used for testing configuration process.
  - Configuration data may come from LCS or ELMB memory
    - Configure each item (register) by downloading value/increment from LCS
    - Download a complete PPIC configuration from LCS to ELMB
    - ELMB sets a specific register in ALL PPICs in chain
  - Real PPIC, SBIC, JRC on PS board will be tested at Technion after ATLAS week.

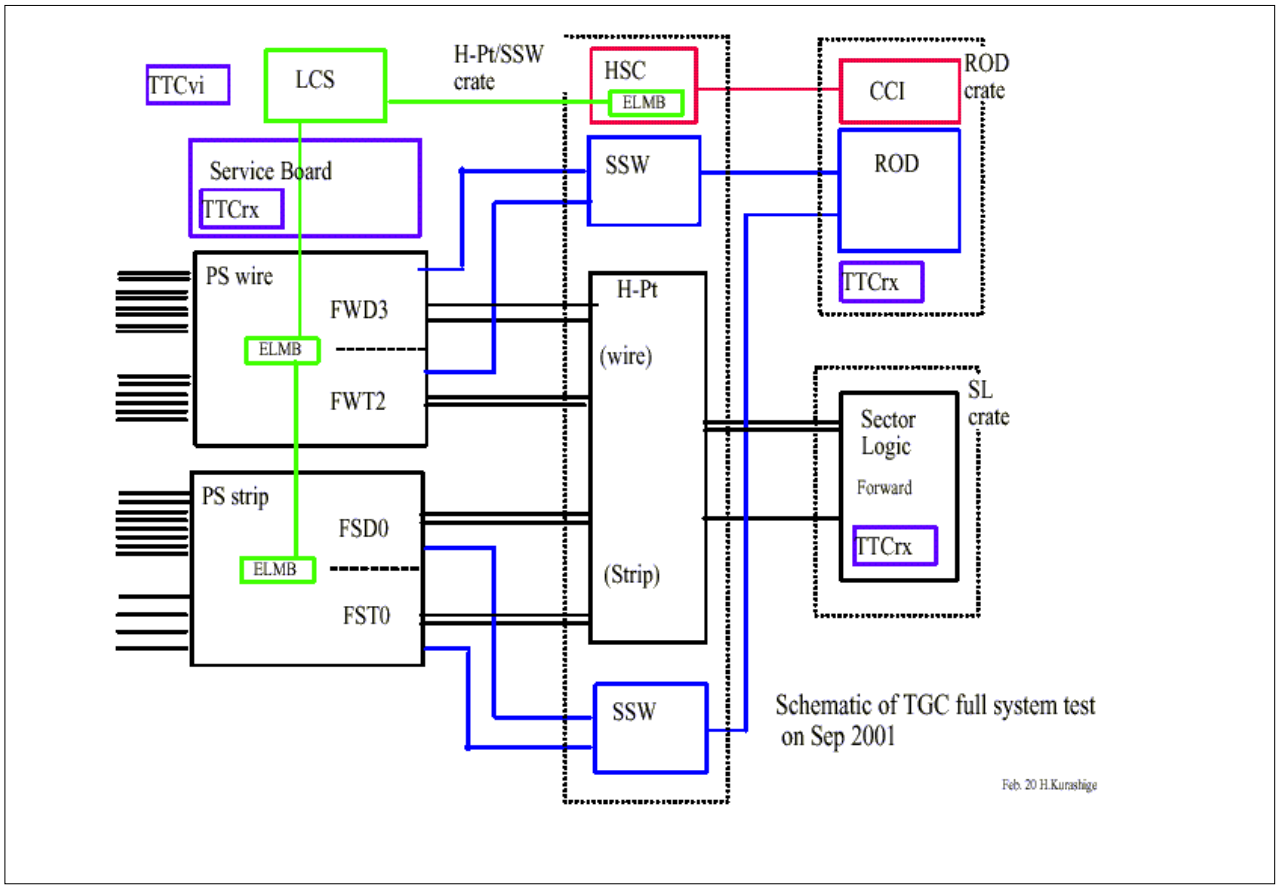
TGC Electronics Slice Test

- In Nov 2001 DCS will participate in a TGC electronics slice test in Japan.

— Trigger

— DAQ

— DCS



Tests before Japan Slice test

- Initialize the DCS Local Control Station (cold start)
- Set ASD threshold through PS board
- Monitor operating parameters (LV,Temp,Thresh)
- ROD-DCS tests
  - Start data taking
  - Configure a single ASIC parameter
  - Complete configuration of on-detector components
  - Capture snapshot of configuration from hardware

Tests planned for Japan (DCS)

- Monitor operating parameters (LV,Temp,Thresh)
- TTCrx configuration
- ROD-DCS-DAQ tests
  - Start data taking
  - Configure a single ASIC parameter
  - Complete configuration of on-detector components
  - Capture snapshot of configuration from hardware
- ROD-DCS-Trigger tests
  - Determine test-pulse delays in a PS-pack
  - Determine PPIC and Slave Board IC signal delays
  - Test a chain of components by applying test patterns to inputs and reading the response from outputs
- Detect and restore SEUs for each susceptible IC (emulation)

Single Event Upsets – ASICs

- ASICs hold 3 copies of the configuration and operate by majority.
  - The 3 copies are compared by ASIC.
  - SEU flag raised by disagreement.
  - SEU flag monitored by ELMB (JTAG)
  - ELMB reconfigures ASIC (JTAG)
  - Until reconfig – voting logic keeps operation correct

LCS keeps track of SEUs & reconfiguration events (HW failure diagnostics).
Persistently failing devices can be masked.

Calibration and diagnostics in Cavern

- Problems in TGC are detected in online histograms.
- Online monitoring identifies suspected channels and initiates action:
  - ASD Threshold verification (read back and compare)
  - Calibrate threshold:
    - Take relevant part out of ATLAS global running
    - Step though threshold voltage range and accumulate test trigger data
    - Set new threshold
  - Read back and verify PPIC and SLBIC configuration values.

Diagnose failing channels

- Suspected ASICs found by online histograms & DCS monitoring
- ROD indicates what test patterns to run and on what channels:
- Inject test patterns to suspected ASIC (JTAG).
- Test patterns can be:
  - all input combinations in few channels centered on suspected channel (ELMB).
  - known pseudo random patterns (ELMB)
  - deterministic patterns: walking 1 and 0, etc (ELMB)
  - specific pattern specified by ROD (or any other agent)
- Test scripts can also be performed periodically

More Plans for 2002

- Test the implementation of CANbus as PS board traces in first ¼ of 2002
- Test repeater (can ELMB be used?) in first ¼ of 2002
- Test redundancy scheme in first ¼ of 2002
- Radiation testing of DCS boards in first ½ of 2002
- Work on control of HV, LV, Gas system from 2002
- Test beam at H8 from second ½ of 2002 till ATLAS turn on

Conclusions

- TGC DCS is complex, requiring several experts for the different activities
- We have a team in place to design and implement TGC DCS
- We have a first prototype of each component of the DCS
- There is much more work ahead