Vivado hardware manager

mini how-to guide

Version 3.0 11-03-2016 prepared by Andrea Borga

1 Starting the hardware server

In the Atlas playground the Xilinx hardware server (hw_server) runs on **rother.nikhef.nl**. The hardware server is used to program the Xilinx FPGAs attached to it, through either the programming cables (Digilent naked or rubber) or the on-board Digilent programmer (on eval kits).

Here is the procedure to start the server, normal users have the rights to do it:

```
$ ssh rother.nikhef.nl
$ source /project/et/fpga/Xilinx/Vivado/2015.4/settings64.sh
$ cd /project/et/fpga/Xilinx/Vivado/2015.4/bin/
$ ./hw_server -d
```

Here is the procedure to kill the server, required when the client becomes irresposive (it happens...):

```
$ ssh rother.nikhef.nl
$ killall hw_server
or
$ ps -A |grep hw_server
$ kill -9 proc_id
or sudo the command if the process is not yours
```

Here is the procedure to <u>re-start</u> the server, after a crash:

```
$ ssh rother.nikhef.nl
$ source /project/et/fpga/Xilinx/Vivado/2015.4/settings64.sh
$ cd /project/et/fpga/Xilinx/Vivado/2015.4/bin/
$ ./hw_server -d -stcp::3121
```

If the server crashed it normally doesn't want to restart on the same TCP port: use ports 3121 (default), or 3122, 3123. One it crashed on one port and restarted on another, the next restart can be done on the previous port again.

Here is the procedure to <u>hard-restart</u> the server:

```
$ ssh rother.nikhef.nl
$ sudo shutdown -r now
wait for reboot
$ ssh rother.nikhef.nl
$ source /project/et/fpga/Xilinx/Vivado/2015.4/settings64.sh
$ cd /project/et/fpga/Xilinx/Vivado/2015.4/bin/
$ ./hw_server -d
```

2 Connecting to the hardware server

The hardware server can be accessed to program the cards or monitor their activity with chipscope.

2.1.1 Launch vivado

From any host with access to the */project* directory:

```
$ ssh -Y hostname.nikhef.nl
or use x2goclient or VNC
$ source /project/et/fpga/Xilinx/Vivado/2015.4/settings64.sh
$ vivado &
```

2.1.2 Open the Hardware Manager

Open Hardware Manager
🗴 🖨 🗉 Vivado 2014.4
<u>F</u> ile <u>E</u> dit F <u>l</u> ow <u>T</u> ools <u>W</u> indow La <u>v</u> out <u>V</u> iew <u>H</u> elp
🟄 🖻 🛤 🛤 🐂 🐂 🗙 🚳 🖭 Default Layout 💿 🗶 🗞 🎉
Hardware Manager - unconnected
No hardware target is open. Open target
Hardware _ ロピン Debug Probes _ ロピン
Name
Open New Hardware Target Hardware Server Settings Select local or remote hardware server, then configure the host name and port settings. Use Local server if the target is attached to the local machine; otherwise, use Remote server.
· · · · · · · · · · · · · · · · · · ·
Connect to: Remote server (target is on remote machine) 💌
Remote Server
Host name: rother.nikhef.nl
Port: 31.21 Idefault is 31.21
or 3122, 3123
Click Next to launch and/or connect to the hw_server (port 3121) application on the remote machine 'turano.nikhef.nl'.
< Back Next > Finish Cancel

2.1.3 Select the target FPGA

🛛 🛛 Open New	Hardware	Target					
Select Hardwa Select a hard frequency. If y	re Target ware target you do not s	from the list of available ee the expected device	e targets, the es, decrease ti	n set the appro ne frequency o	opriate JTAG (ir select a diff	clock (TCK) erent target	
Hardware Target Type i xilinx_tcf xilinx_tcf	s Port	Name Digilent/210249854652 Digilent/210203826227;	11AG 100000 A 150000	 HTG-71 Clock Frequence OO OO VC709 	LO cy		
Hardware Device Name ♥ xc7vx690t_0 3	s (for unkno ID Code 33691093	wn devices, specify the IR Length 6	Instruction Re	egister (IR) lenç	gth)		
Hardware server:	turan o .nik	hef.nl:3121					
			(< <u>B</u> ack	<u>N</u> ext >	<u>F</u> inish	Cancel

3 Load firmware to the FPGA

Hardware Manager - turano.nikhef.nl/xilinx_t	cf/Digilent/2102498546	52
Hardware	_ □ ₽ ×	Deb
오 🔀 😂 🔳 🕨 🕨 🗖		٩ ۽
Name	Status	
ዋ 🚦 turano.nikhef.nl (2)	Connected	
∳- ø/ xilinx_tcf/Digilent/210249854652 (1)	Open	
• • • • • • • • • • • • •	Programmed	
- 📴 XADC (System Monitor)		
- 霾 hw_vio_1 (∨IO)	OK - Outputs Reset	
└፼ hw_ila_1 (ILA)	🔾 Idle	
└ छ ♂ xilinx_tcf/Digilent/210203826227A (0)	Closed	

Click on the device you want to program

Hardware Device Pr	operties _ D Z ×
← → 🗞 📐	
<pre> % xc7vx690t_0 </pre>	
Name:	xc7vx690t_0
Part:	xc7vx690t
ID code:	33691093
IR length:	⁶ path to test bitfiles
Status:	Programmed Patil to test Ditilies
Programming file:	/project/et/Atlas/Atlas_DAQ/Felix/Firmware/test_bitfiles/pcie_dma_tor_HTG_50428_11_02.bit
Probes file:	/project/et/Atlas/Atlas_DAQ/Felix/Firmware/test_bitfiles/p_bie_dma_tog_HTG_ebug_nets_150428_11_02.ltx
User char count: N General Propert	o need to set probes if ot debugging logic eave blank) Files name help identify the card they had been build for

Hardware Manager - turano.nikhef.nl/xilinx_tcf/Digilent/210249854652				
Hardware	_ 🗆 🖻 ×	Deb		
🔍 🔀 😂 📕 🕨 🕨 🔳		۹.		
Name	Status			
🗣 🚦 turano.nikhef.nl (2)	Connected			
• Image: Provide the second state of the	Open			
• • • • • • • • • • • • •	Programmed			
- \overline a XADC (System Monitor)				
—i hw_vio_1 (∨IO)	OK - Outputs Reset			
–iia_1 (ILA)	O Idle			
└ I ⊘ xilinx_tcf/Digilent/210203826227A (0)	Closed			

right-click the device and click "program device"

🚳 Hardware Device Properties	Ctrl+E
💸 Program Device	
▶ Run Trigger	
🕪 Run Trigger Immediate	
📕 Stop Trigger	
Enable Auto Re-trigger	
Disable Auto Re-trigger	
🚳 Open Hardware Dashboard	
🥏 Refresh Device	
🥮 Add Configuration Memory Device	
Boot from Configuration Memory Devi	ce
Program BBR Key	
Clear BBR Key	
Program eFUSE Registers	
Export to Spreadsheet	

NOTE: remember to reboot the machine after every FPGA reprogram!

4 Program the Flash EEPROM

4.1.1 Create a PROM .mcs file

From the Tcl console in vivado run the command below

Tcl	Console			
\mathbf{Z}	Format	MCS		
	Size	128M		
-	Start Address	0x00000000		
	End Address	0x07FFFFFF		
đ	Addrl Add	r2 Date		
	00000000 013	C646B Jul 30		
×	⊖write_cfgmem: T:	ime (s): cpu =		
	4			
	write_cfgmem -forc	e -format MCS -		
🔚 Tcl Console 💭 Messages 🔊 S				

\$ cd /path_to_bitfile

\$ write_cfgmem -force -format MCS -size 128 -interface BPIx16 -loadbit "up 0x000000000 your_bitfile_name.bit" your_promfile_name.mcs 4.1.2 Add Configuration Memory Device to target card and flash chip

 There are no debug cores. 	Program devic	<u>e</u> <u>Refr</u>	esh device	
Hardware	_ 🗆	2 ×	Debug Probes	- 🗆 🖉 🗙
९ 🛣 🖨 🛃 📭 🕨 💓 🔳			🔍 🔀 🖨 🛃	
Name		Sta		
🗣 🚦 turano.nikhef.nl (2)		Conne		
	249854652 (1)	0 pe n		
♀-领 xc7vx690t_0 (1) └靋 XADC (System Md	🚳 Hardware (- Device F	properties	Ctrl+E
- O xilinx_tcf/Digilent/210	🔮 Program D	evice		
	🥏 Refresh De	vice		
	🔍 🧐 Add Config	uration	Memory Device	
	Boot from	Configu	ration Memory Devi	ce
	Program Bl	3R Key		
	Clear BBR H	(ey		
	Program el	FUSE Re	egisters	
	Export to S	preads	heet	

8	8 Add Configuration Memory Device								
6	Choose a configuration memory part. This can be changed later.								
De	evice: 🧇 xc7vx690	it_0							
Filte	er								
	<u>M</u> anufacturer	Micron		-		Туре	e bpi		-
	Density (<u>M</u> b)	1024		-		Width	n x16		
				Beset All	Filters				
				<u>Reset All</u>	FILLEIS				
Sele	ect Configuration N	lemory Part							
	i la	ioniony r are		7					
	Search: Q-]					
	Nam	e	Part	Manufacturer	Alias	Family	Туре	Density (Mb)	Width
	🥦 28f00am29ew-k	opi-x16	28f00am29ew	Micron		m29ew	bpi	1024	×16
	降 mt28gu01gaax	le-bpi-x16	mt28gu01gaaxle	Micron	28f00a g 18f	g18	bpi	1024	×16
	🌼 28f00ap30b-bp	i-x16	28f00ap30b	Micron		р30	bpi	1024	×16
	🌼 28f00ap30e-bp	i-x16	28f00ap30e	Micron		р30	bpi	1024	×16
	🌼 28f00ap30t-bpi	-×16	28f00ap30t	Micron		p30	bpi	1024	×16
	OK Cancel								

Both <u>HTG710 and VC709</u> have the same type of EEPROM: use filters **Micron – 1024 – bpi – x16**.

Select "Alias" 28f00ag18f

Add Configuration Memory Device Completed				
Do you want to program the configuration memory device now?				
Don't show this dialog again				
OKCancel				

8 Program Configuration Memory Device					
Select a configuration	file and set programming options.				
Memory Device: <u>C</u> onfiguration file: <u>S</u> tate of non-config	<pre>mt28qu01qaax1e-bpi-x16</pre>				
Program Operations Address Range:	Configuration File Only				
RS Pins:	NONE -				
፼ <u>E</u> rase □ <u>B</u> lank Check					
✓ P <u>r</u> ogram					
l ⊻ ⊻erity					
	OK Cancel				

If you cancel the operation above you can reassign a configuration .mcs file at a later stage from:

Hardware		_ 🗆 🖻 ×				
	Name	Status				
🗣 📱 turano.nikhef.	nl (2)	Connected				
∳- Ø- xilinx_tcf/D	igilent/210249854652 (1)	Open				
)t_0 (2)	Programmed				
- 🦉 XADC ((System Monitor)					
📃 🗆 🛶 mt28g	u01gaax1e-bpi-x16_0					
└─ 🖉 🖉 xilinx_tcf/D	igilent/210203826227A (0)	Closed				
Configuration Mem	ory Device Properties	_ 🗆 🖻 ×				
🔶 🔶 🔶						
🌼 mt28gu01gaaxle	e-bpi-x16_0					
Name:	mt28gu01gaaxle-bpi-x16_()				
Memory Part:	🔷 mt28gu01gaaxle-bpi-xl	6				
Memory type:	bpi					
Memory density:	1024					
Programming file:						