Technical Departments

Electronics Technology

Below a summary of the various projects in the department:

- ATLAS DAQ FELIX; (Front-End Link eXchange(FELIX) system), a common interface system for the ATLAS data acquisition, detector control and timing and control systems. The FELIX team demonstrated the required design progress in Design review in 2016. This was realised first using industrial evaluation boards and later with a prototype board that is based on an advanced Xilinx FPGA. The team now continues with the final design to be delivered in fall 2017.
- KM3Net first deployments and use of the optical network that is designed by the team in the electronics department:
  * Recovery of a detector line and review process of all major subsystems for stability and reliability improvements of the whole system.
  * Improvements in the stability and accuracy for timing synchronization implemented now in firmware and proposed for inclusion in hardware. Also calibration methods are further developed to achieve accurate timing (1 ns) for the foreseen number (~12,000) of optical modules in the final system. The used timing system 'White Rabbit' has spin-off for other experiments (*e.g.* CTA) with whom we already exchange useful experience. For calibration techniques we collaborate with the Free University of Amsterdam.

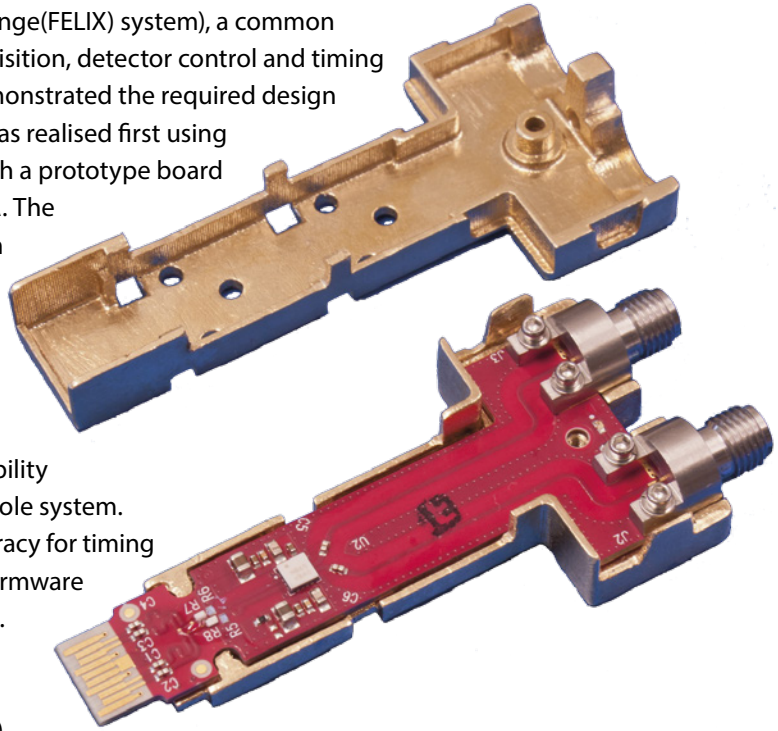

Figure 1. Picosecond Timing Calibration Test Tool; enclosure developed with 3D-design tools in co-operation with the Mechanical Technology department.

- LHCb SciFi readout system and board design with a special feature: "Design for manufacturability". This methodology is required for high-quality boards to be produced by selected industrial manufacturers. The final production may require a European tender procedure, and the present design method will result in the correct specification and quality criteria. This methodology was presented at the TWEPP2016 workshop in Karlsruhe by Wilco Vink.
- IC design: the electronics department contributes to the CERN RD53 R&D project. The project's purpose is to develop a common platform for ATLAS & CMS that can be used as a basis for a final pixel front-end chip for ATLAS and CMS with very high radiation tolerance.

Moreover, the ET delivered the following IC design results in 2016:

- Collaborative design of the ATLAS RD53 DRAD test chip for Radiation-tolerant digital library characterization. The chip is produced and characterised before and after irradiation and delivered very useful results in preparation for the RD53 pixel chip.
- Nikhef prototype: GWT65: a test chip for our 5 Gbps serialiser design in 65 nm CMOS technology. The circuit can be validated before integration in the RD53A chip, to be produced around summer 2017. The RD53A is the first common pixel front-end chip for ATLAS & CMS.

Figure 2. ATLAS FELIX design and integration workshop at Nikhef in October 2016.

- Contribution to LHCb VeloPix (LHCb Velo front-end pixel chip); produced in 2016 and tests are still on going. This chip is presently the most advanced pixel readout chip in the sub-atomic physics community; the IC contains about 190 million transistors.
- For testing the VeloPix IC, an available readout system for MediPix & TimePix IC's (SPIDR) was used and modified. Required was a chip readout speed of 20 Gbps (!) over 4 serial data lines. This is implemented and was made available in time.

New Techniques

This year Nikhef invested in an (expensive) advanced, high bandwidth (33 GHz) Real-Time oscilloscope for the Electronics department to characterise and debug serial data communication with FPGA's and ASIC's (like VeloPix).

Concerning personnel developments, the introduction of a flexible layer of personnel at Nikhef forces the department to actively choose what belongs to the core business and what not. The realisation of projects by outside companies is then an ongoing challenge. A successful example is the development of a frame grabber by TOPIC Embedded Systems for the ATLAS detector alignment. The system is installed in 2016 at CERN.

Computer Technology

For the Computer Technology Department, 2016 was a year of structural improvements and updates to prepare our systems for the future. For the system administration activities, this is a normal way of working to ensure smooth operation of the infrastructure, which from the point of view of its users takes place largely behind the scenes. This year's main efforts from the Experiment Support group and the group supporting the local analysis facility are also focused on preparations for the future.

Experiment Support

The barrel alignment system of the ATLAS muon spectrometer consists of more than 5,800 optical channels, each of which comprises a camera, a light source, a coded mask and a lens. The channels are eventually connected to an array of eight computers with frame grabbers. These computers with frame grabbers have been running for more than 10 years and needed to be replaced. Not only were they running an old and no longer supported operating system, but also the chances that hardware failures would disrupt operation of the alignment system have become too large to be acceptable. Replacement of the computers and their operating system triggered two major problems: there is no driver software for the frame grabber cards anymore that works with more recent operating systems, and newer computers no longer support the hardware interface used by the frame grabber cards. Consequently, alternative frame grabber cards were needed. Unfortunately, the market does not offer off-the-shelf alternative frame grabber cards that would be compatible with the 5,800 cameras and replacing the cameras was not an option. In close collaboration with the Electronics Technology Department, the search for an alternative solution resulted in a connection with the Dutch company TOPIC in Best, which is specialised in development of embedded software systems. TOPIC could build an embedded solution based on FPGA technology with an ARM processor, which is essentially a standalone small Linux server that can be configured and connected via the network. The new systems could be configured such that they are fully compatible drop-in replacements for the outdated computers and frame grabber cards. At the end of 2016, after shutdown of the LHC, the new solution has been installed in the ATLAS experiment. In 2017 a similar upgrade of an equivalent system in the LHCb experiment is foreseen.

Local Analysis Facility

The local analysis facility consists of a compute cluster *'Stoomboot'* with about 800 cores of processing power and a dedicated, high-performant storage system, which provides about 200 Terabytes disk capacity for storage of large data sets. This facility is known to give Nikhef's physicists a competitive advantage over research groups in other institutes.

After almost five years, both the hardware and software for the old storage system needed an update to increase its capacity to accommodate larger data volumes. Renewing the hardware is rather straightforward with plenty of choice by various vendors, but there is only a limited choice for a suitable storage system. A simple expansion into new hardware using the old system was not feasible due to scalability issues. Instead after careful consideration we opted to investigate the dCache storage system developed at DESY. dCache is widely used in the Grid computing context and has the required stability and scalability absent from the old storage system, but had not been used as storage for a local analysis facility. To ensure dCache would work in the context of our analysis facility we worked closely with the dCache developers to test, debug and deploy dCache for this new use case.

These efforts have resulted in taking the dCache system in production. It currently offers a net capacity of 550 Terabytes and will be enhanced with another 300 Terabytes in early 2017, leading to a fourfold increase of storage capacity. The system also has a better performance under high load conditions and supports multiple protocols for accessing the data, allowing more simultaneous analysis jobs to access the ever-growing data sets.

Mechanical Technology

At the Nikhef mechanical technology department, the activities for the upgrades of the LHC detectors Alice, ATLAS and LHCb have come to fruition, and will continue to consume most of the department's resources for the next year. Some highlights of 2016 are:

Figure 3. Eric Hennes won the Best Poster Award 2016 at the Conference on Precision Mechatronics of the Dutch Society for Precision Engineering (DSPE)

- The complex geometry of two monolithic half-size RF box prototypes for the LHCb Vertex Locator (VELO) have been successfully machined, with the critical foil milled to thicknesses of 0.5 and 0.25 mm. Moreover, in December the first full-size box has been almost finished.
- The final design of the readout box of the Scintillating Fiber detectors (SciFi) for LHCb has been tested. It includes a glass-filled nylon thermal insulation structure and 200 micron thick titanium cooling structure, both 3D-printed (see Fig. 4), as well as a high-precision positioning tool to ensure proper alignment of the fiber modules and the Silicon Photomultiplier sensors (SiPM).
- An in-house developed tool for cutting at high precision (20 micron) flexible printed circuits carrying the monolithic active pixel sensors of the Alice Inner Tracker.
- Mechanical highlights for the astroparticle physics projects:
- The mechanical design of the Scintillator Surface Detector (SSD) for the upgrade of the Pierre Auger Observatory has been successfully prototyped.

A total of 80 Digital Optical Modules (DOM) for KM3Net were produced in-house in 2016. The production capacity has grown to 200 DOMs per year.

Figure 4. Lara Veldt shows two connected 3D-printed, 0.2 mm wall thickness multichannel titanium cooling-structures, to be mounted inside the read-out box of the scintillation fiber tracking detector of the LHCb upgrade.