LHCb Outer Tracker – Electronics (NIKHEF)

Meeting Minutes
11 January 2006

Present:
A. Berkien, A. Pellegrino, T. Sluijk, J. Spelt, A. Zwart

A. Minutes

These minutes can be found at
http://www.nikhef.nl/pub/experiments/bfys/lhcb/outerTracker/Documents/Meetings/OT-Electronics-NIKHEF/11-01-2006/

B. Solved Issues

- For the time being (for 1st series FE) will live with the 3 GOL/AUX boards available, while D. Wiedner will get production of another 20 going
- Eduard clarified issues with ASDBLR ChipSerial
- 1 FTE for the LV lost (went back to Russia), but work outsourced for ~10,000 EUR
- HV Board failure analysis done (15% of boards failed, failures due to manufacturing errors) and sent to QPI. Meeting with QPI on 25/1/2006
- One Chinese student found and paperwork started for HV Boards test
- Man-power for construction of HV patch panel in LHCb will be A. Berkien
- A rack and cabling description document was provided by T. Sluijk

C. New Issues

Man-power issues and possible conflicts with the overall OT schedule were discussed. In particular:

- 1 FTE for the assembly of the FE box must be available by April 1st 2006
- 1 FTE for the C-frame assembly needed from now until half May (now covered by Tom+Ad+Jan)
- 1 additional Ph.D. student for FE test will be asked during platform gesprek, unclear whether we get one or ??% of one
- Materials, Manpower and Schedule for detector installation and commissioning needs to be evaluated, including detailed travel/detachering plans, in particular:
  - Preparations
  - C-frame installation
  - Cable trays and tunnel
  - FE-Box installation and test
  - OT commissioning and global commissioning
  - Etc.

In addition, problems with the 1st batch of the FE:

- OTIS Board assembly problems at RIPA
- OTIS Board test problems

D. Open Issues

The following issues are still open:

- Design of "small" FE boxes update by H. Band and checked by Ad , now two prototypes "ordered" at MA by half of January 2006 [J. Spelt]
- ASDBLR chips need to be "ordered" at Upenn by end of January 2006 (must be available by March 2006)
- Schedule of HV Boards PCB needs to be revised

E. Action List

FE Electronics:

1) Come to conclusions about HV Boards [J.Koopstra]
2) "Order" new ASDBLR chip series [E. Simioni]
3) Discuss with RIPA about OTIS Board assembly
4) Complete bonding and test of OTIS boards and FE electronics
5) Check status of "small" FE Box
6) Update FE production/assembly schedule (don't wait for test of batch N to start production/assembly of batch N+1???) [E.Heine]
7) Clarify the manpower issue for FE Box assembly [A. Pellegrino]
8) Clarify the manpower issue for FE Box test (30% of E. Simioni +???) [A. Pellegrino]

C-Frames

1) Do we need an FTE for the assembly or do we go on like this? [J. Spelt]
2) Eduard shall test cabling of C-frame [E. Simioni]
3) Tom provide electronic version of Rack+cabling document

Installation & Commissioning

1) Address man-power issue [T. Sluijk + E. Heine + A. Pellegrino]
2) Address time schedule issue [T. Sluijk + E. Heine]
3) Tom provide electronic version of Rack+cabling document
4) Order missing components (cables, cooling flexibles etc.)

F. Agenda for Next Meeting

- Checklist Open Issues and Station Action List
- Discussion Updated Schedule
- Discussion status CTRL Box

Adjournment:

The next meeting will be at 13:30 on Wednesday January 25 2006 in N-248.

Minutes submitted by: A. Pellegrino

Approved by: