MROD-X performance tests

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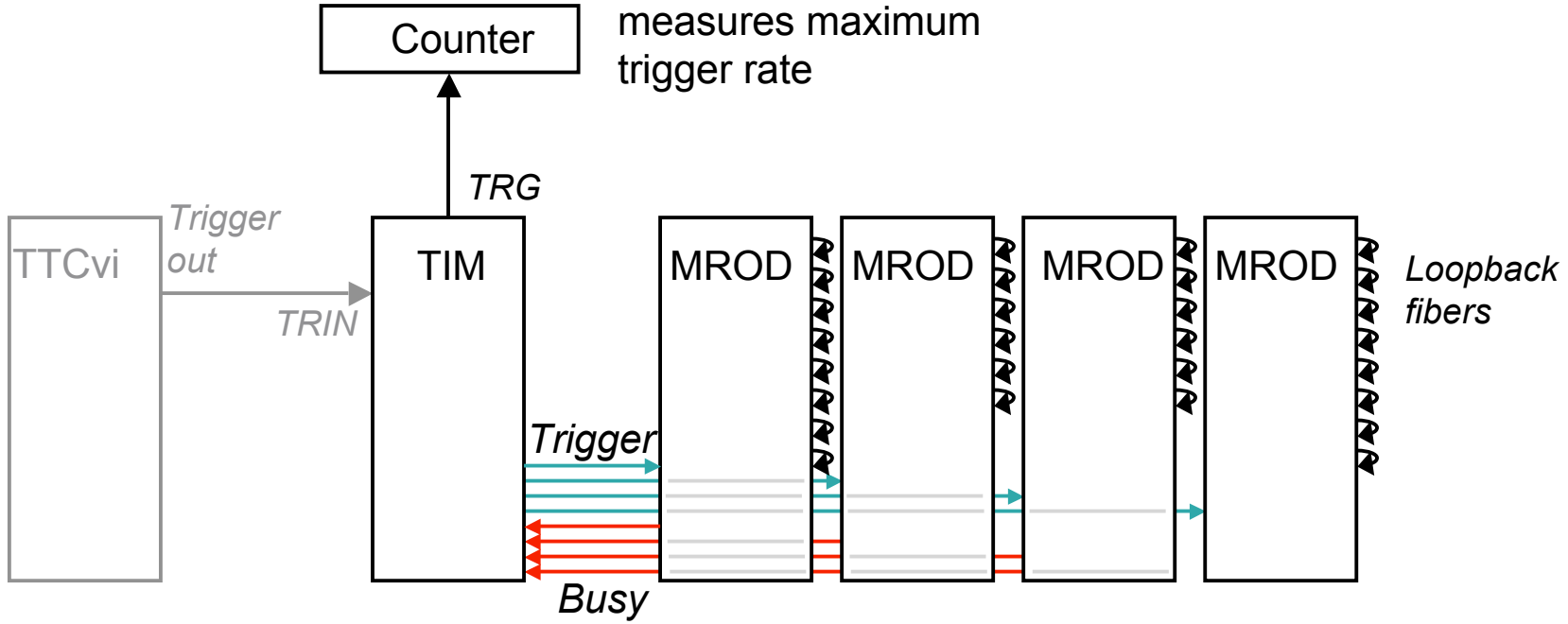
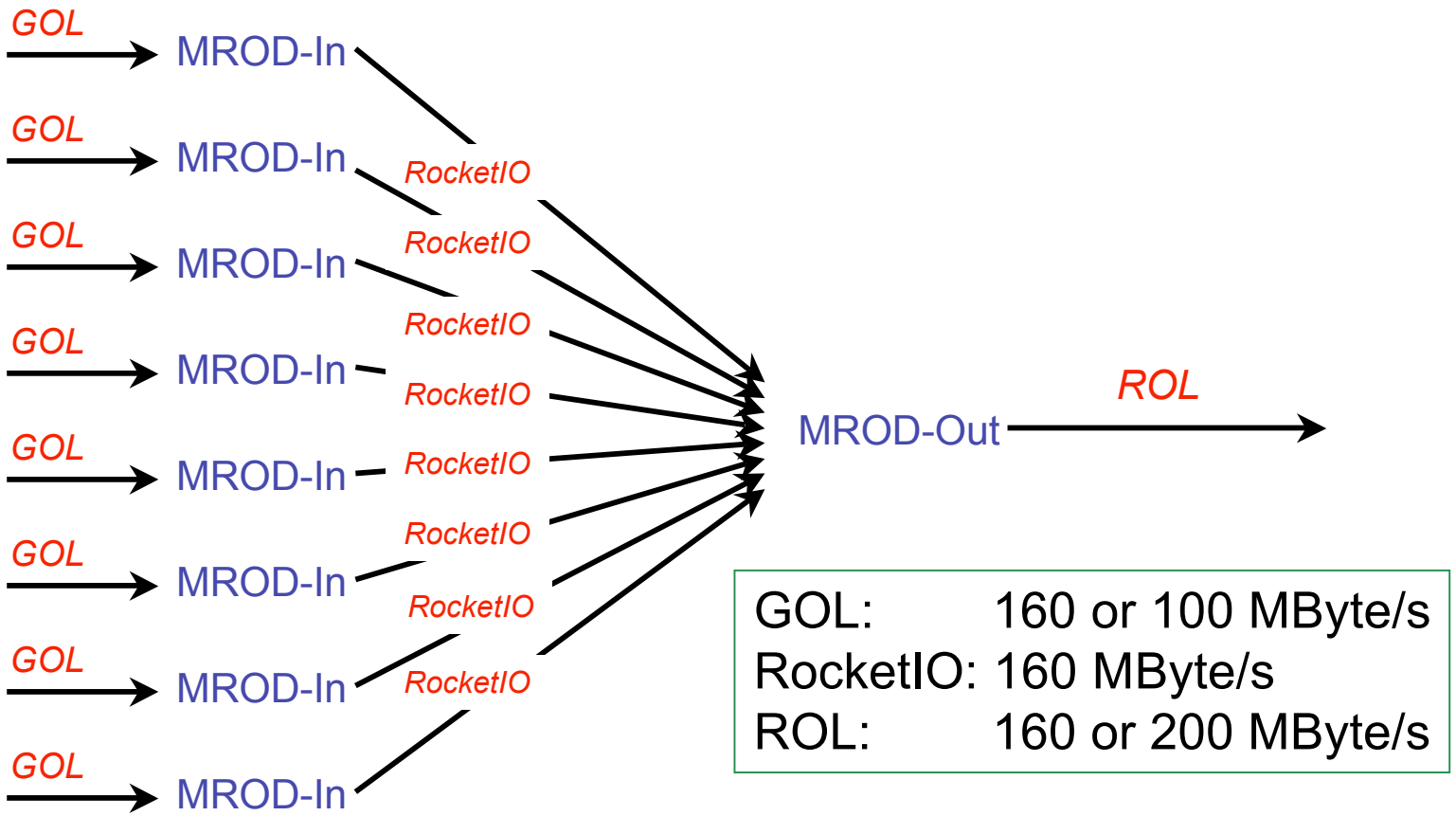


TTCvi: only used
for random triggers

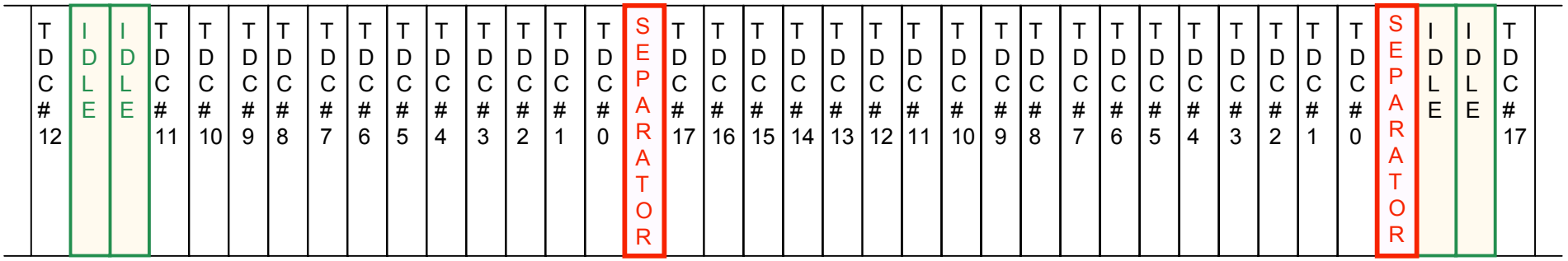
Busy and Trigger via backplane

TIM: can generate fixed rate (non-random) trigger, OR of busy signals suppresses
Internal or external trigger. Trigger signals sent to MRODs fire internal data generators.

Data flow into, inside and out of MROD-X



Data on the GOL link



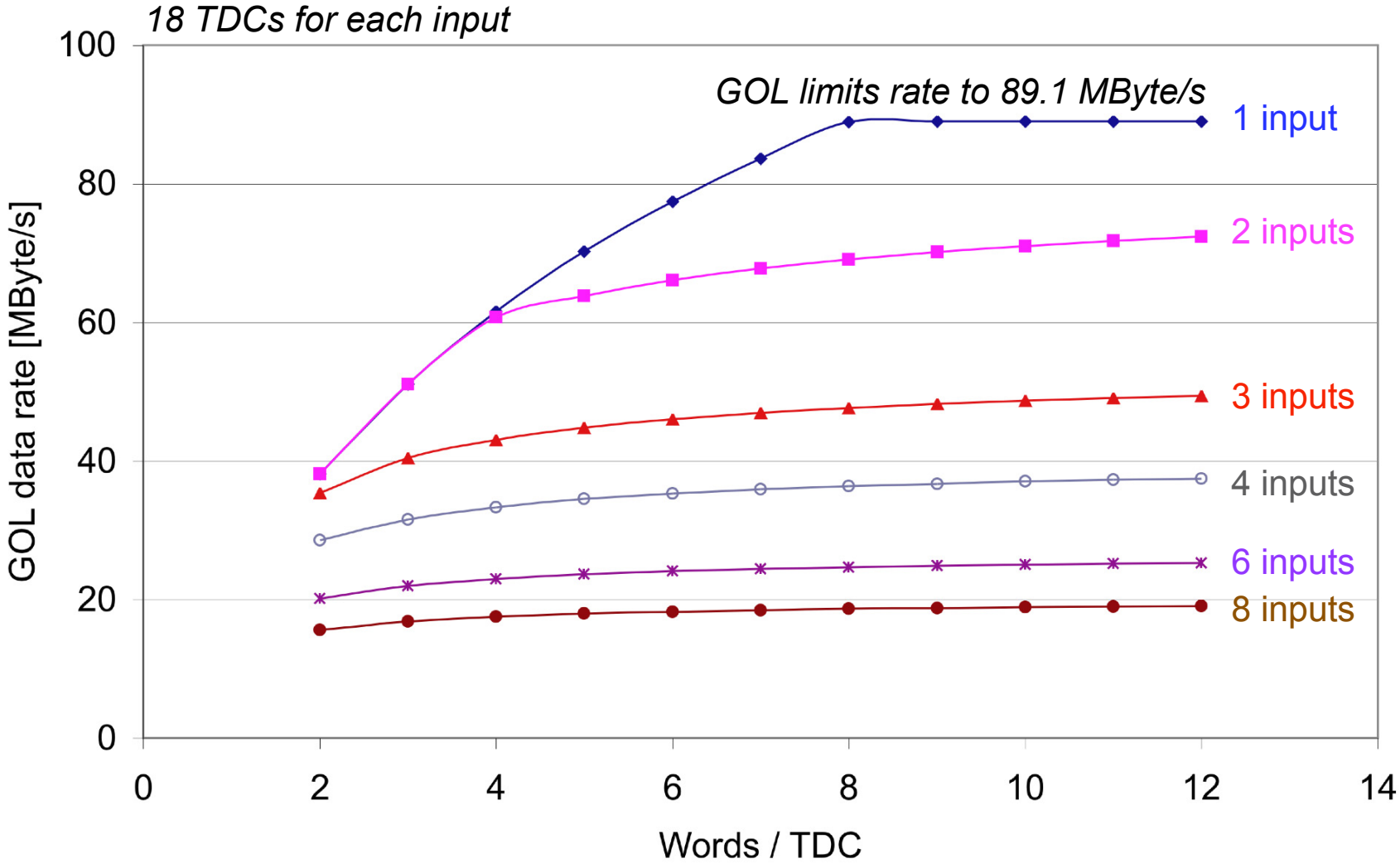
Test generator in MROD-X: inserts ever 32 cycles 2 idle cycles:
effective bandwidth = 32 / 34 = 94.12% of nominal bandwidth,
taking into account the separator word results in 94.12 * 18 / 19 = 89.16%

With **40 ns per word** the effective bandwidth is: **89.16 MByte/s**
With **25 ns per word** the effective bandwidth is: **142.66 MByte/s**

CSM: 2 idles after 19 words:
effective bandwidth = 19 / 21 = 90.48% of nominal bandwidth,
taking into account the separator word results in 94.12 * 18 / 19 = 85.71%

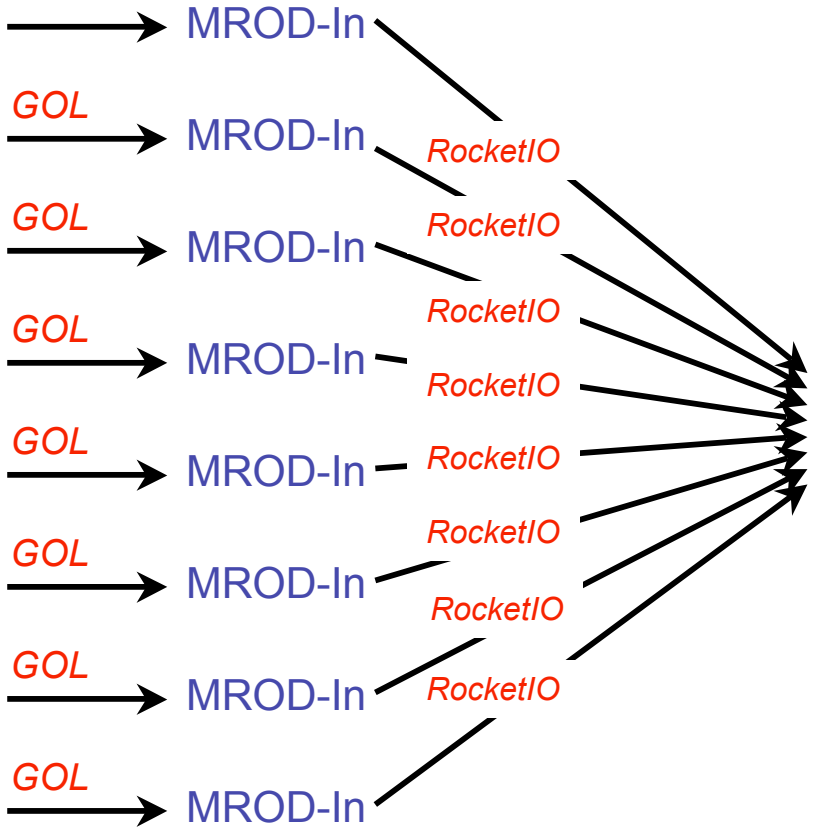
With **40 ns per word** the effective bandwidth is: **85.71 MByte/s**
With **25 ns per word** the effective bandwidth is: **137.14 MByte/s**

Results with test generator in MROD-X



2 - 8 inputs or 1 input with < 8 words / TDC: maximum rate **not** determined by GOL link

Data added to TDC data



GOL: 160 or 100 MByte/s
RocketIO: 160 MByte/s
ROL: 160 or 200 MByte/s

MROD-Out, for each event:

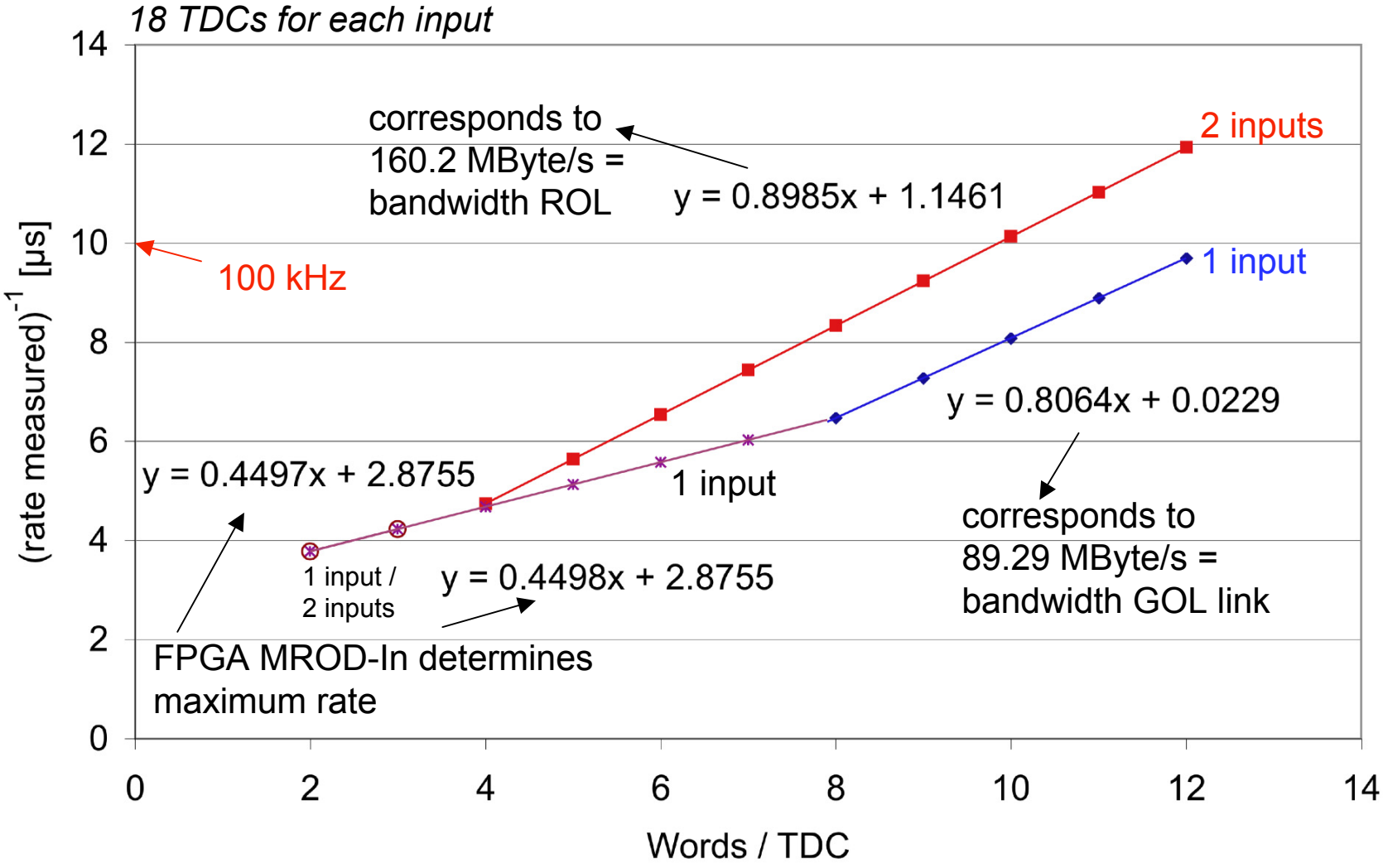
- strips "magic" words
- adds 9 header and 4 trailer words
- adds BOB and EOB words
- adds BOF and EOF control words

i.e. in total 17 words per event added, up to 8 words removed

MROD-In:

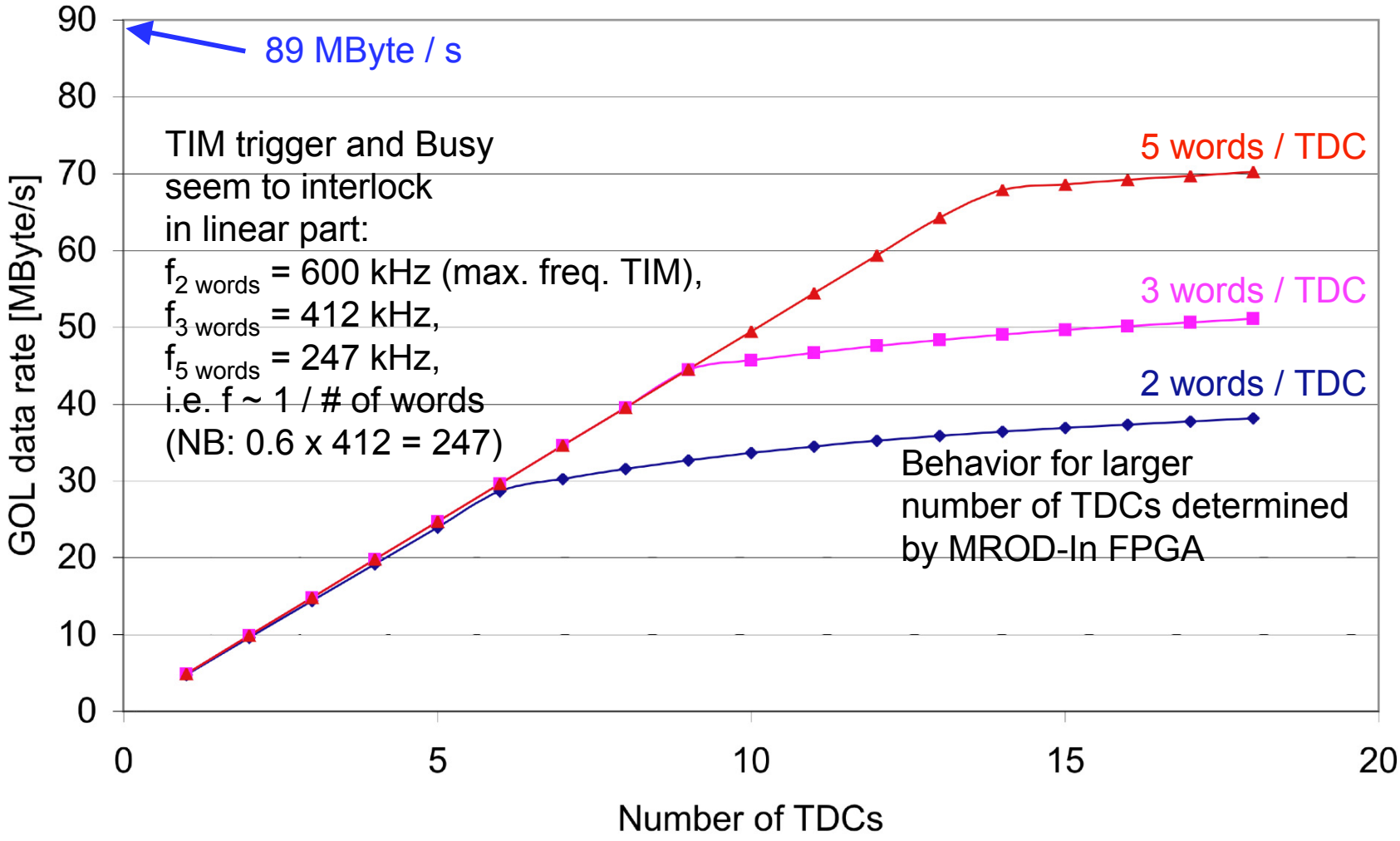
- strips separator words,
- adds one "magic" word (for MROD-1 compatibility) per event
- adds 4 additional words per event.
- via the RocketIO link idles and two more words are sent per event, but as these links are not fully utilized these data never affect the maximum event rate.

Inverse rate for 1 and 2 inputs

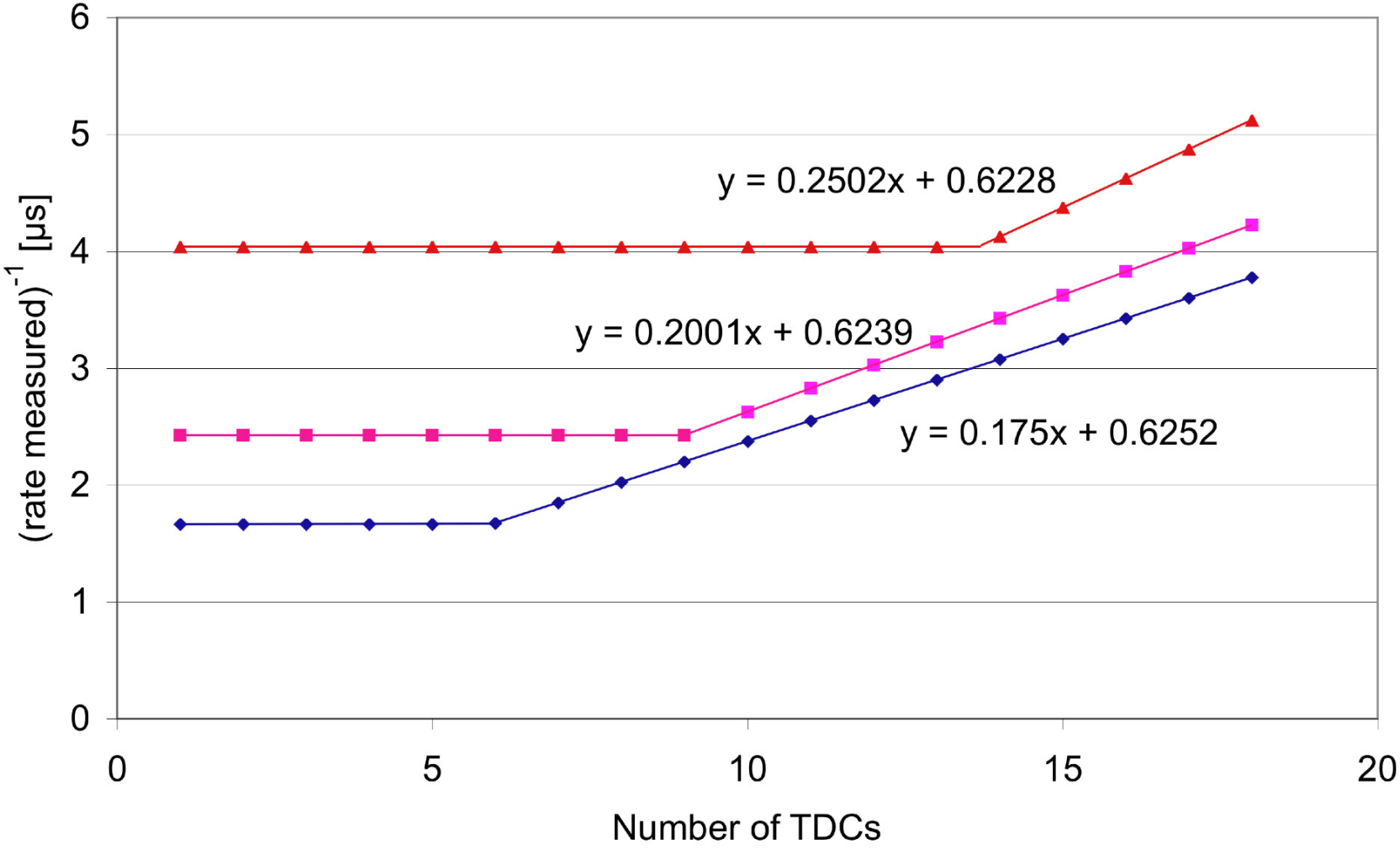


NB: time per event = 1 / rate measured

1 input: data rate below GOL maximum (89.1 MByte/s) for few words per TDC



Inverse rate for single input for few words per TDC

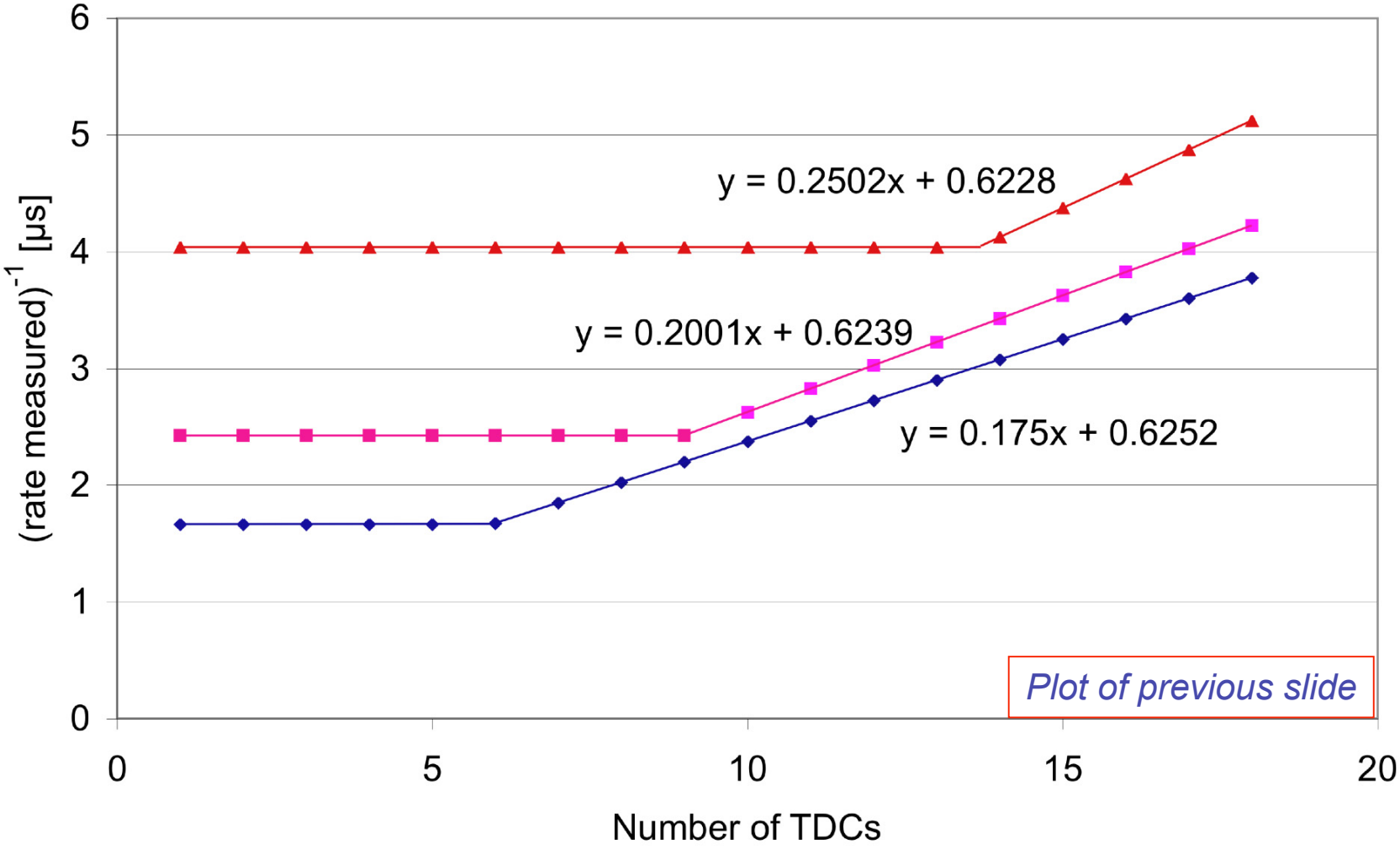


for 5 words per TDC: 0.250 µs.

-> *for each word: 0.025 µs* (FPGA clock of 40 MHz)

-> *+ per TDC 0.125 µs, i.e. 5 clock cycles*

Inverse rate for single input for few words per TDC



Per event: 0.625 µs, i.e. 25 clock cycles

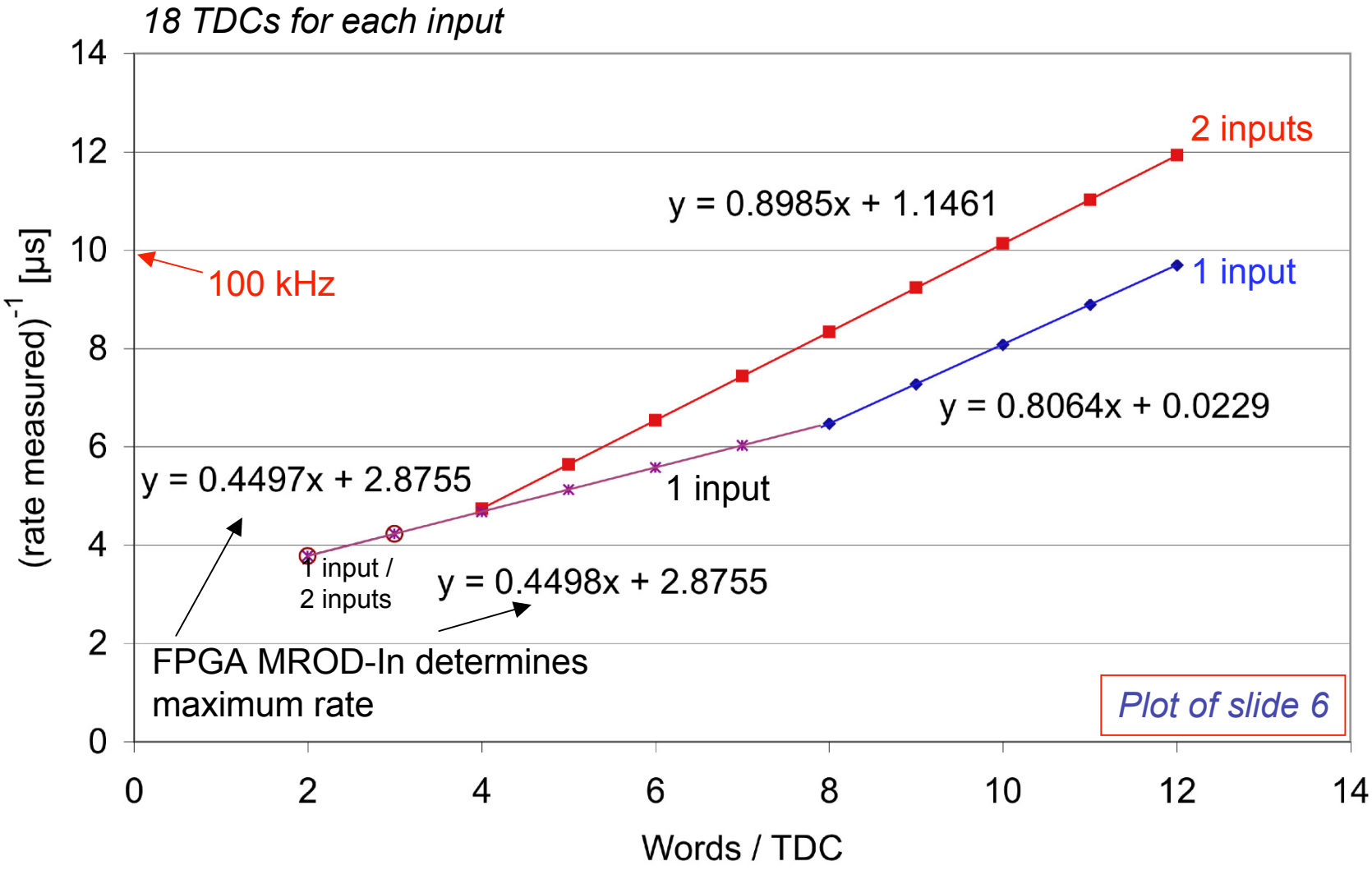
-> 1 cycle per TDC (active or inactive) ——— 18 cycles

-> transfer of "magic word" + additional words into the output FIFO —— 5 cycles

-> overhead ——— 2 cycles +

25 cycles

Inverse rate for 1 or 2 inputs for few words per TDC



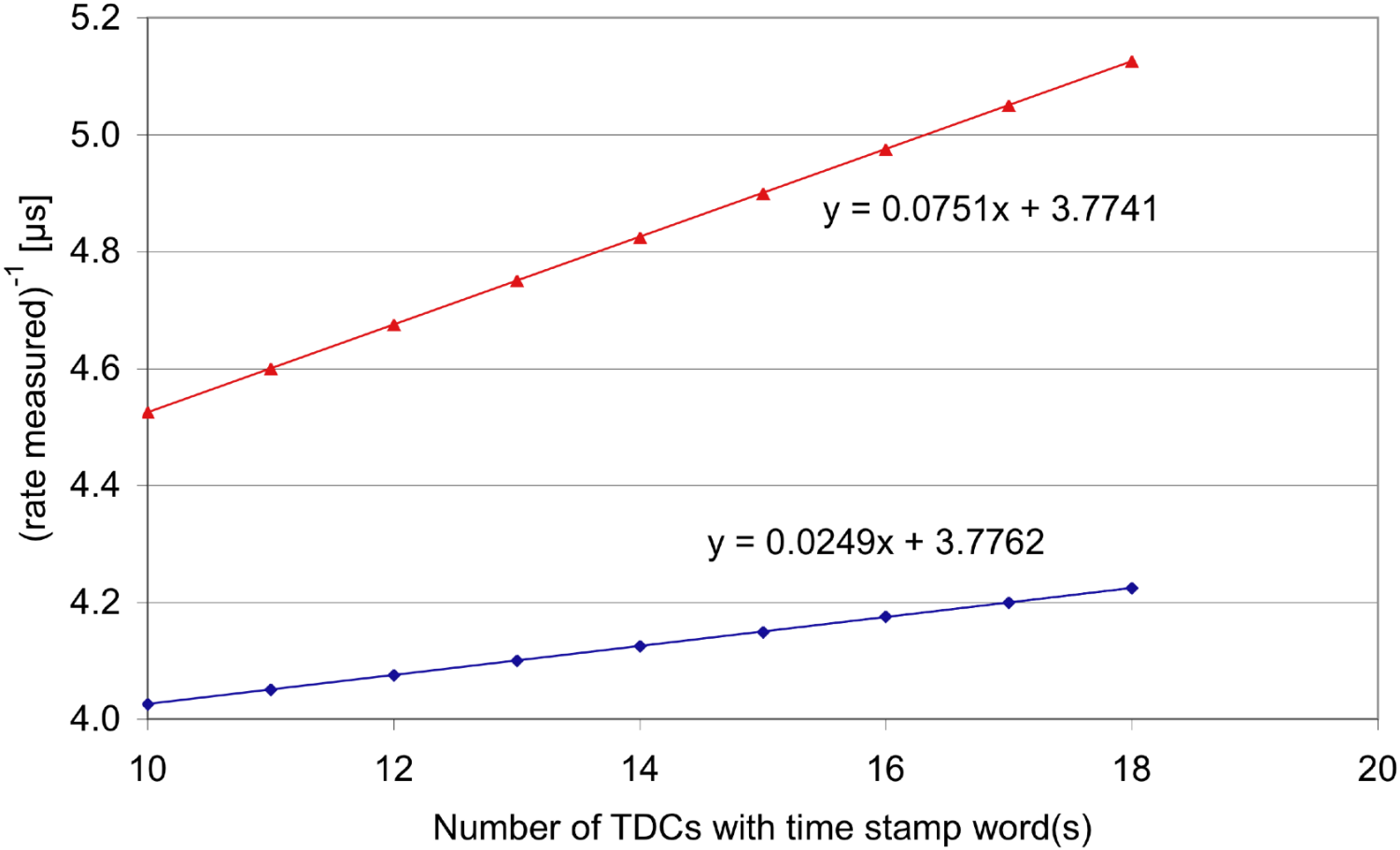
Transfer of 1 additional word for 18 TDCs -> 18 cycles, i.e. 0.45 µs.

For 18 TDCs active: per TDC 5 + 1 cycles 108 cycles

per event ——— 7 cycles +

total: 115 cycles, i.e. 2.875 µs

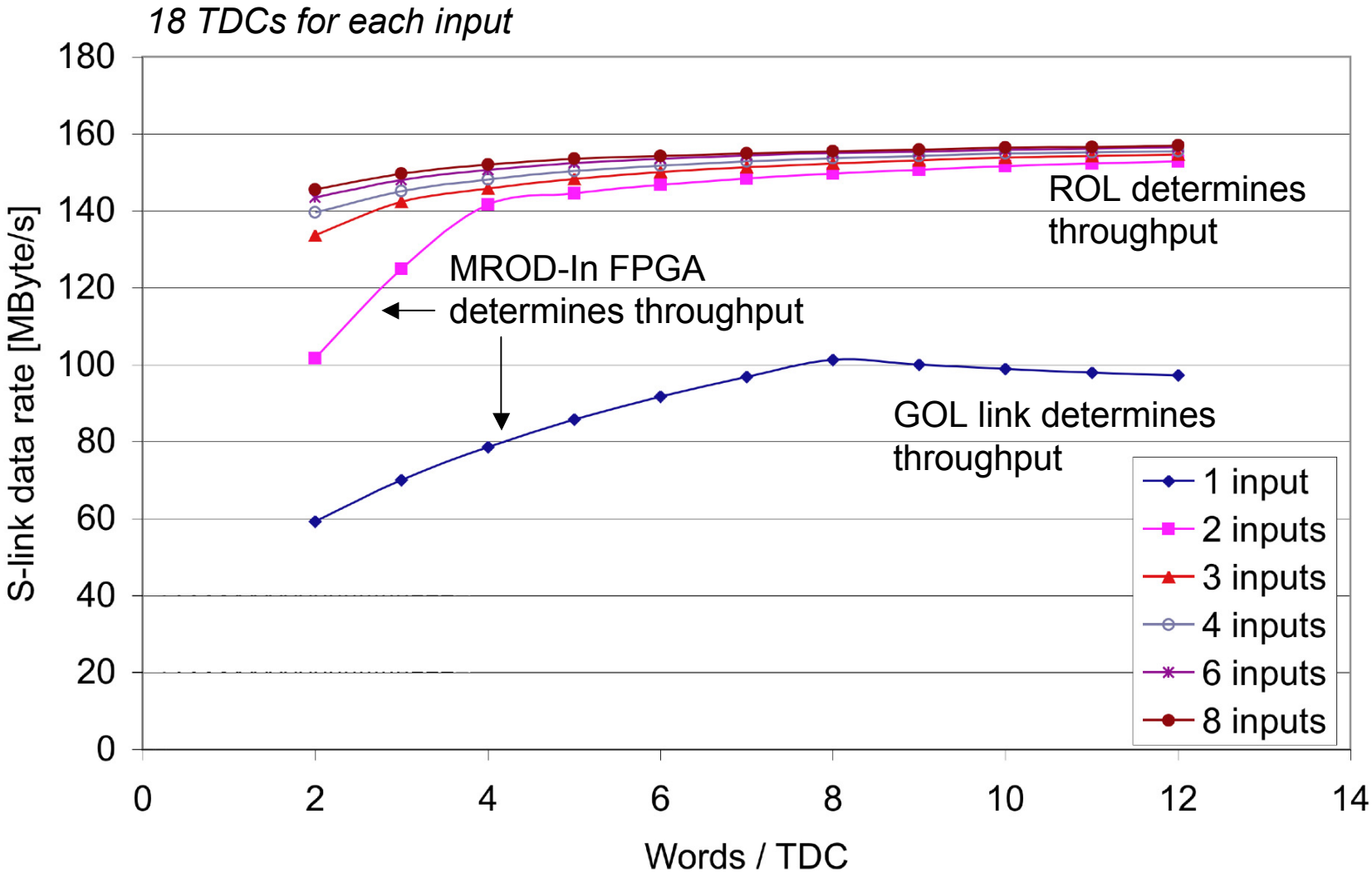
With zero-suppression on: inverse rate for single input, 18 TDCs active



Per additional time stamp word 0.025 µs, i.e. 1 clock cycle is needed

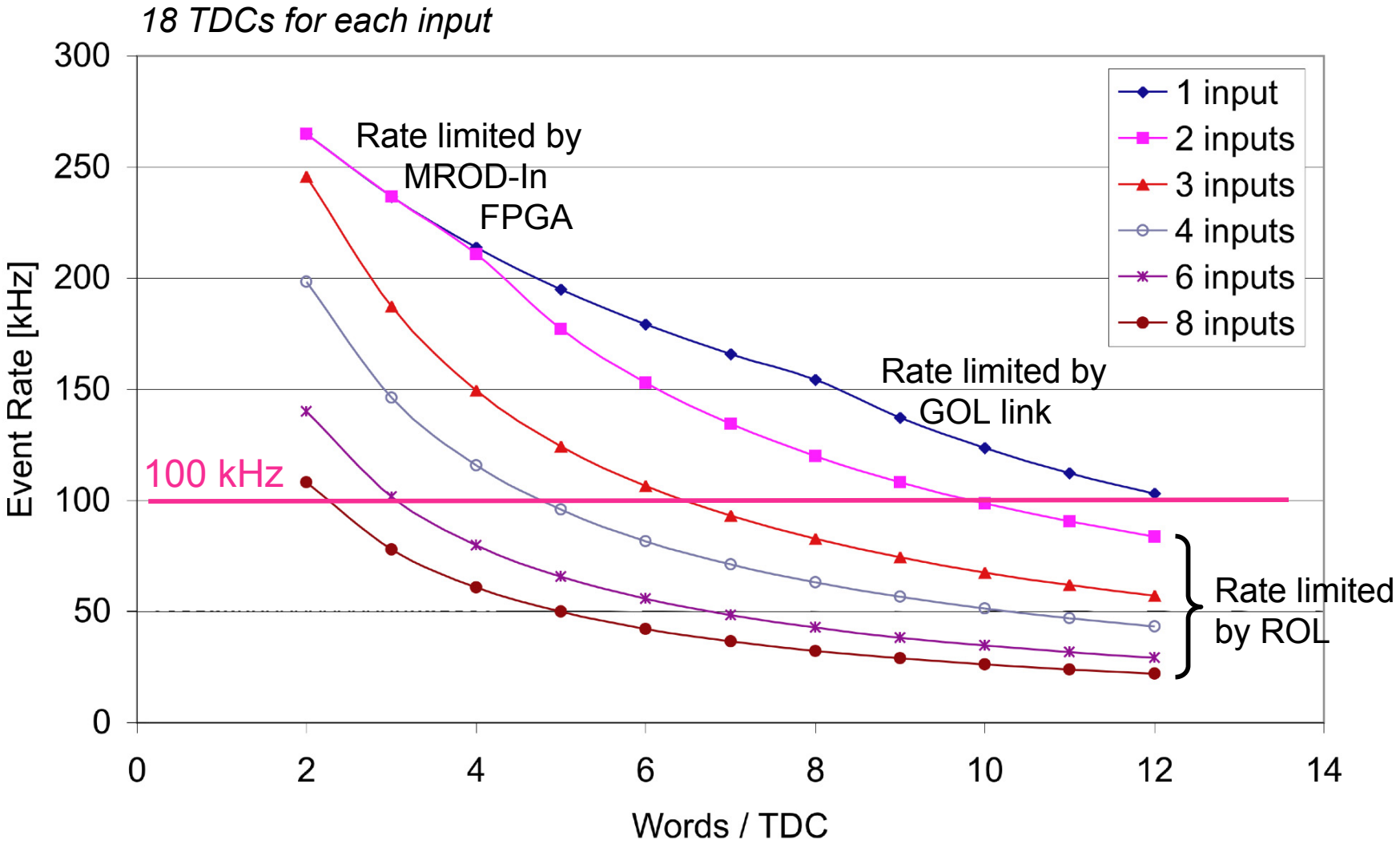
Without time stamps ~3.775 µs is needed, this comes from:
7 cycles overhead per event (2 + 5 for outputting data words) = 0.175 µs
6 cycles per TDC (1 + 5 per active partition) = 108 cycles = 2.700 µs
2 cycles per TDC for reading BOT/EOT words = 36 cycles = 0.900 µs +
3.775 µs

ROL bandwidth determines throughput in most cases

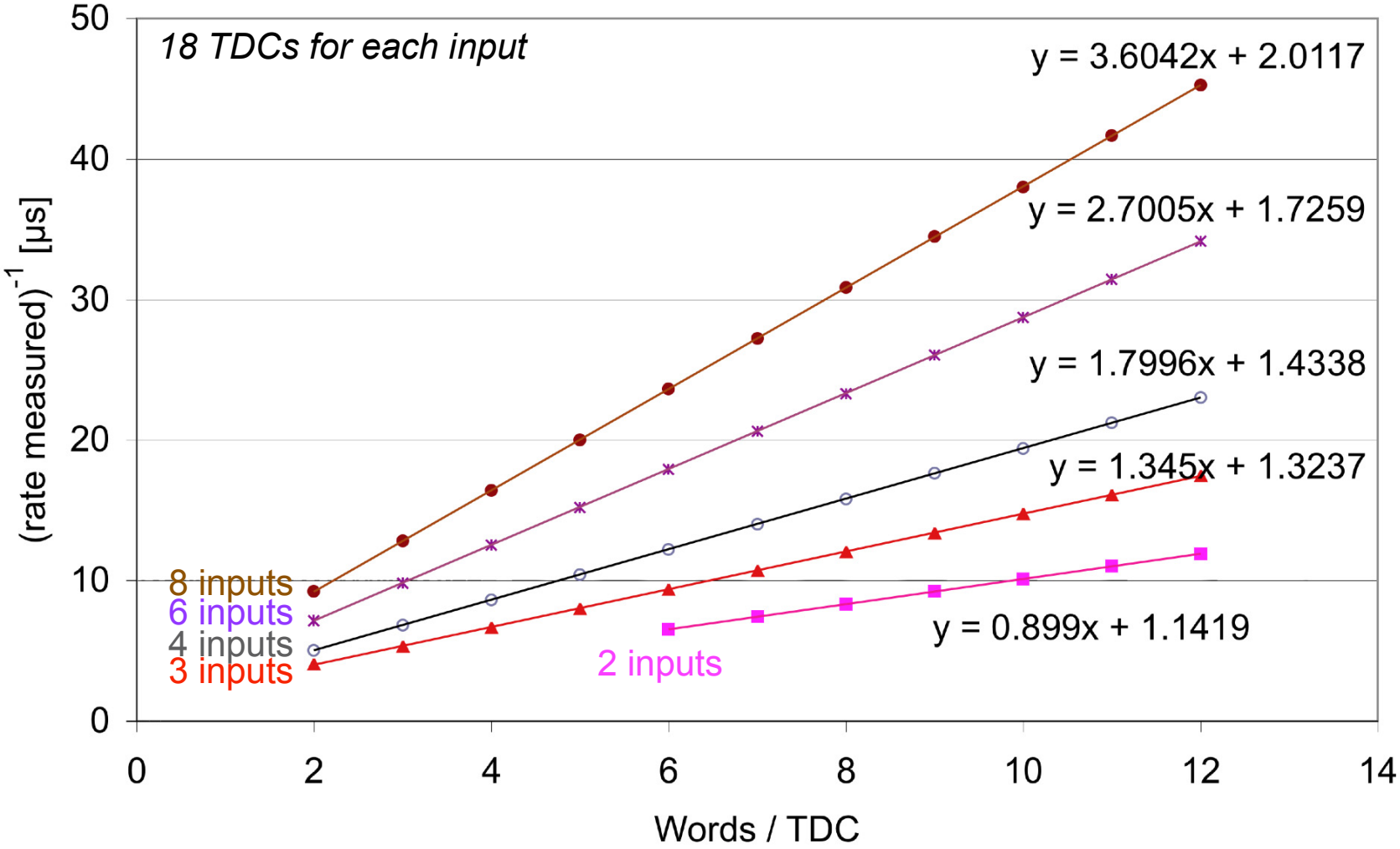


BOB and EOB control words not taken into account in bandwidth calculation

ROL bandwidth determines throughput for event rates < 100 kHz



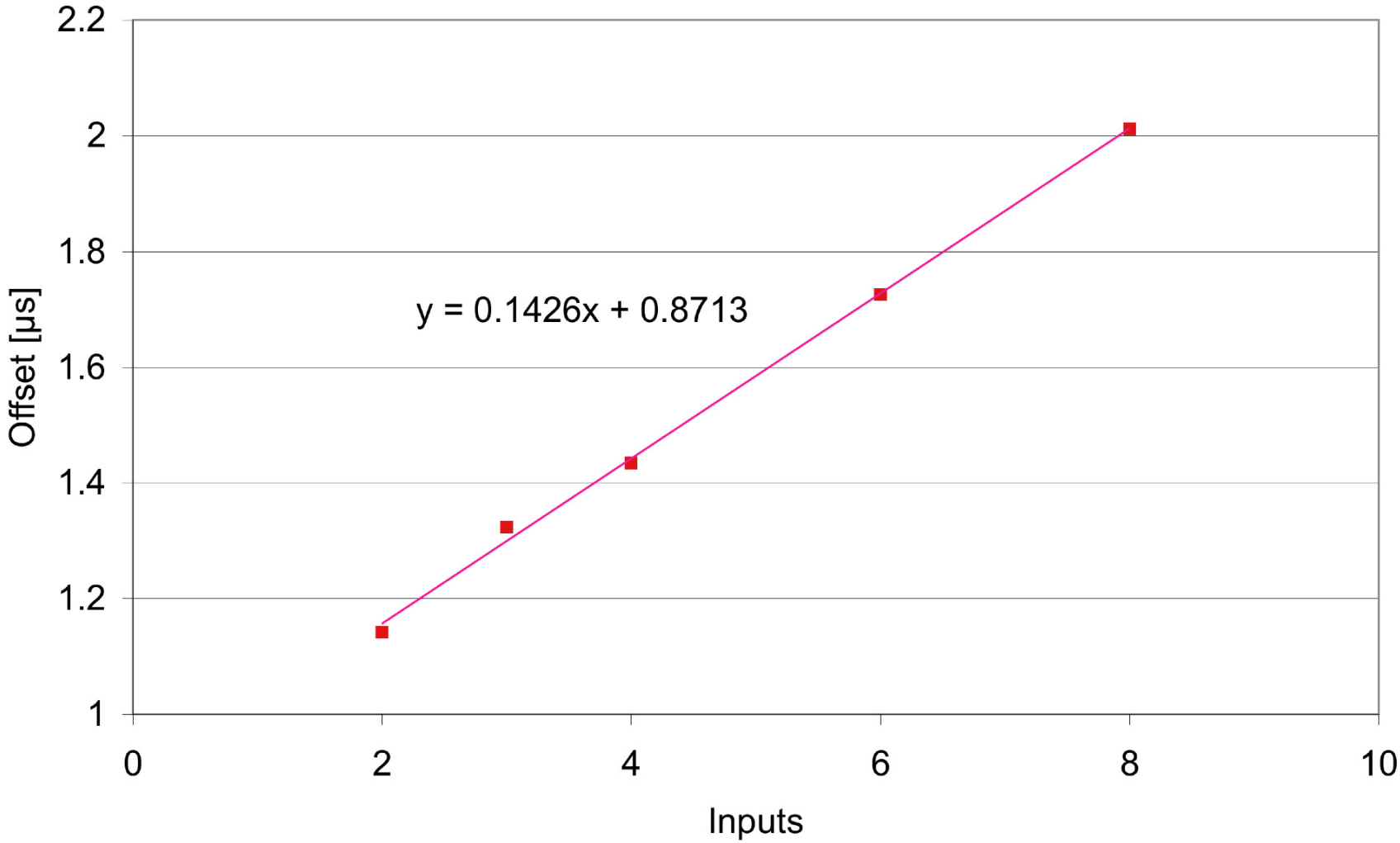
Increment in inverse rate for > 2 inputs consistent with ROL speed



3.6042 / (8 x 18) = 0.025 µs
2.7005 / (6 x 18) = 0.025 µs
1.7996 / (4 x 18) = 0.025 µs
1.345 / (3 x 18) = 0.025 µs
0.899 / (2 x 18) = 0.025 µs

As expected for ROL of 160 MByte/s
(0.025 µs per 32-bit word)

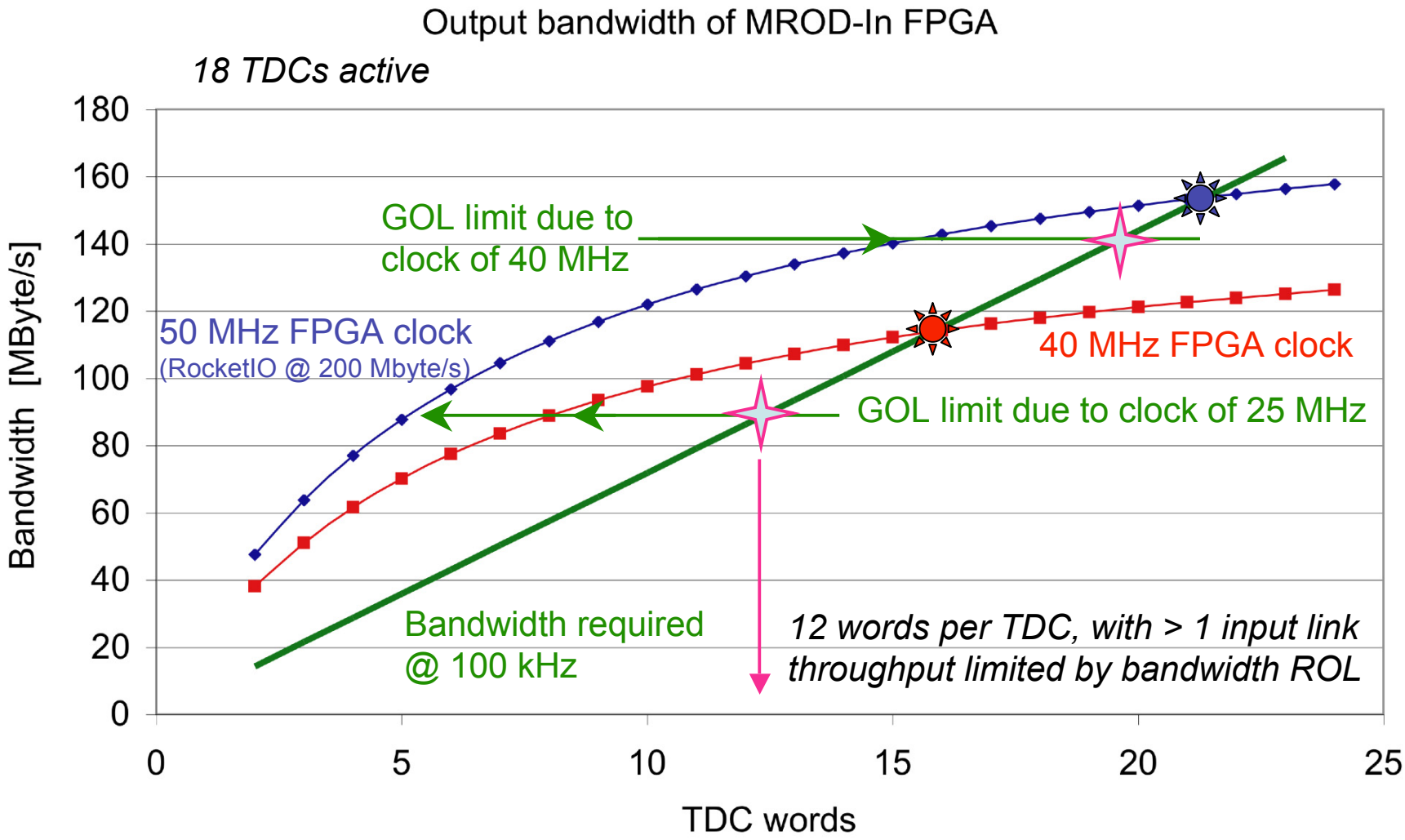
Offset in time per event as function of the numbers of inputs



Per input: ~0.15µs
for 4 words to be transferred via ROL
-> + 2 cycles per active RocketIO link

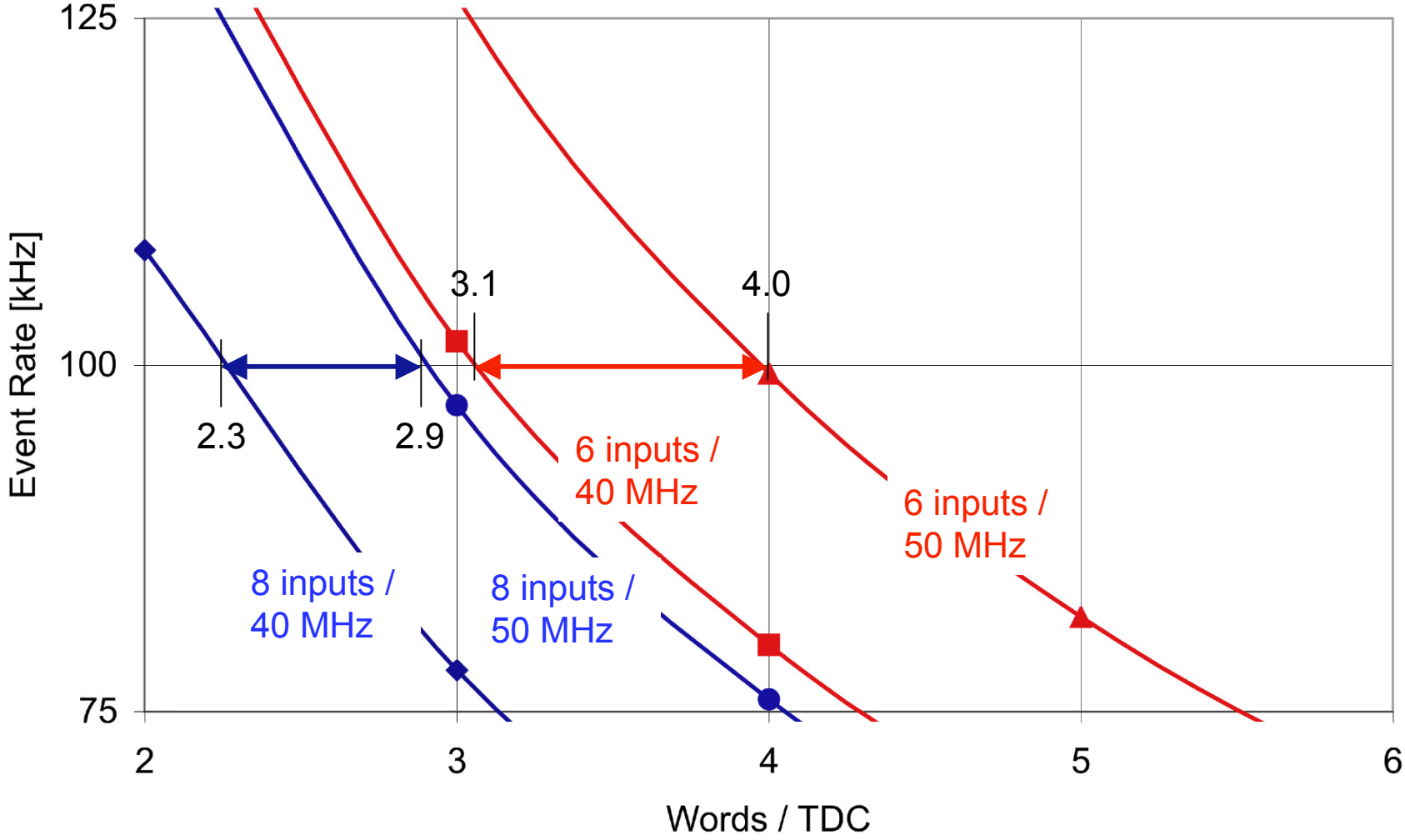
Per event: ~0.875 µs = 35 cycles
for 17 words to be transferred = 17 cycles
18 cycles additional overhead:
2 per link -> 16 cycles + 2 per event

Rate limitation by MROD-In FPGA



GOL @ 25 MHz, FPGA @ 40 MHz : GOL limits throughput @ 100 kHz
GOL @ 40 MHz, FPGA @ 40 MHz : FPGA limits throughput @ 100 kHz
GOL @ 40 MHz, FPGA @ 50 MHz : GOL limits throughput @ 100 kHz

Rate limitation by MROD-Out FPGA / ROL for 40 and 50 MHz clock, 18 TDCs for 6 or 8 inputs



MROD-Out FPGA clock 40 -> 50 MHz: throughput increases by ~1.3 for 6 inputs

(at 100 kHz and for 6 * 18 TDCs all outputting 3 - 4 words, note that 4 words correspond to header, time stamp for leading edge, time stamp for trailing edge and trailer)