Pixel Front-end development for CMS

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Outline

- Modifications at the front-end chips and data link for the next CMS pixel upgrade
- Overview of silicon pixel detector for CMS
- Planned design modifications for the readout chip (ROC)
- Simulations, results of first measurements on the ASIC test structures
CMS Pixel Detector BPIX

barrel pixel detector BPIX

forward pixel detector FPIX

Supply Tube (+Z)

Supply Tube (-Z)

5m
Barrel Pixel Detector Cabling
Barrel Pixel Detector Cabling

modules (66 x 20 mm)
sensor with 16 read out chips (ROC)
and one token bit manager (TBM)

BPIX supply tube with electro optical converter
DOH & AOH

barrel pixel detector
Front End Electronic (Barrel Pixel)

- 3 layers, 720 (half-)modules
- Data uplink: analog chain (electrical $\rightarrow$ optical), multi level coded & analog pulse height
- 1104 data uplinks (layer 1 & 2: two links; layer 3: one link / module) + 48 spares
- 1546 data fibres totally to PP0 (important for upgrade)
- 256 fibres for control (clock, trigger, setup) and status
- Sparsified system (zero suppression)
  $\rightarrow$ Data buffer to reduce data fluctuations
Requirements for an upgraded System

- 3 → 4 layers

<table>
<thead>
<tr>
<th></th>
<th>ladders</th>
<th>modules</th>
<th>ROC’s</th>
<th>pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>existing pixel detector</td>
<td>90</td>
<td>720</td>
<td>11’520</td>
<td>47.9 Mio</td>
</tr>
<tr>
<td>upgraded pixel detector</td>
<td>152</td>
<td>1216</td>
<td>19’456</td>
<td>80.9 Mio</td>
</tr>
</tbody>
</table>

- Reduce material budget (structure, cooling, cabling) → micro twisted pair cables
- Higher luminosity (2x10^{34} cm^{-2} s^{-1} peak)
- Same number of fibres to counting room (+ spares)
- Higher data rates not possible with analog link
  → digital uplink
  → 320 Mbit/s
  → increase size of data buffers

<table>
<thead>
<tr>
<th>layer</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>pixel fluence [MHz/cm^2]</td>
<td>224</td>
<td>96</td>
<td>48</td>
<td>27</td>
</tr>
<tr>
<td>hits / trigger / module</td>
<td>68</td>
<td>31</td>
<td>15</td>
<td>8.4</td>
</tr>
<tr>
<td>MBit/link/sec</td>
<td><strong>194</strong></td>
<td>93.6</td>
<td>55.9</td>
<td>40.0</td>
</tr>
<tr>
<td># links</td>
<td>128</td>
<td>224</td>
<td>352</td>
<td>512</td>
</tr>
</tbody>
</table>

estimated data rates (simulation done by H.C. Kästli, PSI)
Data loss Mechanisms in ROC

**SLHC rate data losses dominated by finite buffer sizes!**

**Pixel busy: 0.72%**
- pixel insensitive until hit transferred to data buffer (column drain mechanism)

**Double column busy: 2.03%**
- Column drain finds hit pixels and transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

**Data Buffer full: 0.68%**
- size: 80 (32)

**Timestamp Buffer full: 0.01%**
- size: 24 (12)

**Readout and double column reset:**
- 2.20% for 100kHz L1 trigger rate

**Luminosity:** $2 \times 10^{34} \text{ cm}^2 \text{ sec}^{-1}$
- layer 1 @ $R = 38 \text{ mm}$

**Total data loss:** 5.63%

**Simulation done by H.C. Kästli, PSI**
Digital Readout Overview

- ROC with digital readout & data buffers
- 160 Mbit/s: ROC to TBM
- Digital multiplexer in TBM
- 320 Mbit/s non standard electrical link from TBM to supply tube (1216 links in tracking area)
- 320 Mbit/s optical fibres
Double Column Interface Modifications

- Data buffer 32 to 80 cells
- Timestamp buffer 12 to 24 cells
- More space with new detector mechanics
- Reduce pitch (36 μm) to have space for readout buffer
ROC CIB Upgrade to Digital Readout

26 double column data buffer

DCOL token control
Pulse Height analog
Pixel Address 15 bit digital

8 bit SAR-ADC
readout buffer

23 bit

MUX
4 bit serializer

160 Mbit/s data bus

160 MHz
80 MHz
40 MHz

token control
sequencer

PLL clock distribution

Token In
Token Out

40 MHz Clock
Test Chip

- Test chip 0.5 x 14 mm, 250 nm ASIC (same as ROC)
- designed in March 2009 by Beat Meier, PSI Chip Design Core Group

- 4/8 bit ADC (Dane Oleson, University of Nebraska-Lincoln UNL, PIRE program)
- Frequency multiplier PLL (Shruti Shrestha, Kansas State University KSU, PIRE program)
- Electrical 320/160 Mbit/s link driver, receiver and cables (Marco Rossini, ETH)
- Serializer (160/320 MHz)
- Clock & data recovery (TBM, FED)
- Readout logic (40 MHz) (implemented on FPGA of electrical link tester)
Technical Data:

- Reference input: 40 MHz
- Outputs: 80 MHz (ADC), 160 MHz (serializer)
- No external components needed (includes loop filter, capacitors)

Block Diagram:

- **PFD**
  - LHC Clock 40 MHz
  - UP

- **Loop Filter**
  - 7 stage ring oscillator
  - 4.4k
  - 50pF
  - 3pF

- **VCO**
  - 160 MHz serial clock
  - 80 MHz ADC clock

- **Bypass filter caps**
- **Charge pump**
- **Driver**
- **Loop filter**

Technical Data:
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- Outputs: 80 MHz (ADC), 160 MHz (serializer)
- No external components needed (includes loop filter, capacitors)
Frequency Multiplier PLL Results

Test results:

- PLL locks for 10 ... 75 MHz reference frequency
- Supply current: 720 µA
- Lock time: 3 µs
- Jitter < 30 ps
8-bit ADC: design

- Successive approximation 8 bit ADC with S&H
- Clock frequency: 80 MHz
- Conversions time: 8 clock cycles
- 4 bit ADC with spy pads
8-bit ADC: test setup

- ADC seems to work (functional test at lower frequency)
- Supply current: 1 mA (depending on final settings), 2% of ROC power
- Some crosstalk problems
- Most critical component of the digital-ROC (→ Layout)

Measurements to do
- Linearity
- Radiation effects

Test setup with microscope and probe for spy pads
ROC Output Signal

Existing system:

- Analog 6 level code $\rightarrow$ 2.5 bits / LHC clock cycle (5 bit / LHC clock with 2 links per module)

New digital readout:

- Module to TBM: 160 Mbit/s, same frame length
- TBM to AOH: two channel multiplexed to 320 Mbit/s $\rightarrow$ 8 bits / LHC clock cycle, one fibre/module
- no linear drivers/receivers needed for analog link $\rightarrow$ low power digital link

existing analog signal
40 MHz (2.5 Bit / clock)

new digital ROC signal
(160 MHz)
Design Changes for the digital-ROC

- No pixel cell modifications
- Increase double column buffers
- Extra space for readout buffer
- Additional and replaced components in CIB
- Same interface to double column periphery
- Same wire bond pads
Electrical Low Power Data Link

- 1216 Up links from module to outside the tracking area
- 320 MBit/s over 1 m
- Unshielded micro twisted pair cable (125 µm wire diameter, low mass)

- Low power differential driver and receiver (LCDS)
- Bundled with power and control wires to one module cable
Results, Eye Pattern

- Wire length: 1 m
- 320 Mbit/s
- Minimal amplitude: 20 mV (+/- 10 mV)
- +/- 500 mV DC offset between driver and receiver
- Bit error rate < 10e-12 (different condition)
- Crosstalk: -27 dB
- Power consumption / link: 4 mW (12 pJ/bit)

Measurement done by Marco Rossini, ETH
Summary

- Digital readout for higher data rate with the installed fibres
- Small changes in present 0.25mm ROC and TBM (minimal effort)
- Limited to small regions in interface block + buffer enlargement (trivial)
- Changes in TBM restricted to uplink signal path. Target speed: 320 MHz
- Peak inefficiency for Layer 1: ≈ 5%
- ASIC test structures for critical components:
  - PLL frequency multiplier tested (irradiate)
  - 8 bit ADC running but some crosstalk problems to solve
  - LCDS Driver/Receiver: tested at 320 Mbit/s speed
  - 1m micro twisted pair cable optimized (bandwidth ↔ mass)
- Robust data link
- Start with ROC design changes: winter 2009/2010