CMOS Sensor R&D Progress Report

M.Winter on behalf of IReS-LEPSI-DAPNIA (& coll.)

Outline

- Signal processing
- Preliminary test results of 1st sensors with integrated signal processing (MIMOSA-6)
- System integration
- Summary: plans for 2003

Summary of prototypes fabricated

▶ 6 MIMOSA prototypes fabricated since 1999

chip	year	process	epi.	pitch	metal	peculiar
M1	1999	AMS $0.6\mu m$	$14\mu m$	$20\mu m$	3M	thick epitaxy
M2	2000	MIETEC $0.35\mu m$	$4.2\mu m$	$20\mu m$	5M	thin epitaxy
M3	2001	IBM $0.25\mu m$	$2\mu m$	$8\mu m$	3M	deep sub-μm
M4	2001	AMS $0.35\mu m$	0 !	$20\mu m$	3M	low dop. substrate
M5	2001	AMS $0.6\mu m$	$14\mu m$	$17\mu m$	3M	real scale
M6	2002	MIETEC $0.35\mu m$	$4.2\mu m$	$28\mu m$	5M	col. // r.o. int. spars.

▶ MIMOSA-1, -2, -3, -4, -5 tested
(in particular with 120 GeV/c π^- at CERN-SPS)

▶ MIMOSA-6: tests under way

Signal processing

- Governed by N($e^{\pm}_{BS}$) in first Vx. Det. layer:

  $N^{sim}_{\pm}(90^\circ)$ = 5.5 $e^{\pm}$ / cm^2 / BX 500 GeV (R=15 mm)

  $\hookrightarrow$ occ. $\gtrsim$ 3-5 % in 100 μs ($m_{clust} \sim 5$)

- Safety factors (simulation accuracy, uncertainty on B, higher $\sqrt{s}$, shorter Δt_{BX}) $\rightsquigarrow$ occ. $\gtrsim$ 15-25 % in 100 μs

- Goal: $t_{L1} \sim$ 25-50 μs (R&D needed)

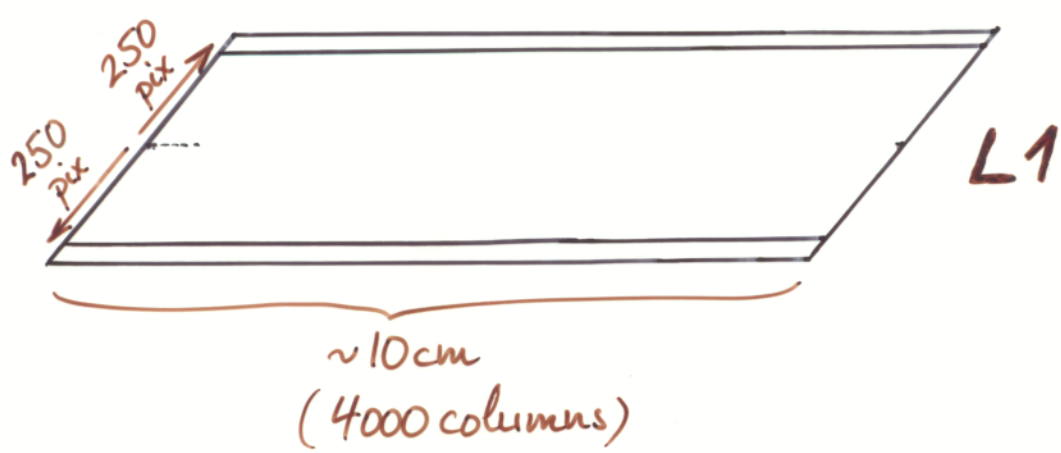
  $t^{L2-5}_{lect} \sim 100 \xrightarrow{R} 200$ μs (no major difficulty)

- major obstacle: data flux (L1)

  $\hookrightarrow$ 15 bits/pix, $t_{L1} \sim 25$ $\mu s \longrightarrow \sim$ 500 Gbits/s/10^6 pix

  ($e^{\pm}_{BS}$: 5 Gbits/s)

$\Rightarrow$ Next CMOS sensor prototypes address signal processing speed AND data compression



1st test results of MIMOSA-6

- Pixels with amplif. & charge storage of 2 consecutive frames:
  - $I_{polar.}$, $V_T \sim$ design values — **Fig. →**
  - measured charge-to-voltage gain at pixel exit as expected from simulation ($\pm$ 15 %)
  - 1st tests with ^{55}Fe (1640 e$^-$): S/N $\sim$ 50 after C.D.S. performed inside pixels (i.e. no off-line treatment)

    $\hookrightarrow$ calibration under way ($\Rightarrow$ S/N $\nearrow$ 110) — Fig. →

- Discriminators integ. on chip periphery at column bottom:
  - measured offset dispersion $\sim$ 1 mV: OK — Fig. →

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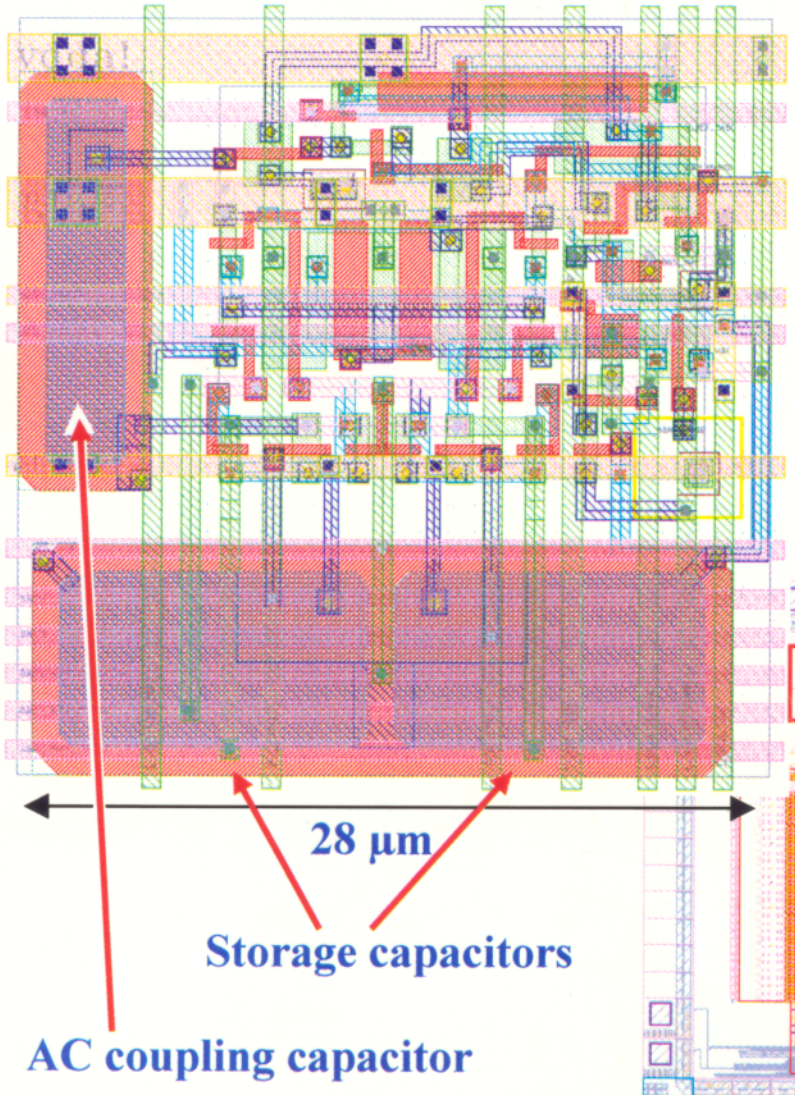
☑ MIMOSA VI - design

Single pixel layout



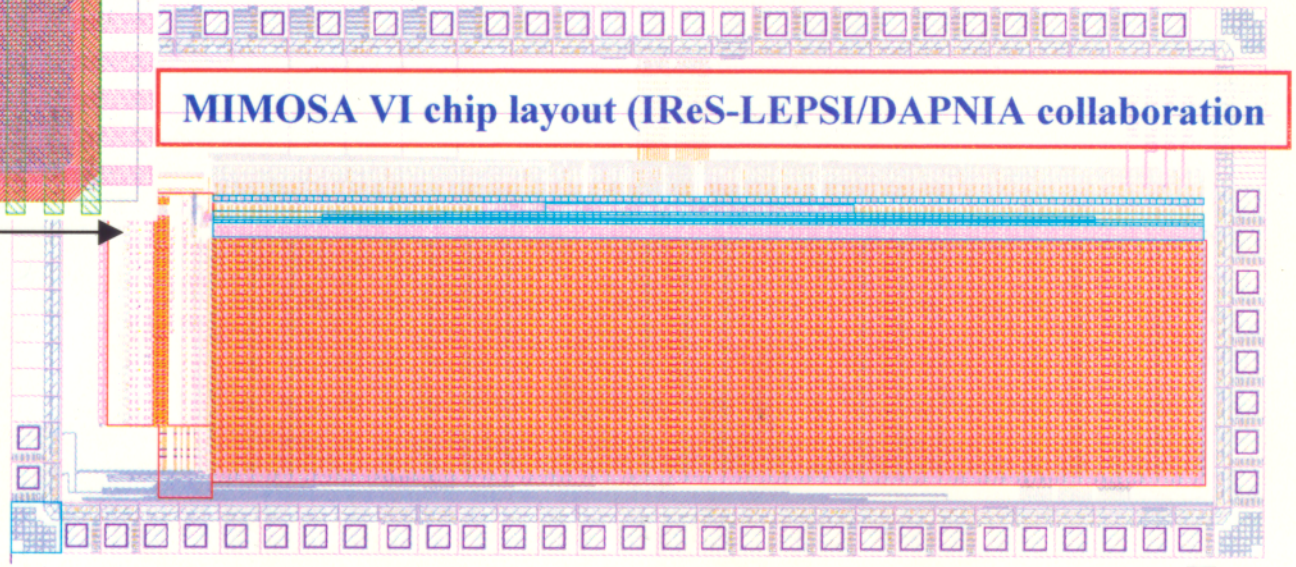
◎ Pixel design features:

- only NMOS transistors, nwell/p-epi and pdiff/nwell diodes and poly1-to-poly2 capacitors.

◎ MIMOSA VI key design features

- 0.35 µm CMOS 4.2 µm thick EPI layer,
- 1 array (24+6) × 128 pixels, pitch 28 × 28 µm^2,
- 24 columns read-out in parallel,
- 30 MHz f_{clk}, 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size 4.0 × 3.7 µm^2 - 3.5 fF,

MIMOSA VI chip layout (IReS-LEPSI/DAPNIA collaboration



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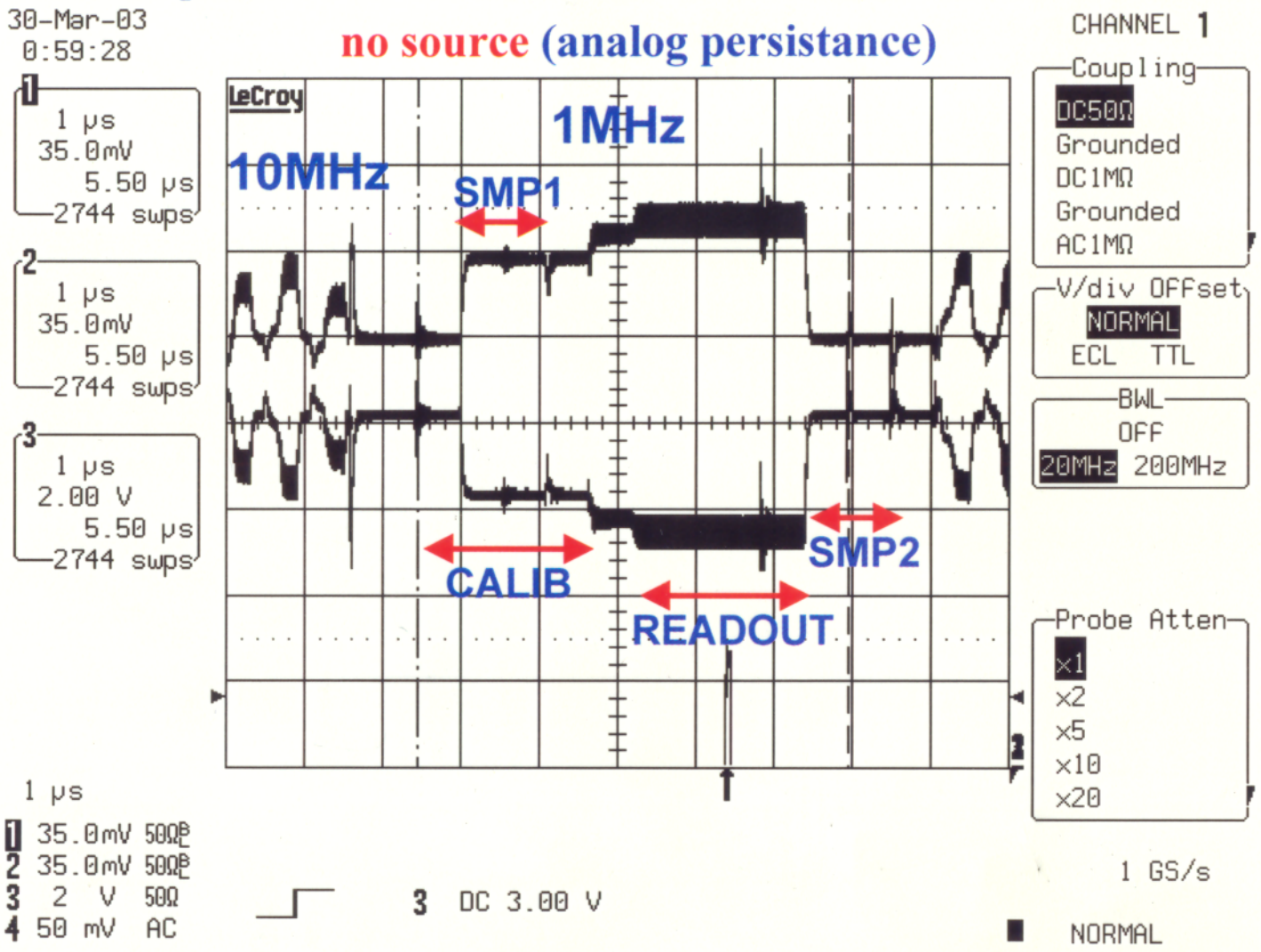
☑ MIMOSA VI - analogue part - preliminary results

☑ Pixel readout phases



digital 8bit oscilloscope, single channel, one pixel @1MHz (for easy visualisation)

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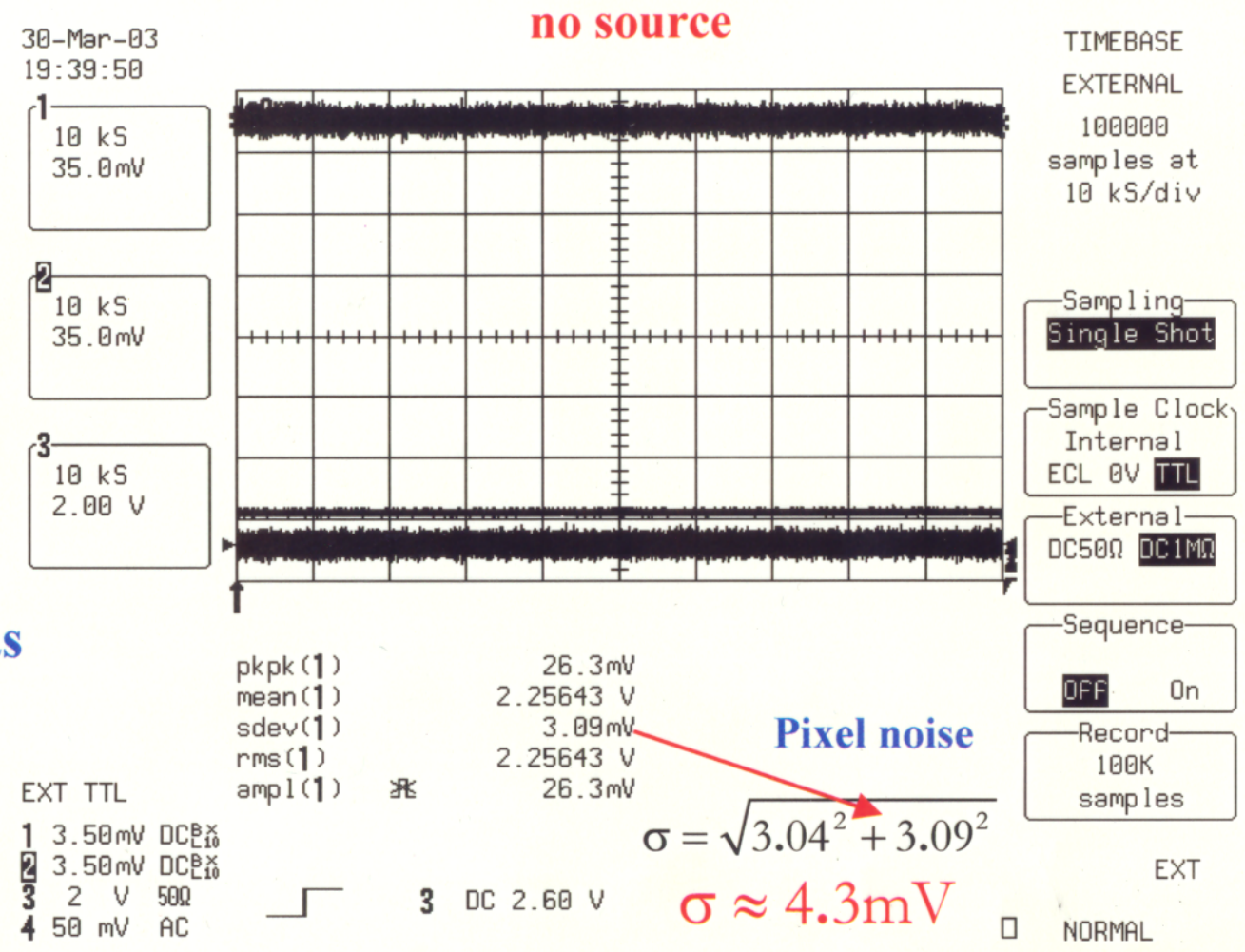
☑ MIMOSA VI - analogue part - preliminary results

☑ Differential output sampled during READ_OUT phase



τ_{int}=77µs

Pixel noise

$$\sigma = \sqrt{3.04^2 + 3.09^2}$$

$$\sigma \approx 4.3\text{mV}$$

digital 8bit oscilloscope, single channel, external sample clock, 100k samples

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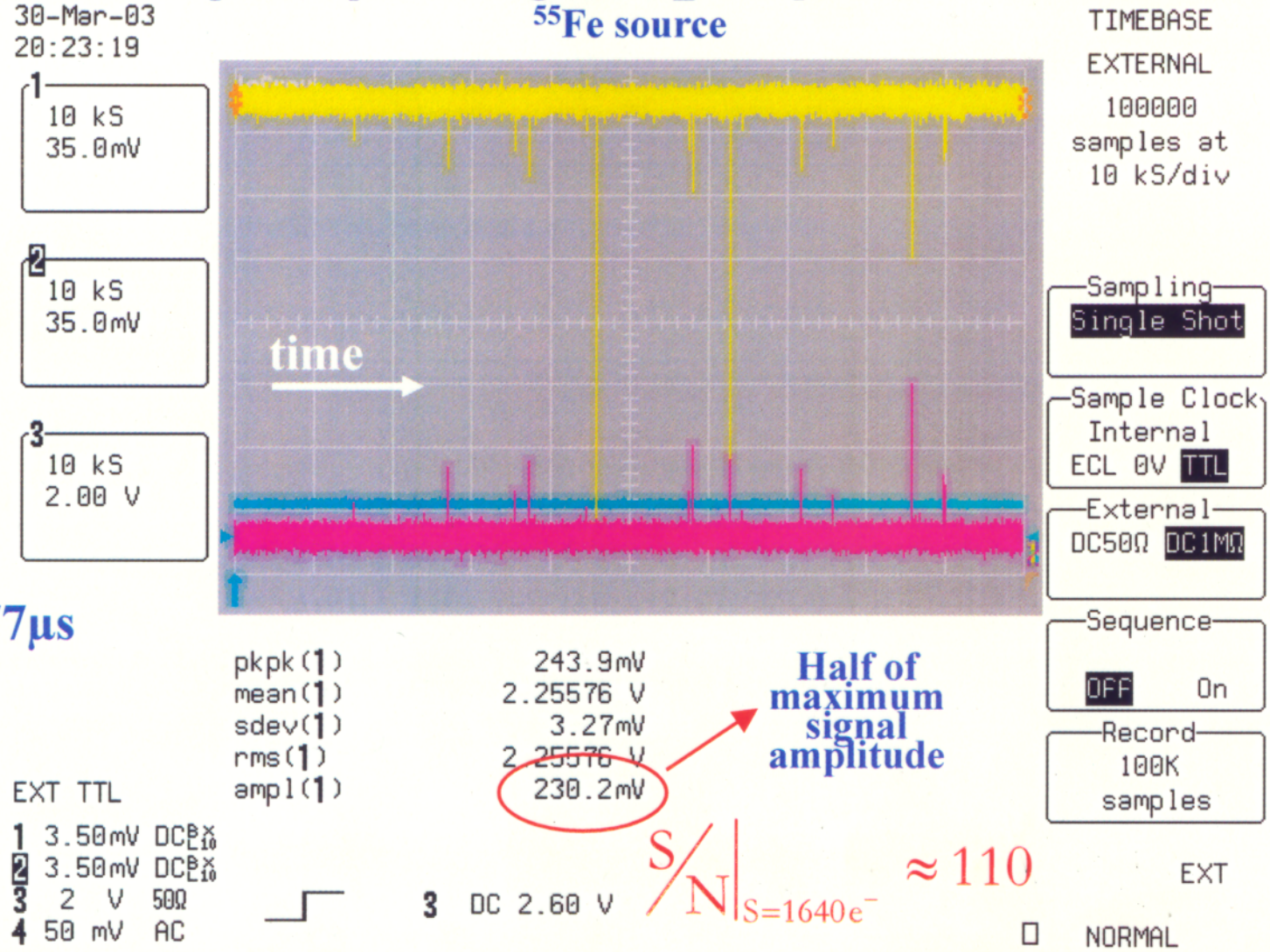
☑ MIMOSA VI - analogue part - preliminary results

☑ Differential output sampled during READ_OUT phase



τ_{int}=77µs

Half of maximum signal amplitude

$\left.\frac{S}{N}\right|_{S=1640e^-} \approx 110$

digital 8bit oscilloscope, single channel, external sample clock, 100k samples

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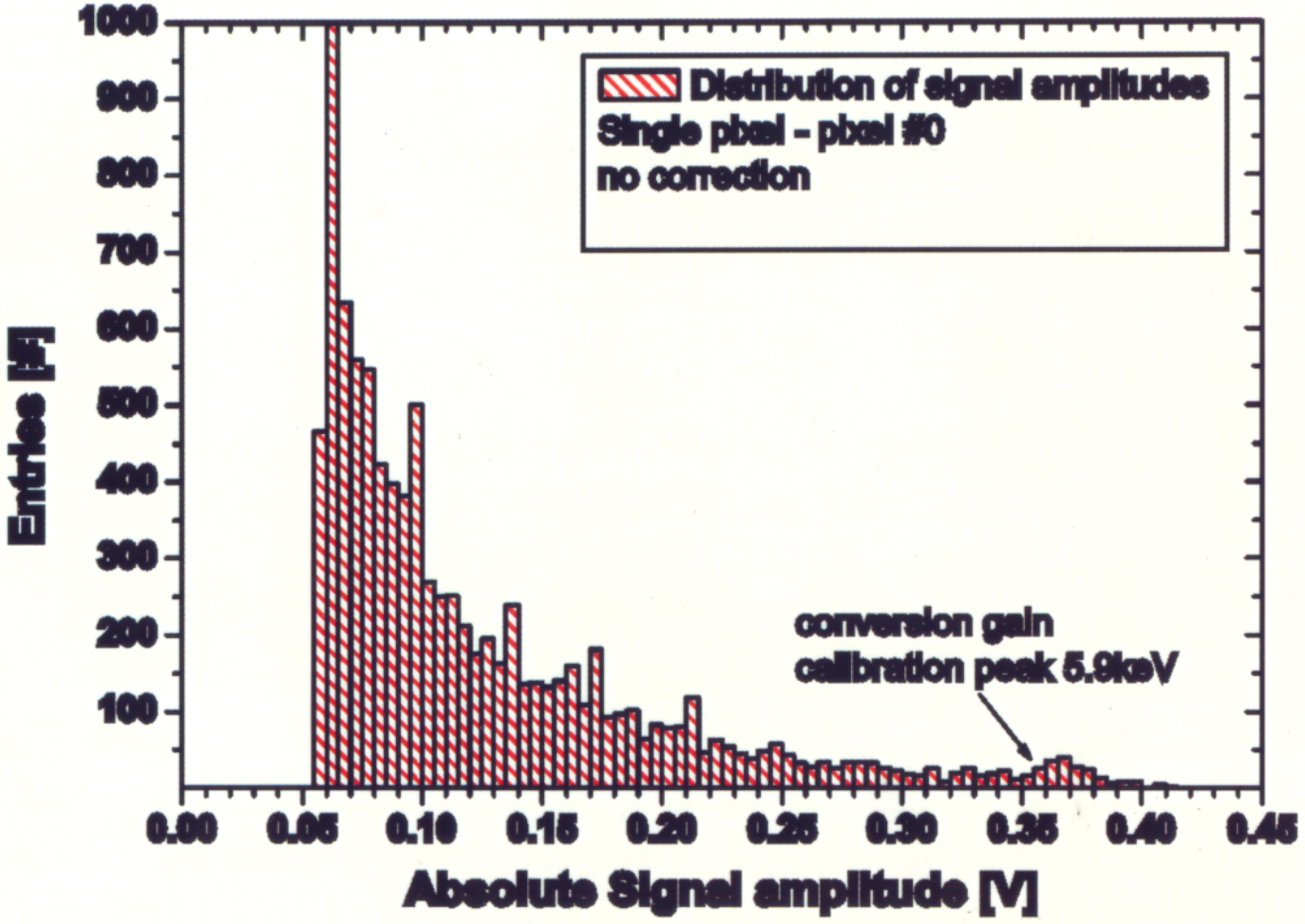
☑ MIMOSA VI - analogue part - preliminary results

☑ Differential output sampled during READ_OUT phase

Single pixel ^{55}Fe source spectrum (integration time = 77µs)

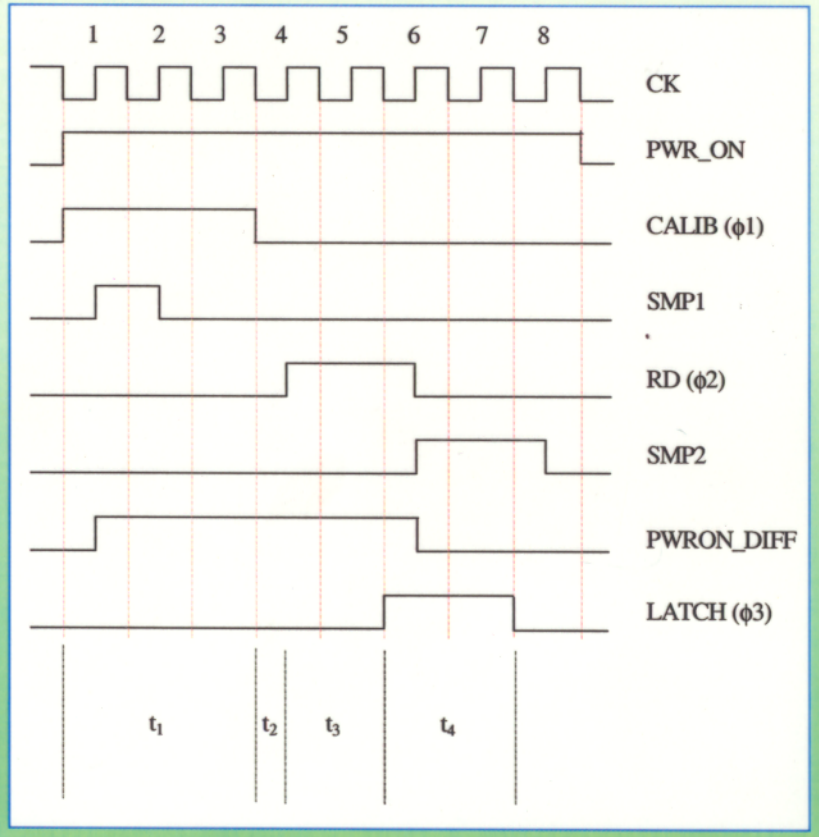


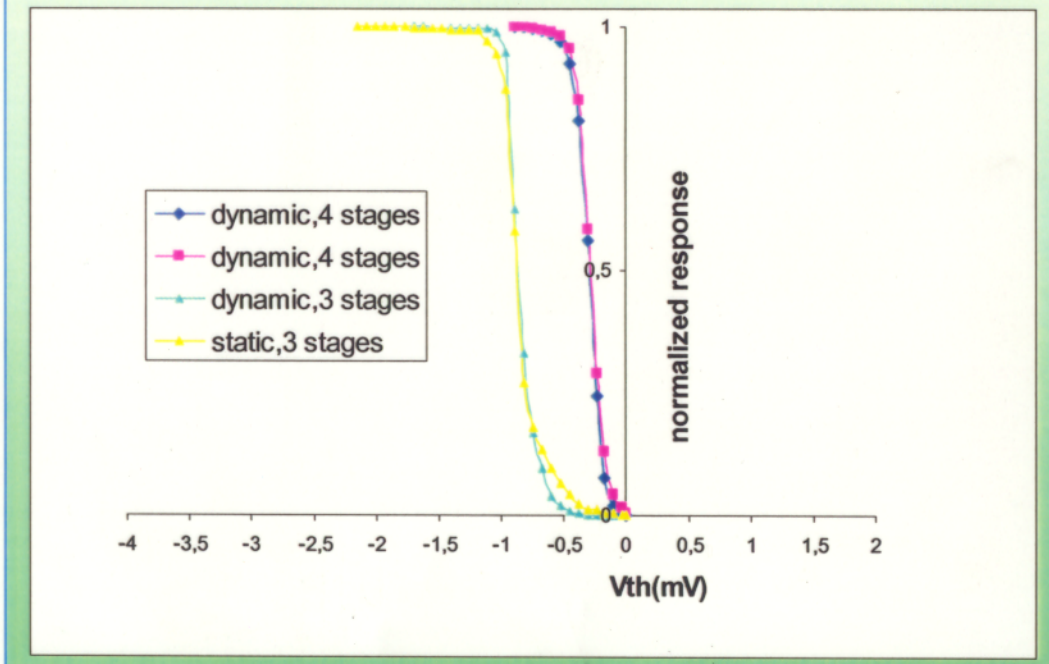
DISCRIMINATORS

DSM - DAPNIA

3 or 4 gain stages : operation on 8 clock cycles

conditions for the plot: fclk=40 MHz t1=75ns,t2=12.5ns,t3=62.5ns,t4=45ns

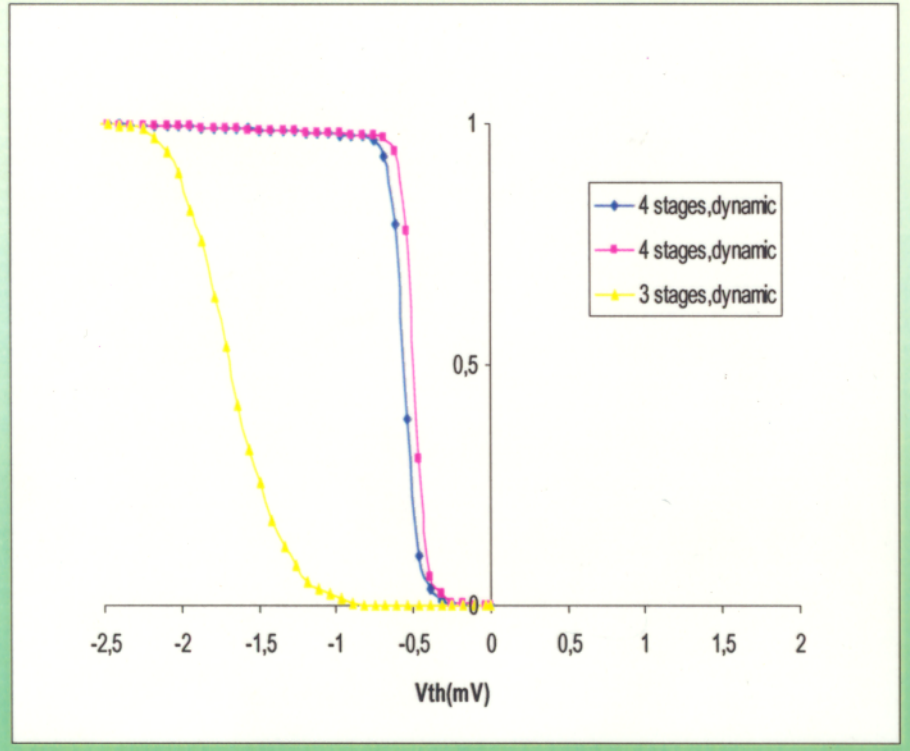




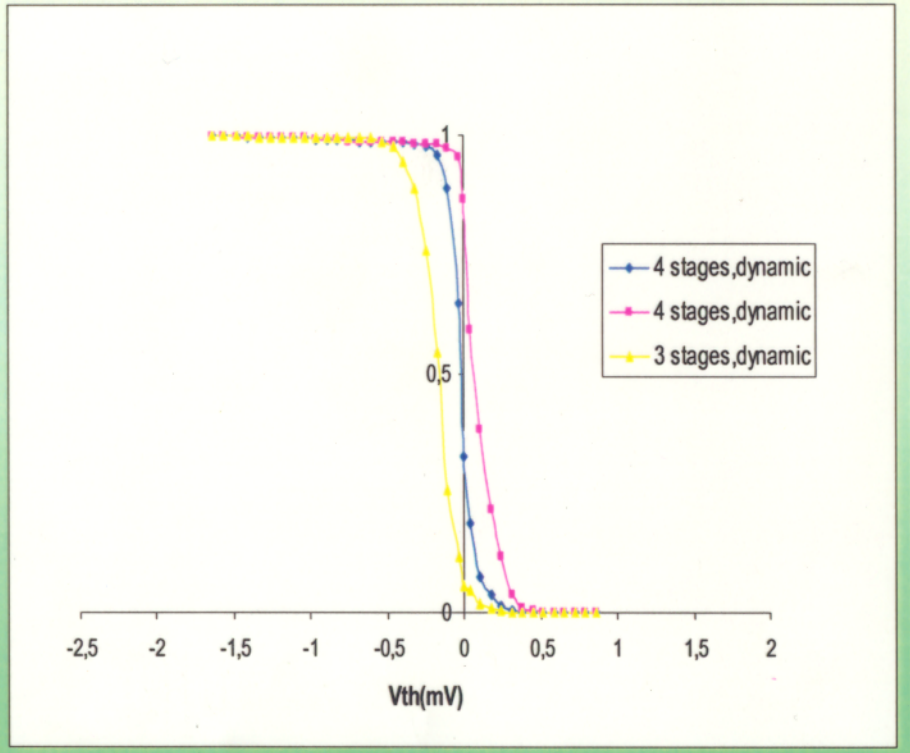
COMPARISON

DSM - DAPNIA

fclk=40 MHz,t1=60ns,t2=15ns,t3=45ns,t4=60ns



fclk=33 MHz,t1=90ns,t2=15ns,t3=45ns,t4=30ns



Summary: Plans for 2003

- MIMOSA-6: column // read-out and integ. signal processing
  - ◇ preliminary test results are satisfactory
  - ◇ tests at CERN-SPS in May-June

- MIMOSA-7: alternative signal collection & processing architecture (photoFET)
  - ◇ design under way in 0.35 μm AMS (8 μm epitaxy)
  - ◇ submission end of April $\rightarrow$ tests in Sept.-Oct.

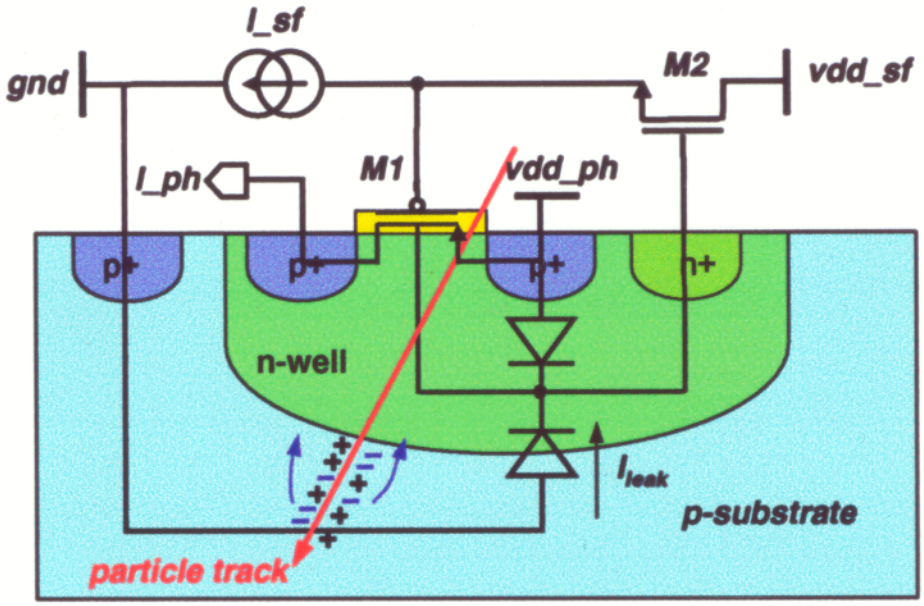
Fig. →

- System integration studies have started:
  - ◇ detailed effect of detector material on $\gtrsim$ 500 GeV physics
  - ◇ GEANT-4 description of CMOS Vx Det. started
  - ◇ pulsed powering studies with MIMOSA-5 in preparation
  - ◇ estimation of limit in $\overline{P_{diss}}$ without active cooling
  - ◇ achieve $\lesssim$ 50 μm thinning on real scale chip (MIMOSA-5)

Fig. →

- Studies based on physics processes $\rightarrow$ best compromise between granularity, signal proc. speed and mat. budget

photoFET operation



- e-h pairs generated at the neutral substrate and at the *n-well/substrate junction* affect the threshold voltage of the pMOS transistor

- Modulation of the transistor current is synonymous with **signal amplification** resulting in conversion of the generated charge to current.

- Advantages:
  - **Charge-to-current amplification**
  - High transconductance = **high sensitivity**
  - **Possibility of ganging current mode pixel outputs**

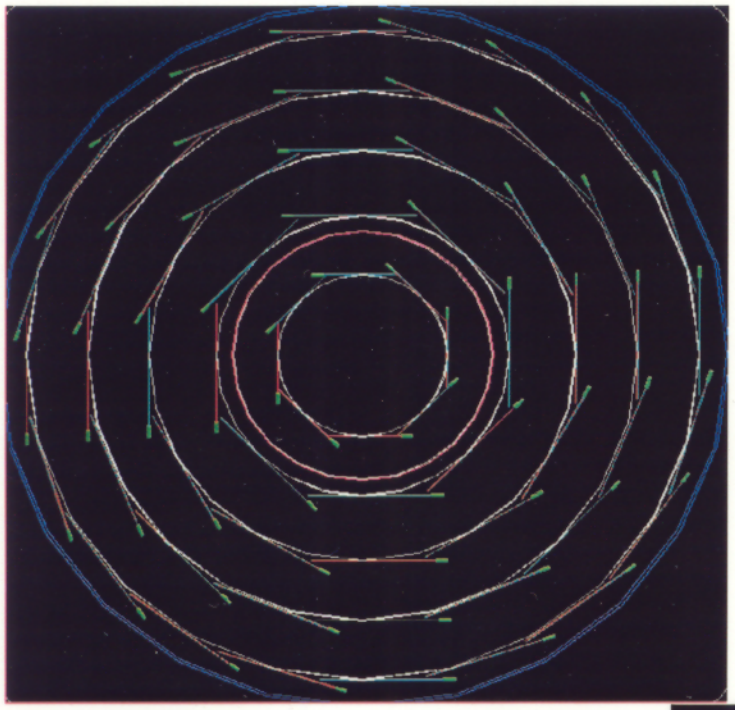
OPERATION MODES

- pMOS in **weak inversion** $V_T<0$
- pMOS in **strong inversion** $V_T>0$

First version of the Vx Det CMOS technology for MOKKA(GEANT4)

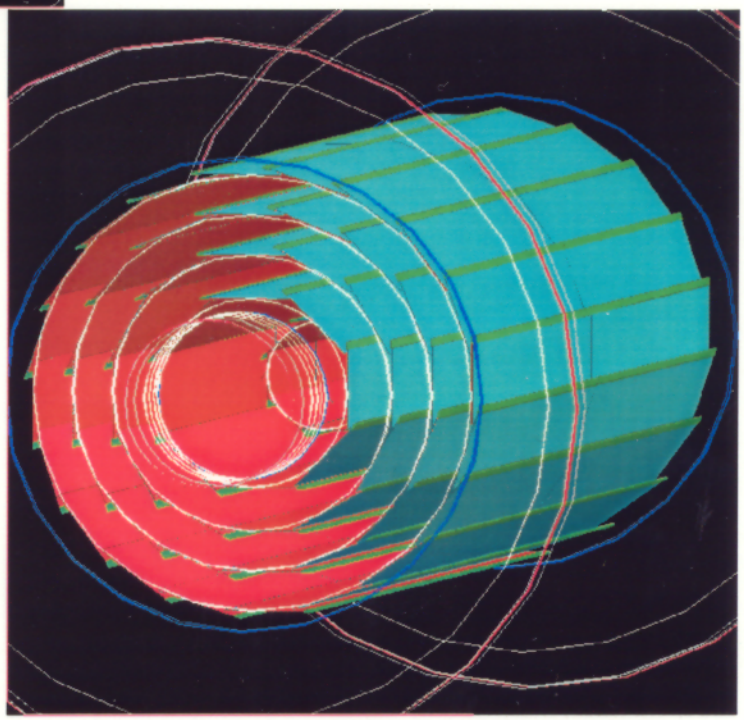
- Former version of the Vx Det.
  - CCD base line geometry
  - cylindrical layers
- Detector geometry with CMOS sensors
  - CCD base line geometry
  - 5 layers composed of planar rectangular ladders
    - layer #1 : 8 ladders, L = 100 mm , l = 13 mm , r = 15 mm
    - layer #2 : 2×8 ladders, L = 125 mm , l = 22 mm , r = 26 mm
    - layer #3 : 2×12 ladders, L = 125 mm , l = 22 mm , r = 37 mm
    - layer #4 : 2×16 ladders, L = 125 mm , l = 22 mm , r = 48 mm
    - layer #5 : 2×20 ladders, L = 125 mm , l = 22 mm , r = 60 mm
  - Readout electronic along the ladders l = 2 mm
  - Pixel pitch : 20 μm

View of the VXD in MOKKA



- 50 µm thick carbon fibre mecanical support
- 50 µm thick CMOS sensor
  - X/Xo ≈ 0.08 %

- Present Work :
  - tracking algorithm implementation
  - impact parameter resolution



- Caution ! This is just a starting point, the final geometry may be totally different.