

CAL SLT and Readout System

Work for the system done by:

Ph.D. Students: S. de Jong, H. v. d. Lugt^a, A. Kruse and H. Uijterwaal

Staff: H. Boterenbrood, J. Vermeulen and L. Wiggers

Electronic Department: G. Kieft, A. de Waard

Present responsibilities:

CAL TP readout: H. Boterenbrood

CAL SLT and ZGANA: L. Wiggers

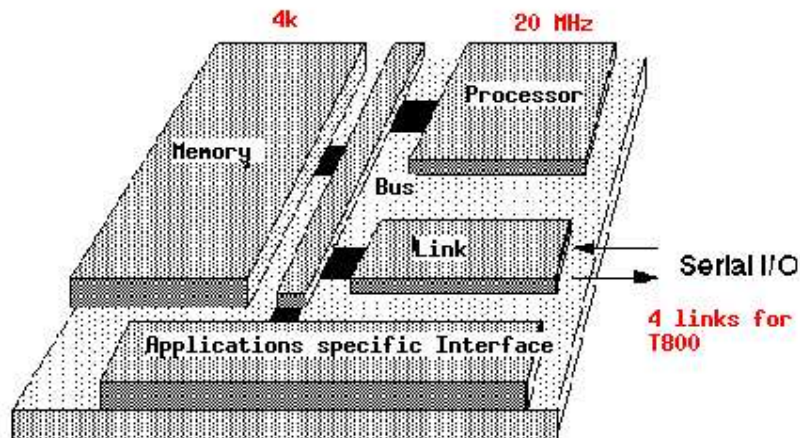
Index of the talk:

1. Transputer and initial ideas concerning readout and slt
2. Interface to Digital Card
3. TP Network
4. Subcomponents
5. CAL-SLT hw/sw and results
6. Error conditions
7. Future

Talk given on 11-3-98 for ZEUS CAL DQM group. See for transparencies: www.nikhef.nl/user/p63. See for more documentation about the CAL-SLT system: www.nikhef.nl/user/n48/zeus_doc.html. A few slides about Transputers and OCCAM are based on: <http://linus.socs.uts.edu.au/xputer/OccamFoils/course.html>.

^aThesis: "The Data-Acquisition and Second Level Trigger System for the ZEUS Calorimeter" (1993).

1 Transputer Introduction



INMOS:

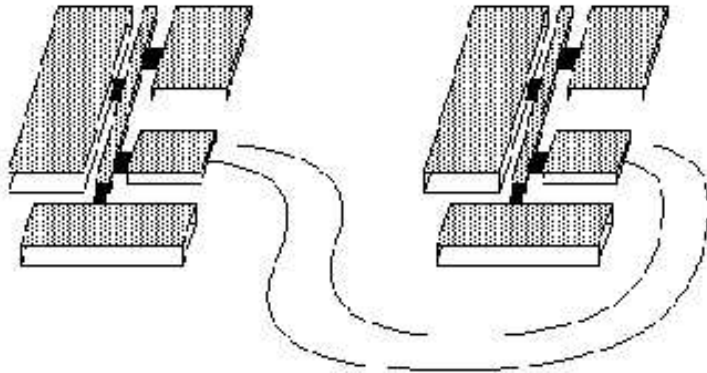
A member of the Transputer family consists of some, or all, of the following functional blocks.

- A fast, RISC-like processor
- On chip RAM
- Inter-processor serial communication links
- Application specific hardware interfaces

A member of the Transputer family could be either a microprocessor or a peripheral chip.

Low glue systems

The Transputer also has benefits in applications such as avionics, industrial control and robotics where packing density and reliability are important. The on chip memory controller minimises the amount of external memory control logic required, and the serial links only require two wires to connect to another processor.



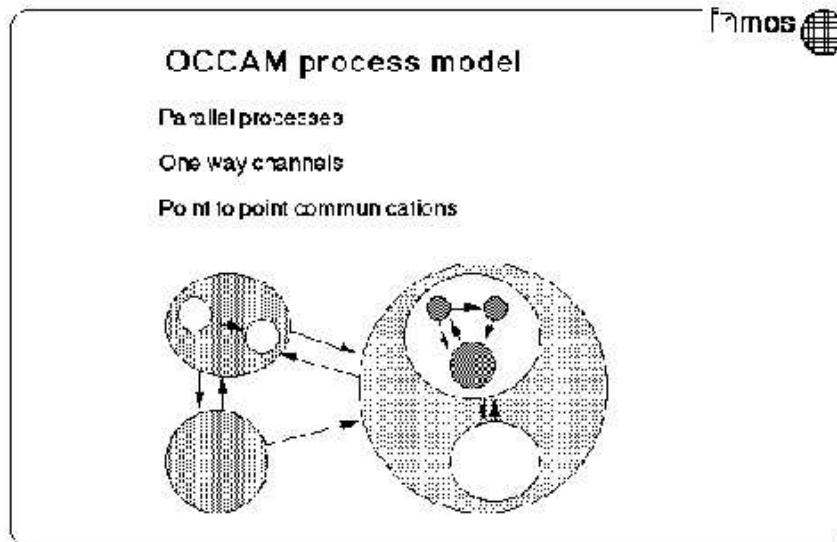
Clock frequencies within 200 ppm.

Clock phases may differ.

Serial links

Serial links have the advantage over shared busses in multiprocessor applications that, as the number of Transputers increase in a system, so does the communications and memory bandwidth. The amount of interconnect required by serial links is far less than a bus system and no extra logic or wiring is required to control the sharing of a buss.

Very large arrays of Transputers are very easily built and programmed, and will find applications in number-crunching add-ons for minicomputers, Artificial Intelligence, 5th generation machines, distributed systems, embedded control systems, supercomputers and fault tolerant systems.



OCCAM

Named after William of OCCAM

Occam's razor: "Entia non sunt multiplicanda praeter necessitatem", or: "Entities should not be multiplied beyond necessity"

Developed by INMOS, assisted by Prof. Tony Hoare at Oxford

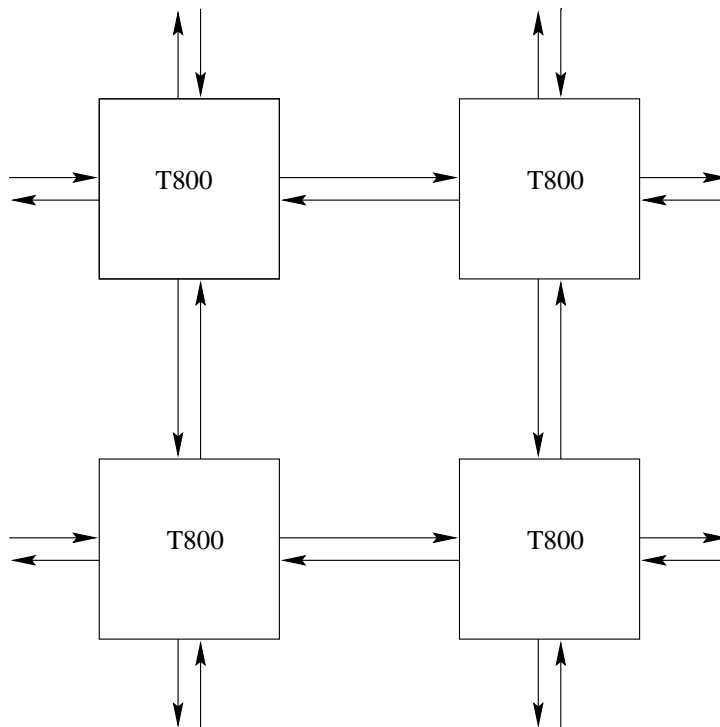
The Occam model of the world is of a number of independent processes or tasks on different machines is true parallel processing. To provide maximum speed with minimal wiring, the Transputer uses point-to-point serial communication links. Correspondingly, Occam uses point-to-point channels, and a message passing scheme between processes (DMA-driven data transfer).

Example of programming in the OCCAM language:

```
ALT
  count ? signal
  counter := counter + 1
total ? signal
SEQ
  out ! counter
  counter := 0
```

C compiler also available, but all Cal code written in OCCAM.

Physical Connections between Transputers using links:

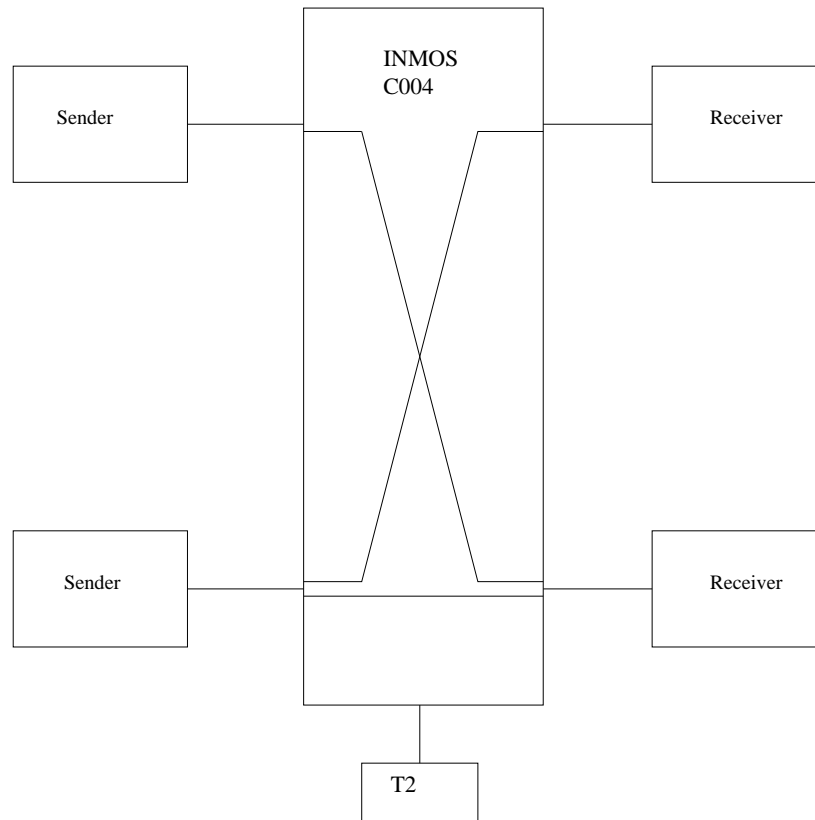


$$transfer - rate = 100 / (60 + [length(m)/5] \times 5) Mbyte/s$$

So 1.4 Mbyte/s for a 10 m link at 20 Mbit/s bit-rate.

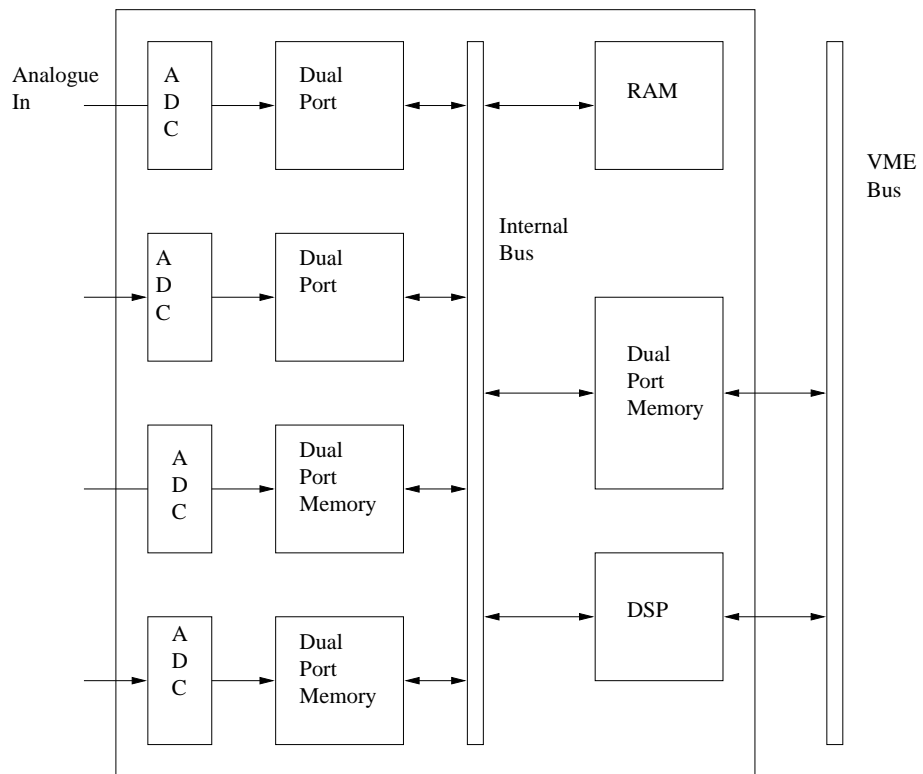
Cable type: shielded twisted pair. All cables inside the racks.

Making connections via the INMOS C004 Link Switch

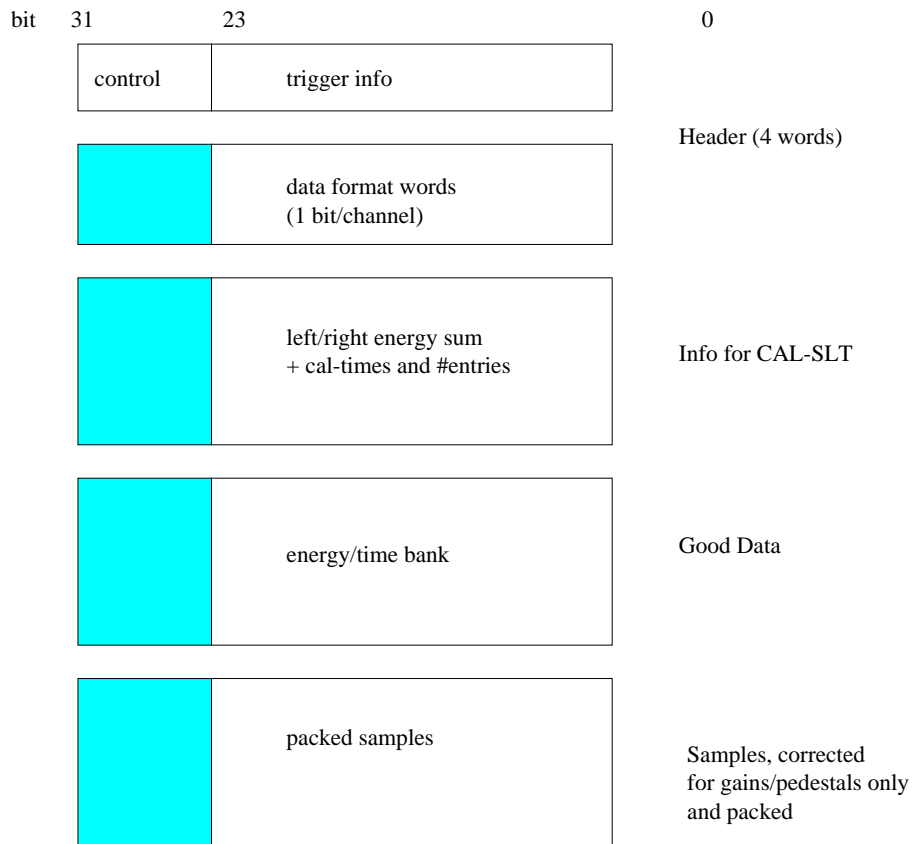


The Sender must signal to the T2 which connection it wants to make. The T2 sets the connection and disrupts it afterwards.

2 Digital Card



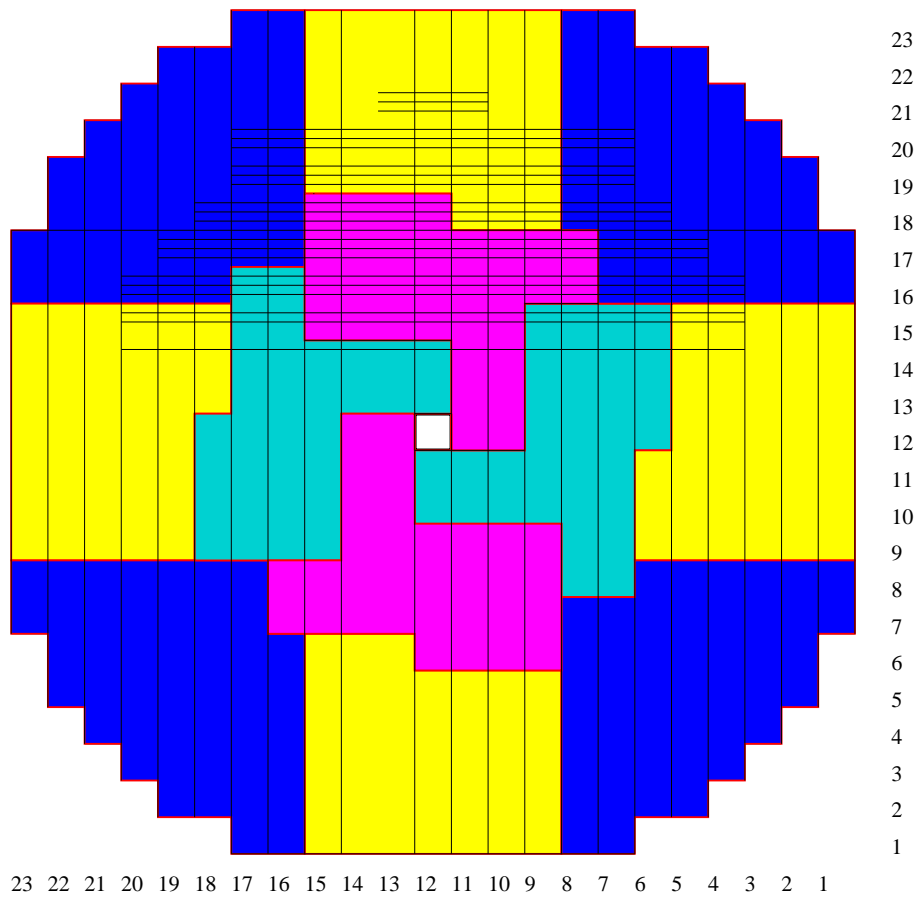
The DSP on the Digital Card processes the data from the ADCs and puts them in the Dual Port Memory, accessible via the VME-bus.



Format of a Page of the Digital Card.

First the CAL-SLT data is read after an FLT. The readiness of the Digital Cards is signalled to the 2TP-module via a linked interrupt. All other information is read after receipt of the GSLT decision. Afterwards the page is cleared by the 2TP-module for further use by the Digital Card.

Forward Calorimeter Mapping



The mapping of the CAL is such that each 2TP-Board processes a compact area.

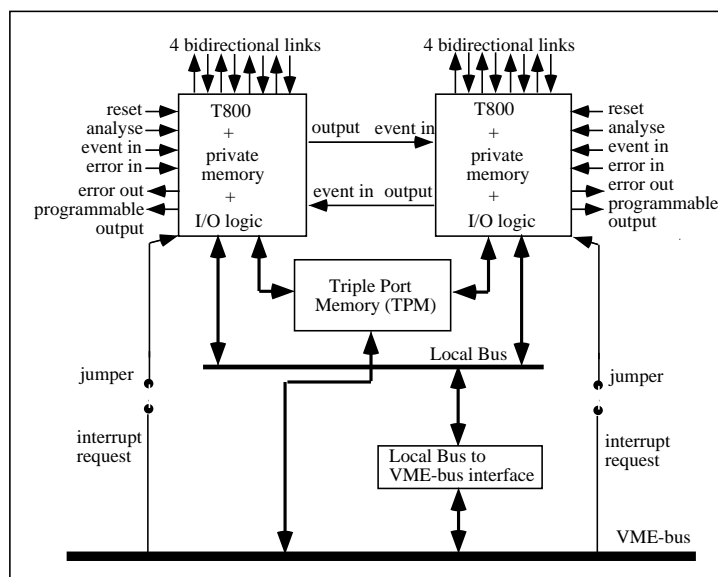
3 TP Network

Use of TPs in many systems:

- GFLT
- GSLT
- EVB
- CAL-FLT
- HES
- BMUON
- BAC
- CAL readout + SLT (+ many subcomponents)

→ modular system; easy to change

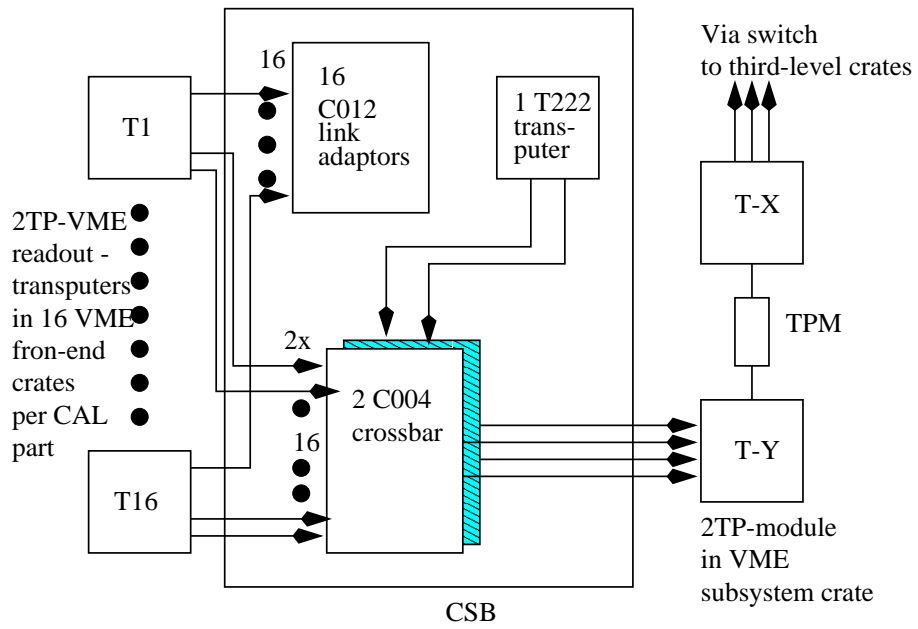
- 2TP-module^a ; link connections on link adaptor boards on VME backplane
- CSB (Control and Switch Box); modules for different functions, all connections on the back



2TP module: the transfer rate over the VME bus is 9-10 MByte/s, the T800 transputer runs at 20 MHz and has a processing power of 20 Mips and 1.5 MFlops.

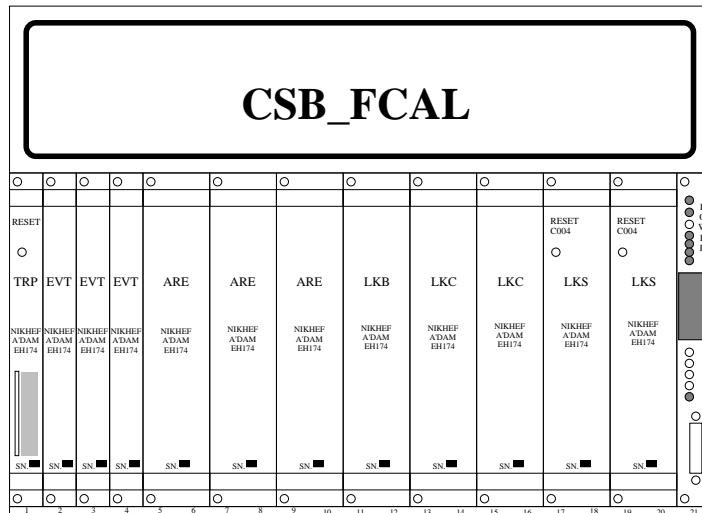
^aSee: NIM A332(1993)263-268

Schematic overview of the CAL-TP system



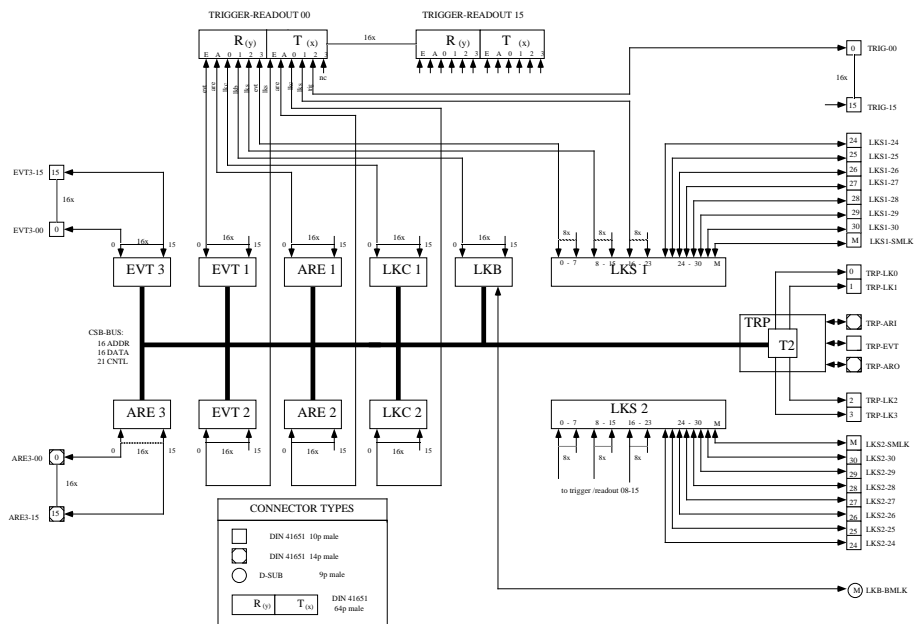
The system is partitioned per Cal part: one CSB per part. Most of the physical connections are laid within the CSB crate.

The CSB system



Front view of the
Control and Switch Box
for the
Forward Calorimeter
update: AW 060291

Front view of the FCAL CSB



Schematic overview of the FCAL CSB

BOARDS:

TRP-T2: Sets connections

EVT: handles 'Interrupts'

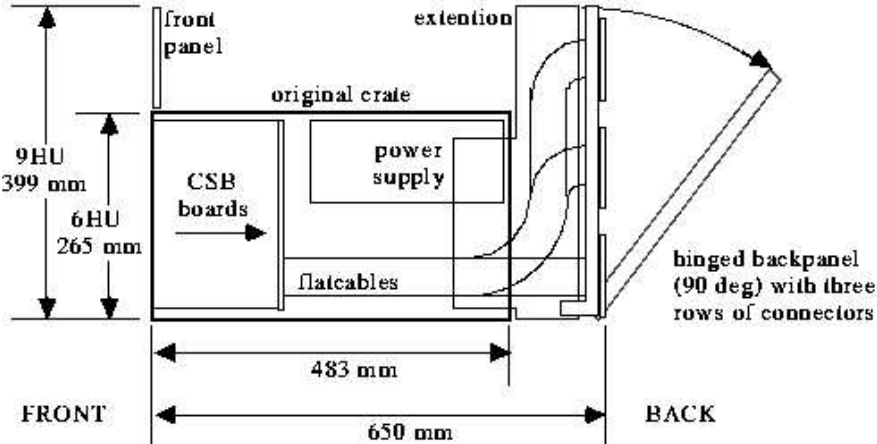
ARE: Analyse-Reset-Error Board

LKB: Link Broadcast Board

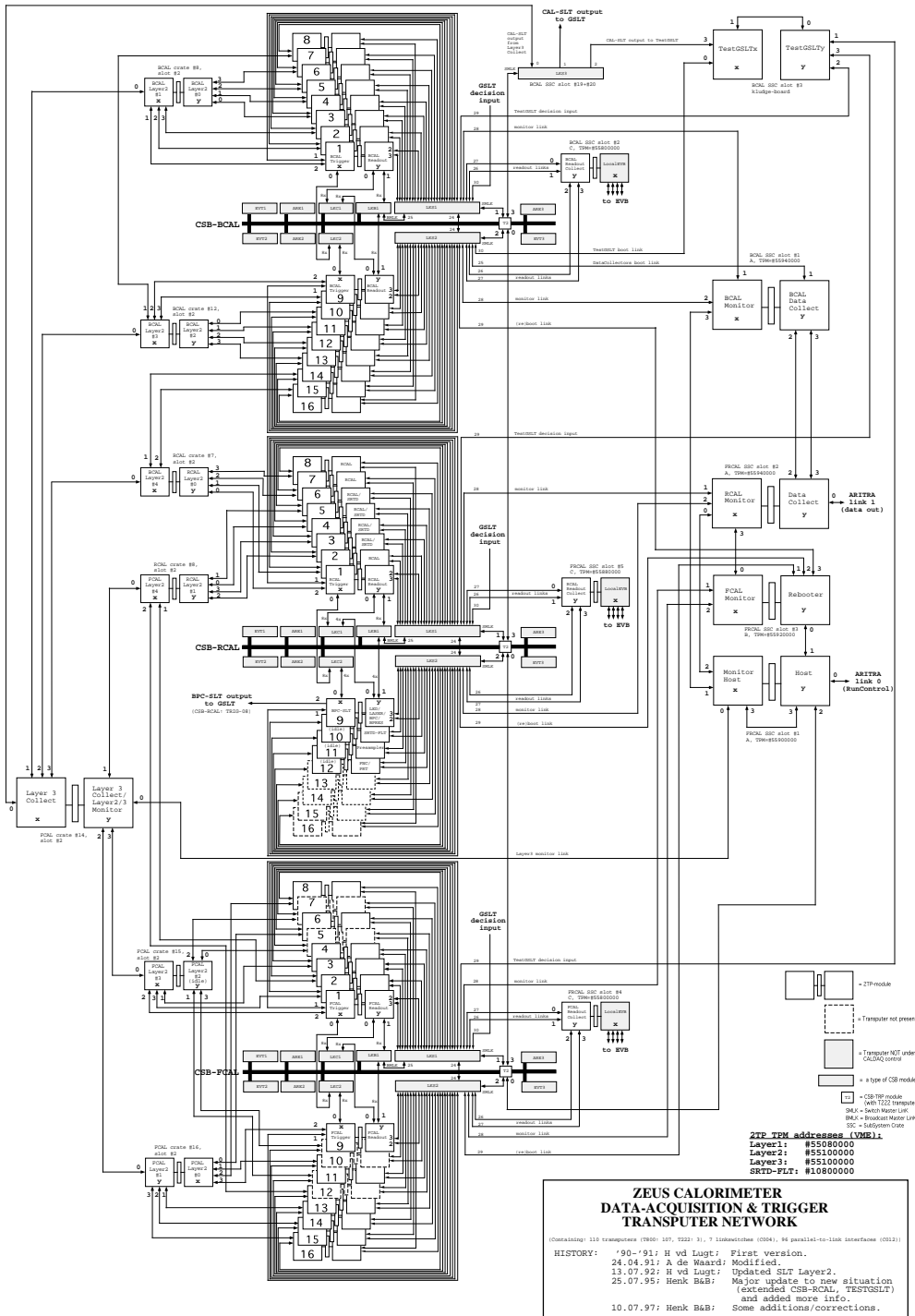
LKC: Command Link: 16 C012 Link Adaptors (Conn)

LKS: Switch Board

Side View CSB



NETWORK IN DETAIL: left part: trigger, right part: readout + monitoring connections.
 Connection to host: to ARITRA with extra 2TP module in ARITRA-VME slot, to the SUN via a CAPLIN TR801 SCSI verbinding.



4 Subcomponents

- Additions easy to make over CSB with 2TP modules: extra crates
- Mapping of Digital Cards in crates under software control
- Extra components: PRT, Presamples, SRTD, BPC, FPLUG, Laser System, FNC
- Increase in data volume in 1995 over 16 kbyte/event in RCAL (22 kbyte); limit to GSLT rate of 75-80 Hz
- Decreased data-volumes in 1996 by introducing CxPECO (compressed bank) besides the CxTene bank: about factor 2 reduction

5 CAL-SLT hw/sw and Results

5.1 Data and Strategy

Mapping of crates on CAL

Readout of limited data-set at GFLT rate

Digital Card provides:

- energy (left+right) per cell
- summed time + Npoints:
 - 2 thresholds: 200 and 2000 MeV
 - sum of the 2000 MeV entries has weight of factor 10 in average

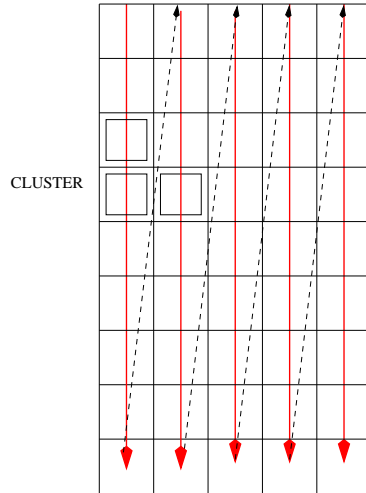
Output of CAL-SLT:

- energy sums : a) all CAL and b) FCAL inner ring
- F/R/B CAL time
- clusters: emc, hac , (muon)

Used in GFLT general vetos for

- spark rejection
- up - down time (to reject cosmics)
- fcal/rcal time and fcal time - rcal time
- E - Pz

and in physics filters.



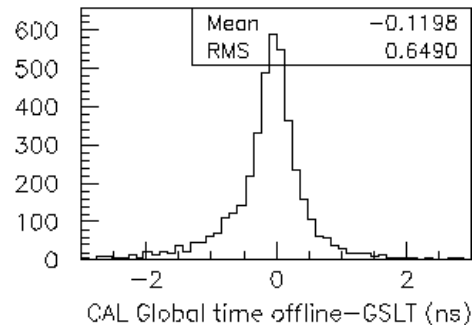
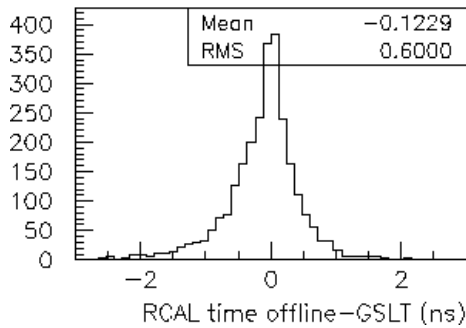
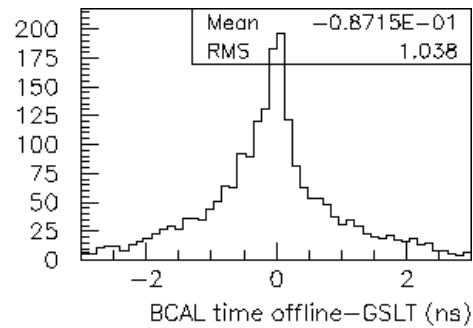
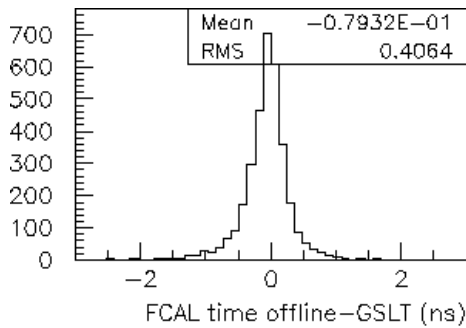
Scanning over the calorimeter cells.

Actions in processing:

- loop over grid
- if $E_{cell} > \text{threshold}$ THEN add to sums
- if $E_{cell} > \text{threshold}$ THEN start cluster
- if neighbour is part of cluster OR distance < 30 cm THEN add to cluster
- check E_{mc}/H_{ac} ratio
- combine clusters at level 2 and 3 IF distance < 30 cm

5.2 CAL-SLT Checks

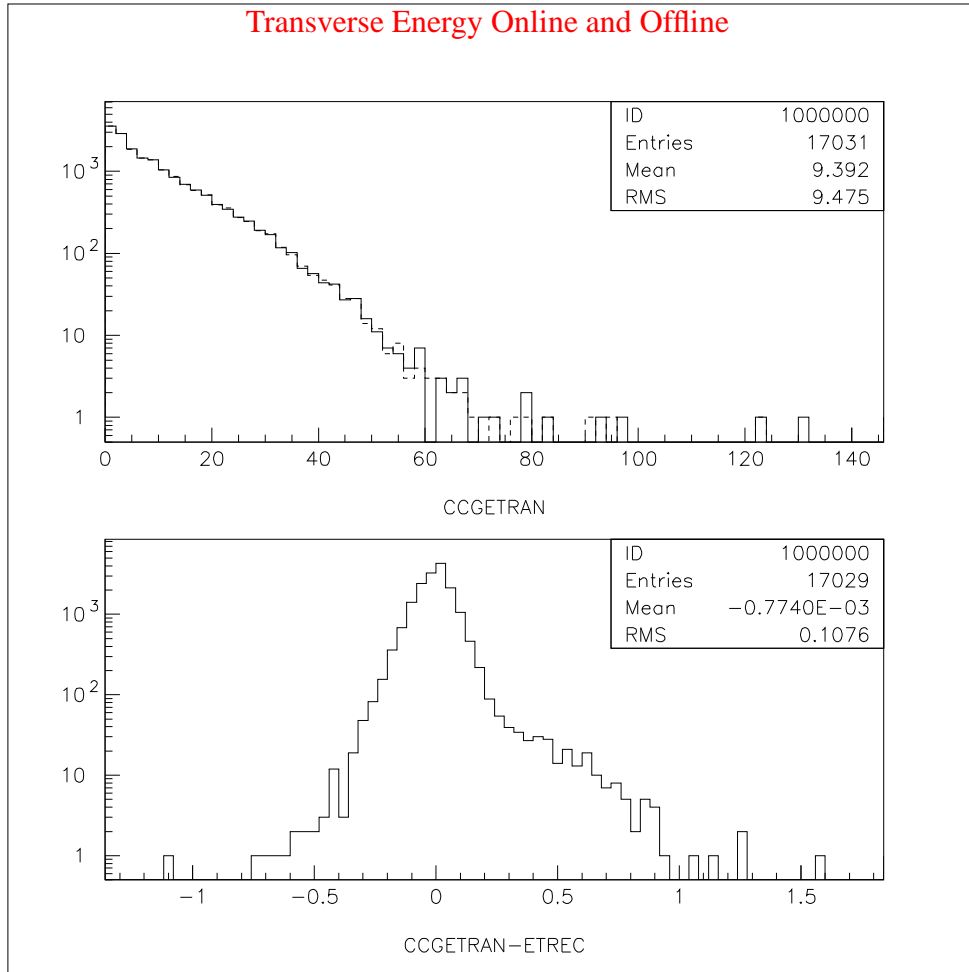
T-online -T-offline



Offline - Offline (ns)

The difference between online and offline results is less than 2 ns. To be safe the SLT cuts are set wider than at the TLT or offline (2 ns compared to the TLT cuts).

Transverse Energy Online and Offline



Online (solid) - Offline (dashed) (GeV)

Although the cell energies are calculated differently, the difference between online and offline values are minimal.

CAL-SLT Electron Finding Efficiency

In a study to check the cal-slt electron finder I used a dst tape and selected the different tlt electron finders. Then I looked whether I could find a cal-slt electron in the same theta-range. The other way around, I also looked when selecting the cal-slt electron, whether there was a tlt electron:

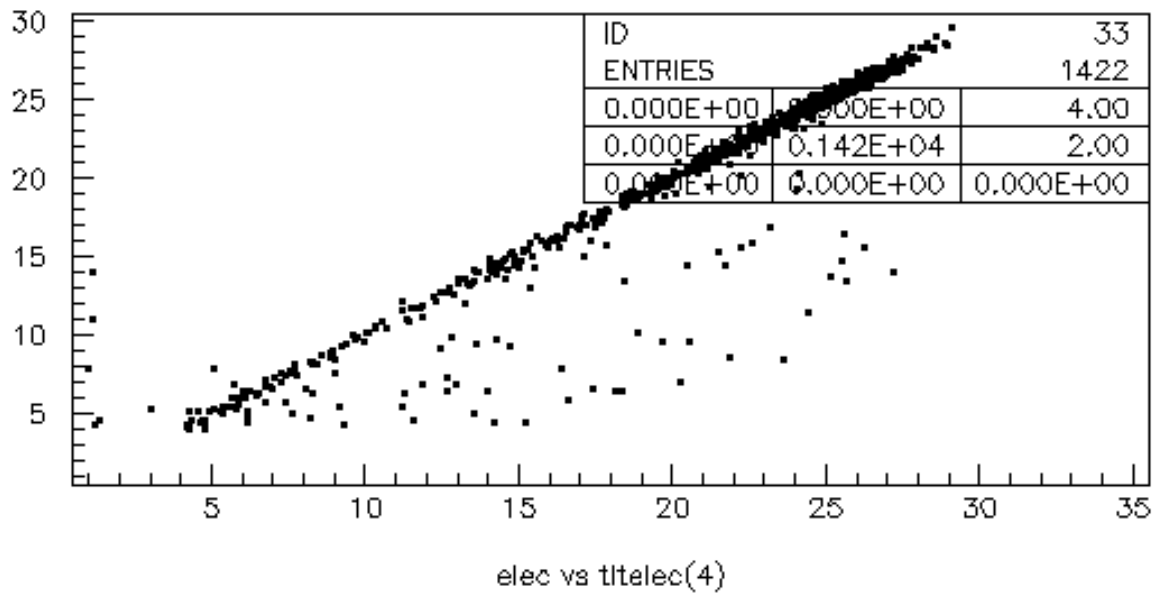
- total number of events: 17031,
- run: 25189 (970224),
- DST-tape without further selection.

cuts:

- cal-slt electron energy ≥ 2.5 GeV and $\theta \leq 0.5$,
- tlt electron energy ≥ 3 GeV , probability (if appropriate) ≤ 0.75 and
- $0.5 \leq \theta \leq 3.1$,
- *if selection on tlt electron then cal-slt electron should be within 0.1 rad of tlt electron.

condition	cal-slt*	cal_slt	tlt1	tlt2	tlt3	tlt4	flt iso-e	golden nc	exo nc 4
cal-slt electron	-	4679	1939	2808	2779	1418	4289	1068	1256
tlt1-electron	1938	1939	1943	1859	1909	1350	1942	693	695
tlt2-electron	2722	2808	1859	3000	2416	1357	2882	904	1045
tlt3-electron	2735	2779	1909	2416	2814	1387	2789	961	1042
tlt4-electron	1417	1418	1350	1357	1387	1421	1418	487	497
flt iso-e	-	4289	1942	2882	2789	1418	5511	1156	1264
golden nc bit	-	1068	693	904	961	487	1156	1175	632
exo nc 4 bit	-	1256	695	1045	1042	497	1264	632	1330

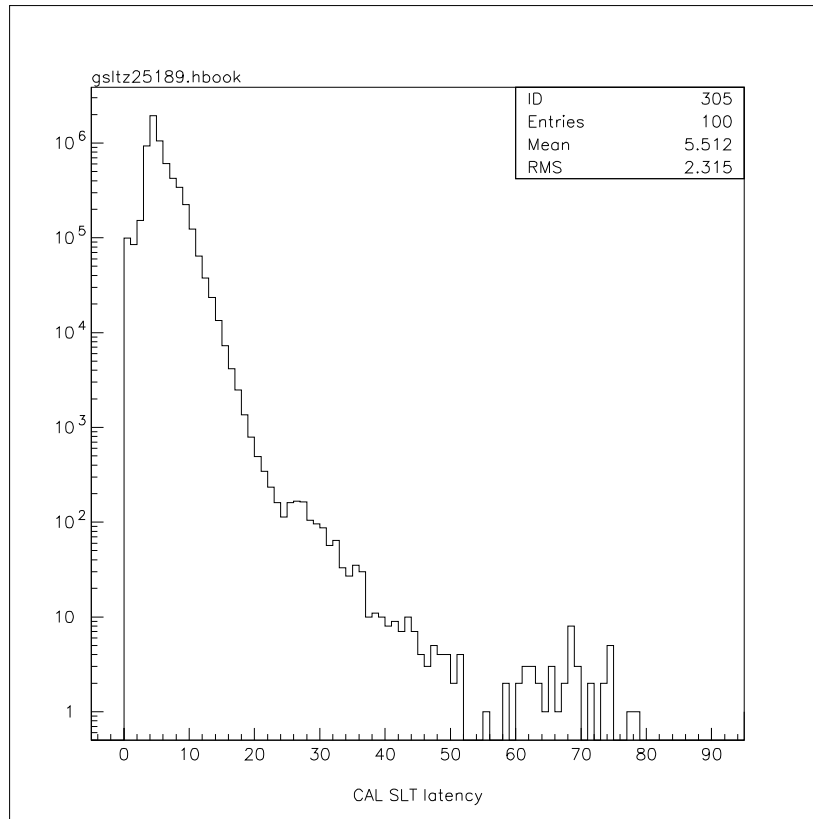
Results per event (the 4 tlt electron finders are: Elec, Local, Sinistra and Emille).



Cal-Slt electron energy vs. TLT Emille electron energy (tltelec(4)). The cal-slt electron had to be within 0.1 rad from the tlt electron. If no cal-slt electron was found, the cal-slt electron energy was set to 1 GeV.

The efficiency to find the Emille electron within 0.1 mrad is: $eff > 99.7$

5.3 CAL-SLT Latency



Latency of CAL-SLT: time between GFLT decision and arrival of CAL-SLT decision at GSLT in ms. The mean latency is 5-6 msec, built up sequentially in the three CAL-SLT layers.

CAL-SLT Processing Times as determined in a special run in 1996:

	FCAL	RCAL	BCAL
Layer-1	1260	960	1100
Layer-2	1250	880	920
Layer-3	-	1480	-

Maximum time for processing step per layer in microseconds. The reciprocal of this value gives the maximum throughput.

6 Error Conditions

HW (not that frequent):

- bad soldered connections
- burn-out of 2TP module in 1997
- burn-out of 3 CSB modules in 1998 (FPC cable badly connected to CSB?)

Repair of TP modules by INCA

Repair of CSB modules at NIKHEF

Be careful: no live insertion and no plastic wrapping of modules!

We have spares but they have to last till end 2005! No transputer made anymore, salvage 2TP modules from ending experiments at NIKHEF-K (nuclear section).

SW

TP system produces error messages for the CAL readout; but not always TP system is the culprit. Sometimes it is difficult to pinpoint the error.

Example of a frequent error in 1997, erroneously ascribed to the CAL:

- GFLT blocks; no data from GSLT (message)
- GSLT: no data from CAL-SLT (plot)
- CAL readout and cal-slt stopped (message in log-file)
- EVB stopped; local EVB buffer full

Log File:

```
>>>> FCAL ROCOLLECT STATUS<<<<
head.ptr, tail.ptr =      16403      16403
calec.tail         =      16403
space.requirement  =       2270
evb.events.written =      75020
data.len           = 294,265,266,270
trigger.no        = 74992,74992,74992,74992
```

```
>>>> BCAL ROCOLLECT STATUS<<<<
```



```
head.ptr, tail.ptr =      49394      46841
calec.tail          =      49394
space.requirement   =       2553
evb.events.written  =      75004
data.len            = 168,194,170,182
trigger.no          = 75018,75018,75018,75018
```

```
>>>> RCAL ROCOLLECT STATUS<<<<
```

```
head.ptr, tail.ptr =      28119      28119
calec.tail          =      28119
space.requirement   =       3494
evb.events.written  =      75021
data.len            = 183,186,546,820
trigger.no          = 75019,75019,75019,75018
event.no(collector)=   -9,75019,   -9,   -9,   -9,   -9,   -9
event.complete      = #0000,#0AD7,#0000,#0000,#0000,#0000,#0000
```

```
LAYER3MON: PEDESTAL trigger 374681
```

```
LAYER3MON: UNO trigger 374682
```

```
LAYER3MON: LED trigger 374683
```

```
LAYER3MON: LASER trigger 374684
```

```
LAYER3MON: PEDESTAL trigger 375331
```

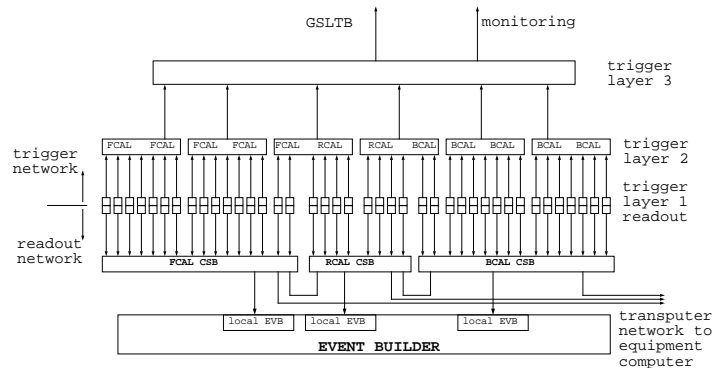
```
FCALEXP: CALDAQ blocked, output buffers to EVB full
```

```
BCALEXP: CALDAQ blocked, output buffers to EVB full
```

```
RCALEXP: CALDAQ blocked, output buffers to EVB full
```

[Test programs by Henk Boterenbrood: www.nikhef.nl/user/n48/zeus_doc.html](http://www.nikhef.nl/user/n48/zeus_doc.html)

7 Future



all connections of calorimeter readout and 2nd level trigger

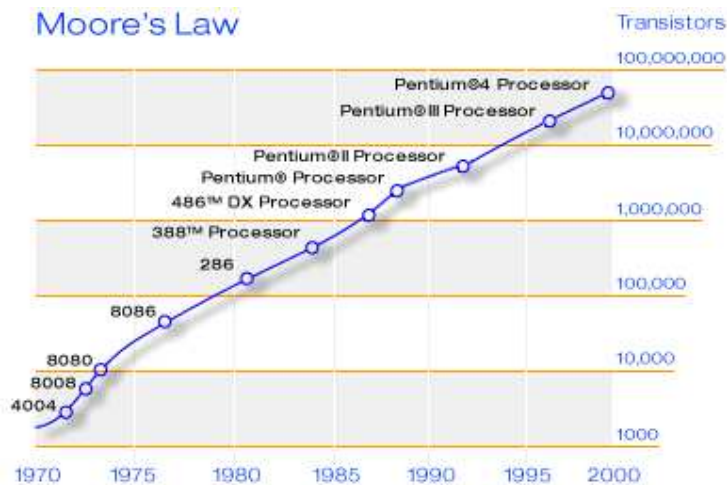
Limit in EVB connections about 110 Hz (good enough), but limit in CAL-SLT rate: 550-650 Hz.

Update (replacement of layer2 and layer3 transputers) in principle could be interesting if:

- We can use standard TP-PCI connections
- The cpu power of a new processor is $3 \times 40 \times 10 = 1200Mips$

Then the throughput and latency should be OK.

New powerful INTEL chips available running at > 1 GHz, still fulfilling Moore's law:



Moore's law for INTEL processors. But time and manpower