

Production Readiness Review of the MDT ROD

Electronic Design Details

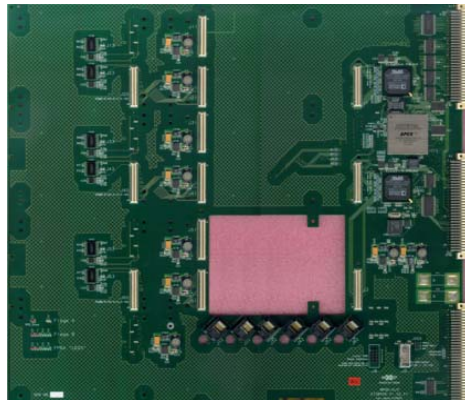
MROD-X Design, Changes with respect to the MROD-1 design

MROD-1

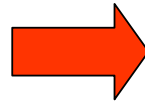
3x



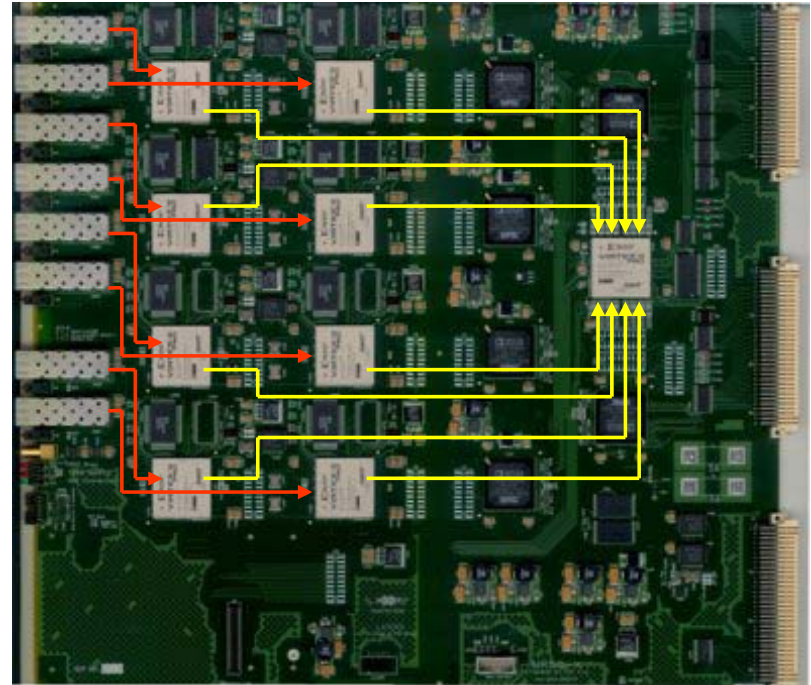
+



SHARC links used for data transport



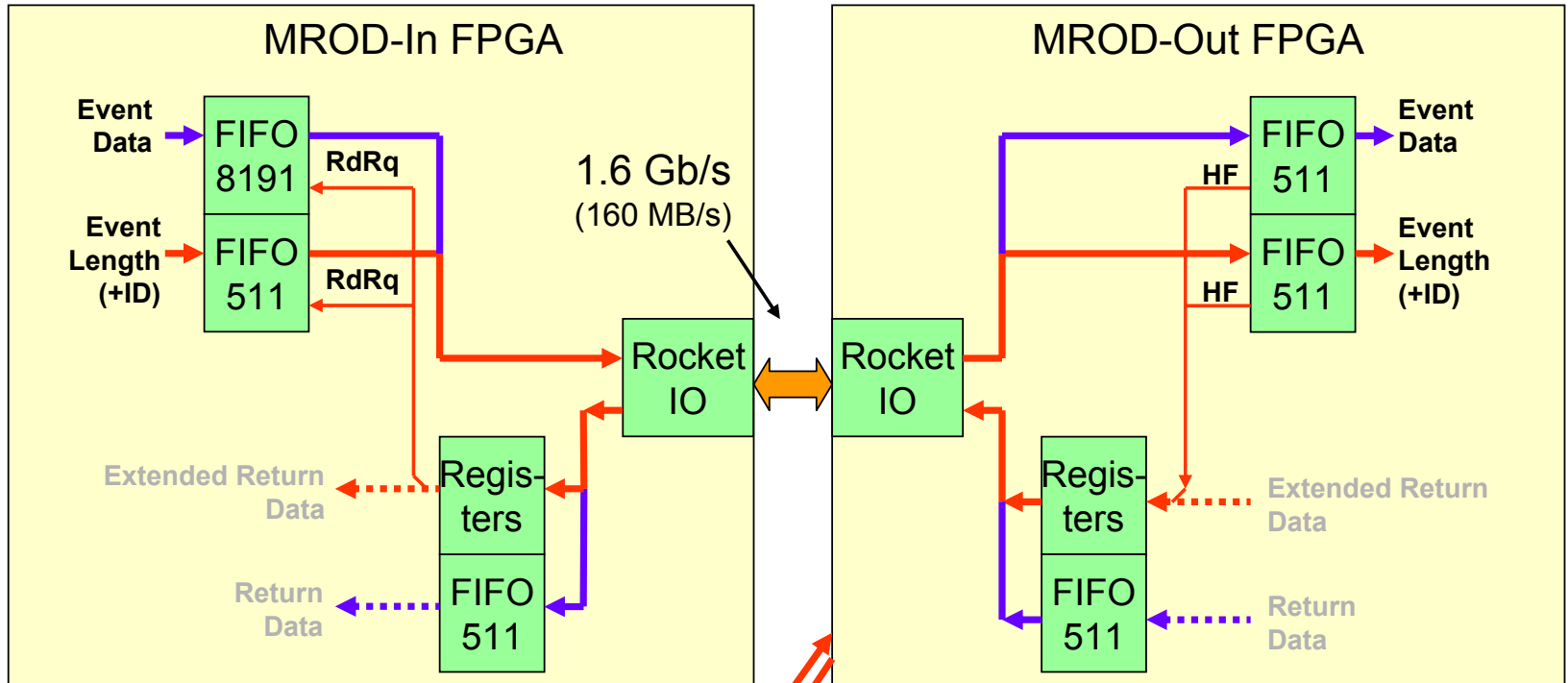
MROD-X



RocketIO links used for data transport

RocketIO

between MROD-In and MROD-Out FPGAs

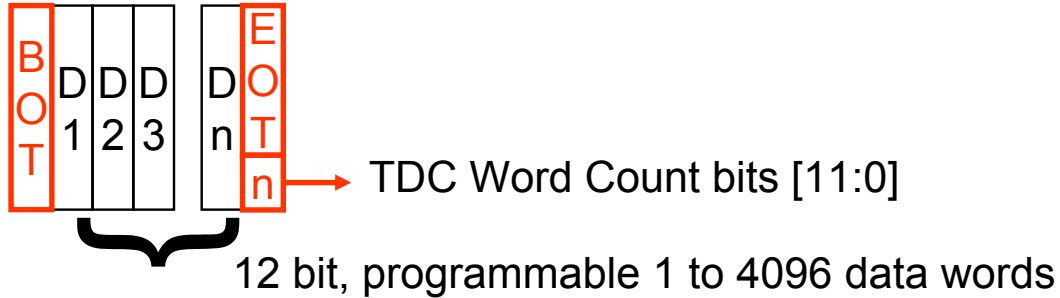


- High Priority Path
- Low Priority Path

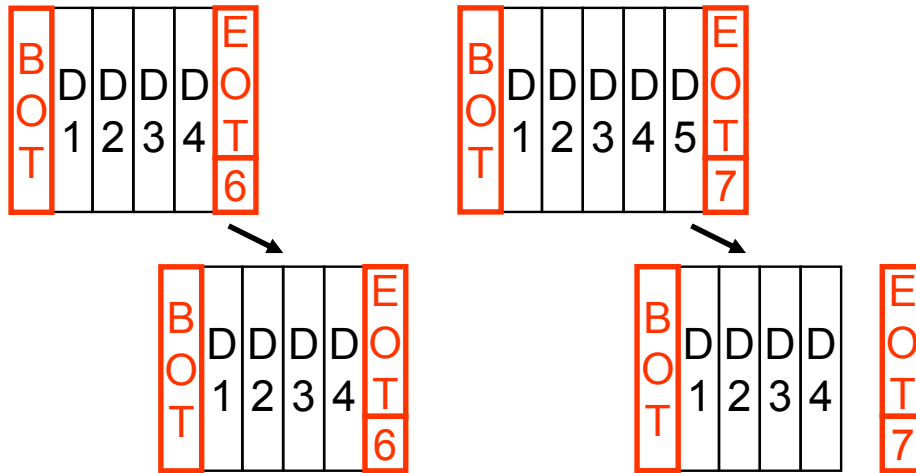
Connections from other
7 MROD-In FPGAs

- Backpressure
- 8B/10B
- Extended Data
- Length Look-ahead
- TDC Limit

TDC Limit Register



Example when limit is set to 4:

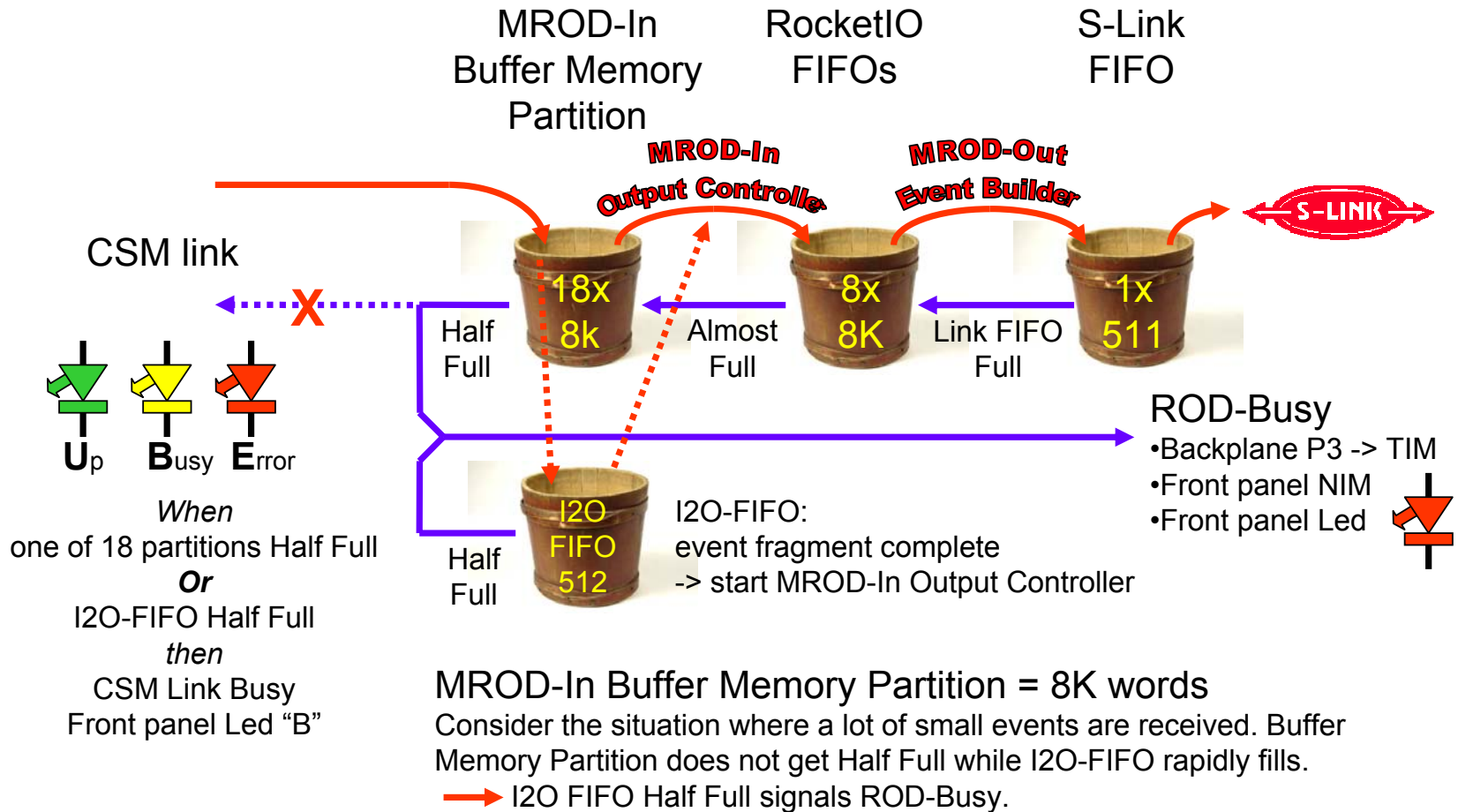


No shutdown as with “Maximum Event Length”
(Default 1K words)

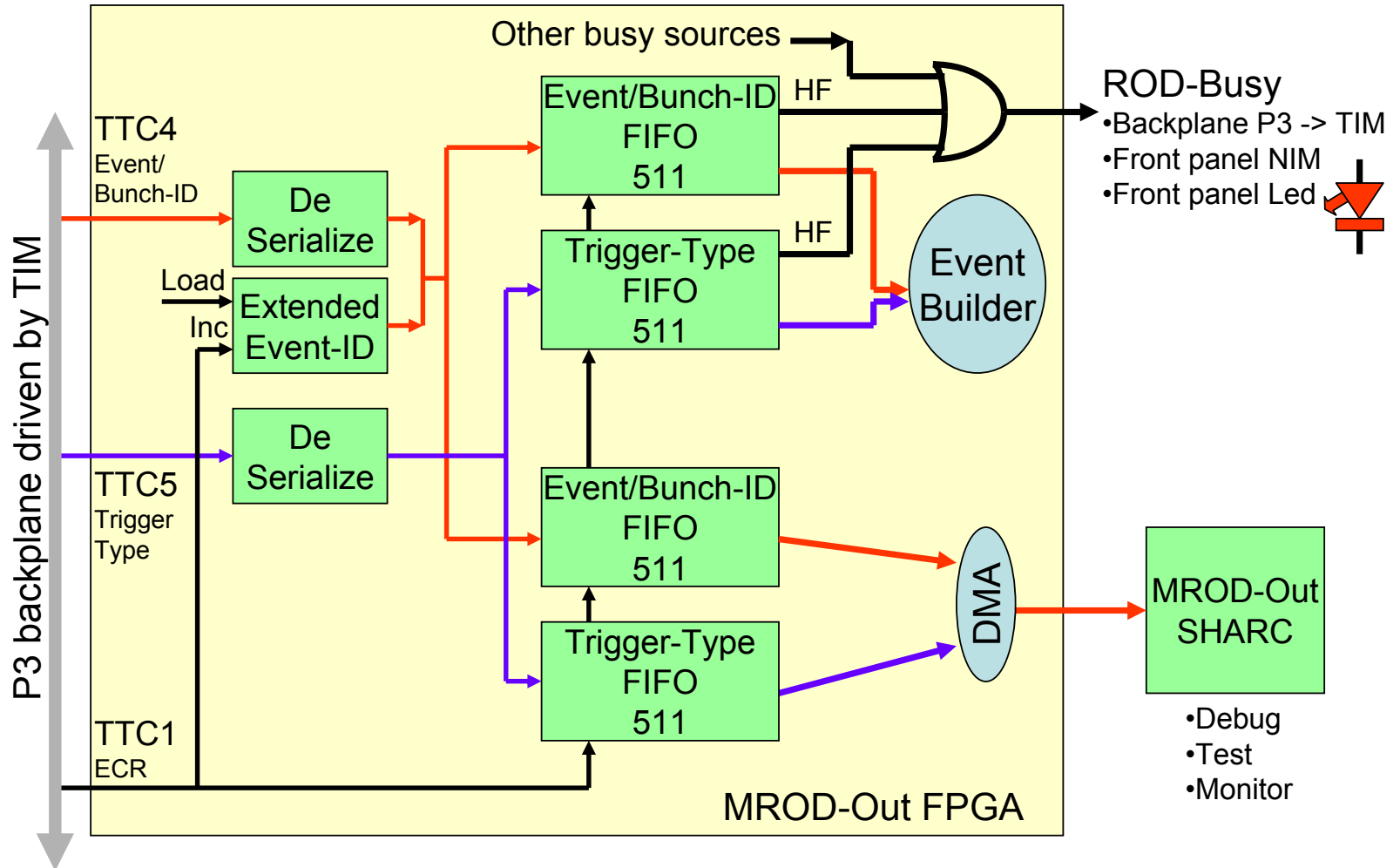
Register default = 0x60
Maximum Event Fragment
for 18 TDCs:
 $18 \times (\text{BOT} + 96 + 1 \text{ EOT}) =$
1782 words

MROD-Out, Event Builder:
Maximum Event Fragment
 $8 \times (1782 + 4 \text{ envelope words}) =$
14288 words

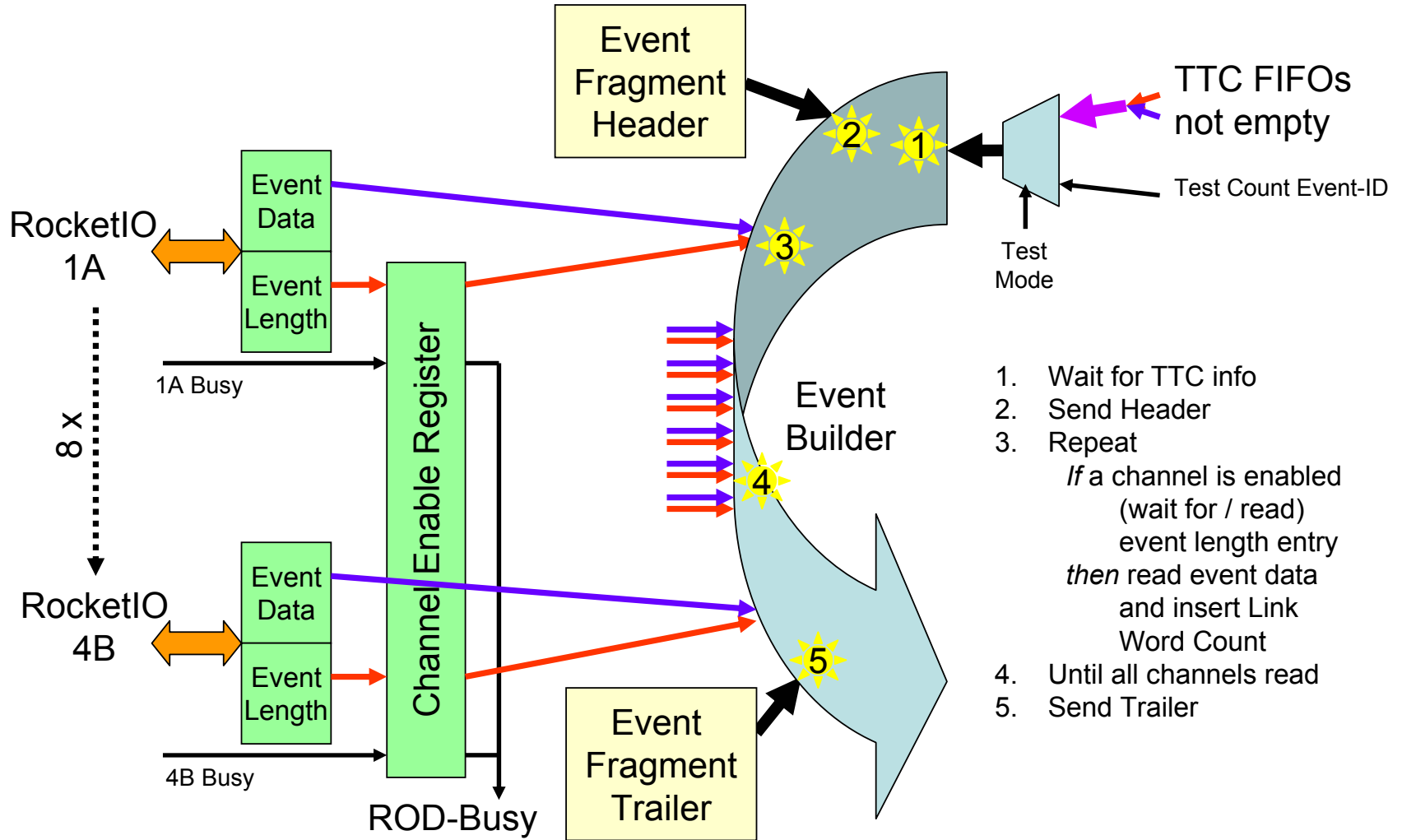
Backpressure and ROD-Busy



TTC FIFOs



Event Builder (1)



Event Builder (2)

Event Fragment Header

- BOF (S-Link Control Word) 0xB0F00000
- Header Marker 0xEE1234EE
- Header Size 0x00000009
- Format Version Number (VME register) 0x03000000
- Module ID (VME Register) 0x00610080
- Run number (VME Register) 0x00000000
- Event -ID 0xEEeeeeee
- Bunch-ID 0x00000bbb
- Trigger-Type 0x00000tt
- Detector Event Type (VME Register) 0x00000000
- MROD BOB 0x80eeeeee

Test Mode

Normal Running

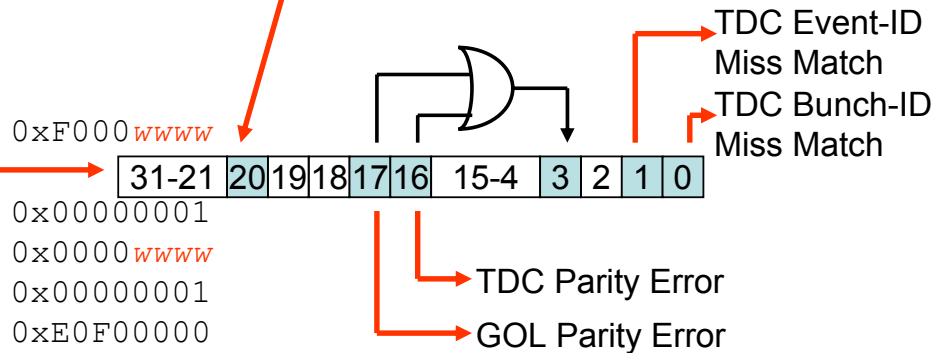
eeeeee = from TTC

Test Mode (run without TTC)

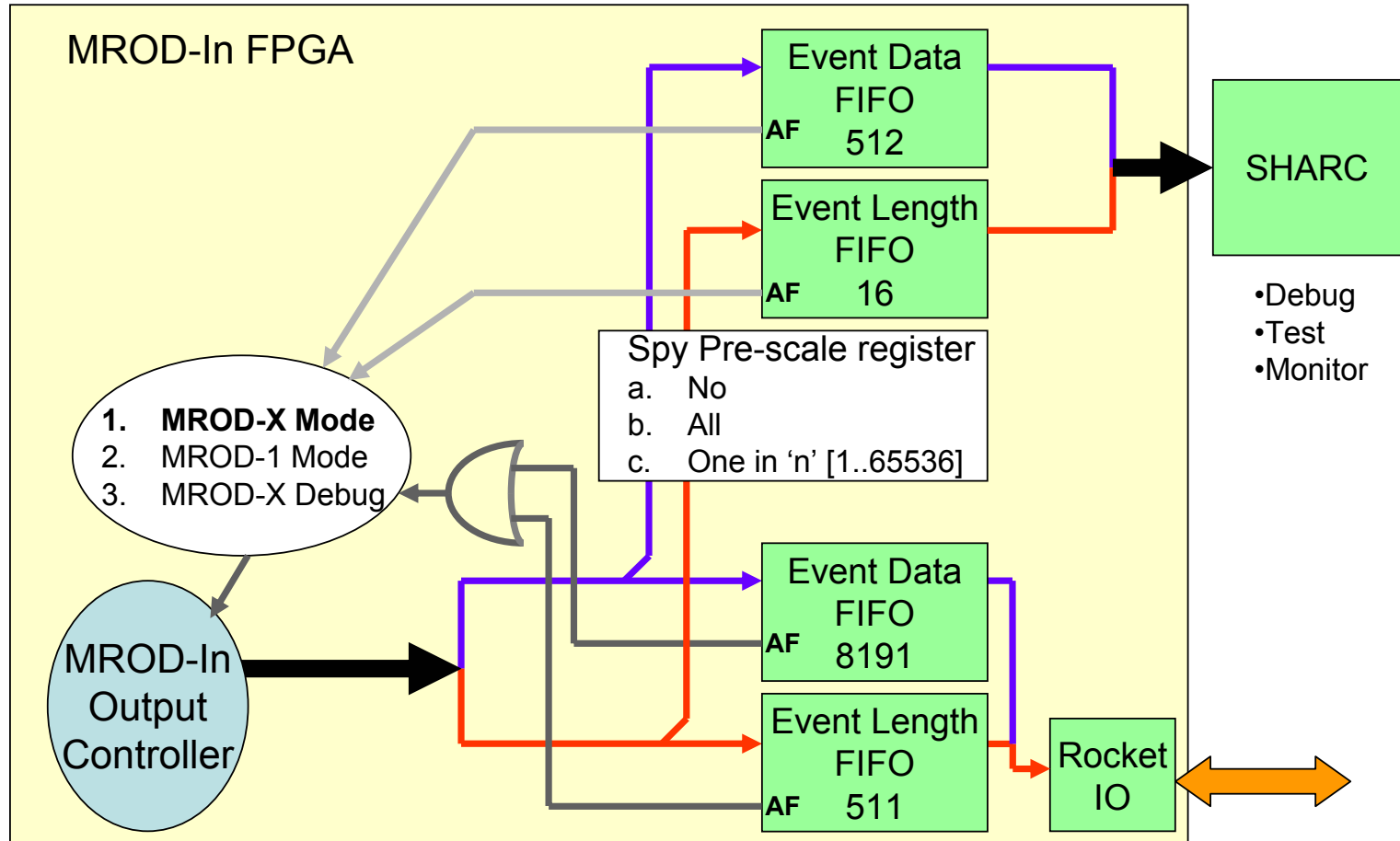
eeeeee = from Test Counter

Event Fragment Trailer

- MROD EOB 0xF000www
- MROD Status word (MSE1) 0x00000001
- Number of Status Elements (NSE) 0x0000www
- Number of Data Elements (NDE) 0x00000001
- Status Block Position 0xE0F00000
- EOF (S-Link Control Word)

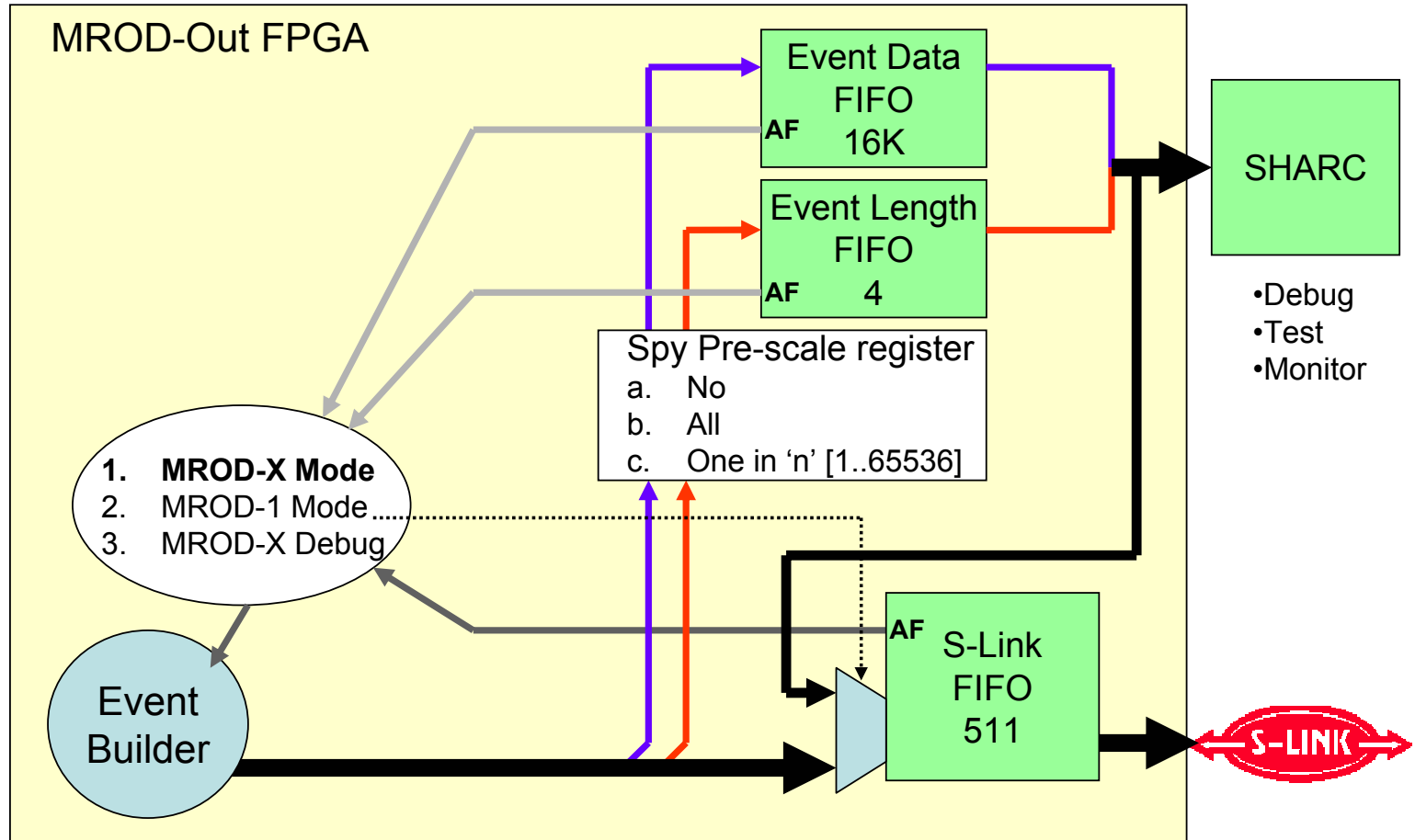


Spy (MROD-In)



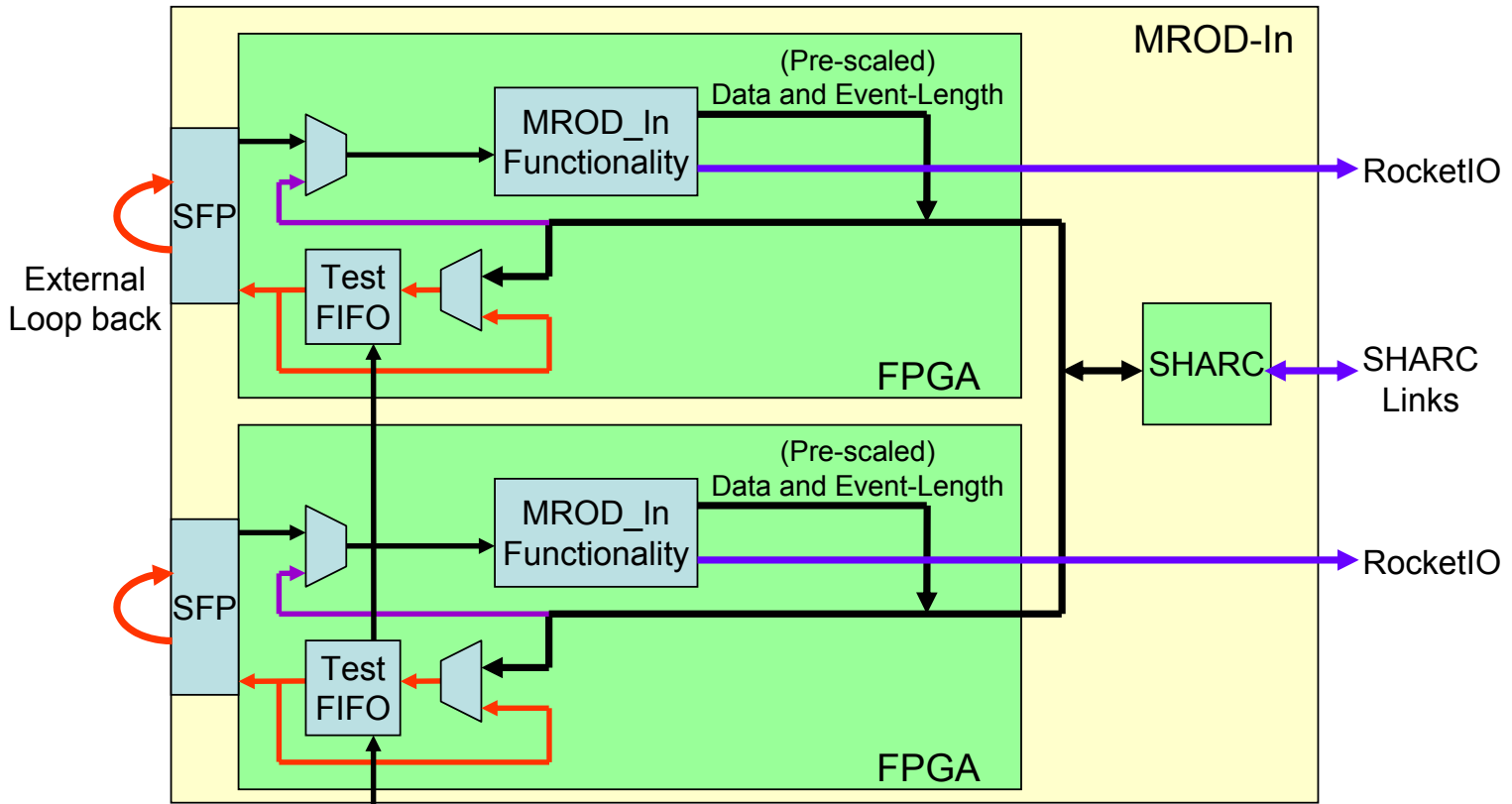
By Default: Main data stream is **not** halted by Spy Channel

Spy (MROD-Out)



By Default: Main data stream is **not** halted by Spy Channel

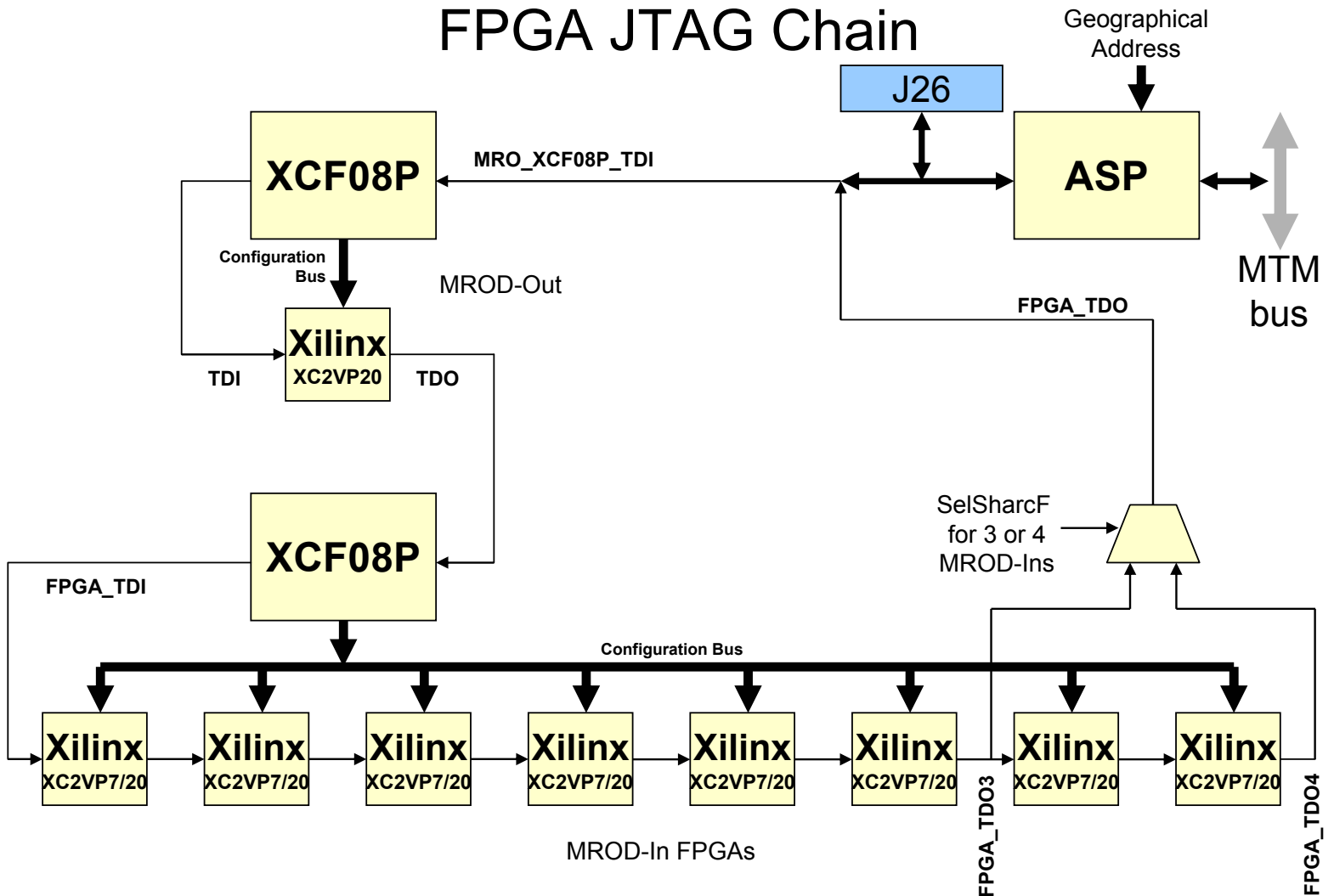
Test Generator



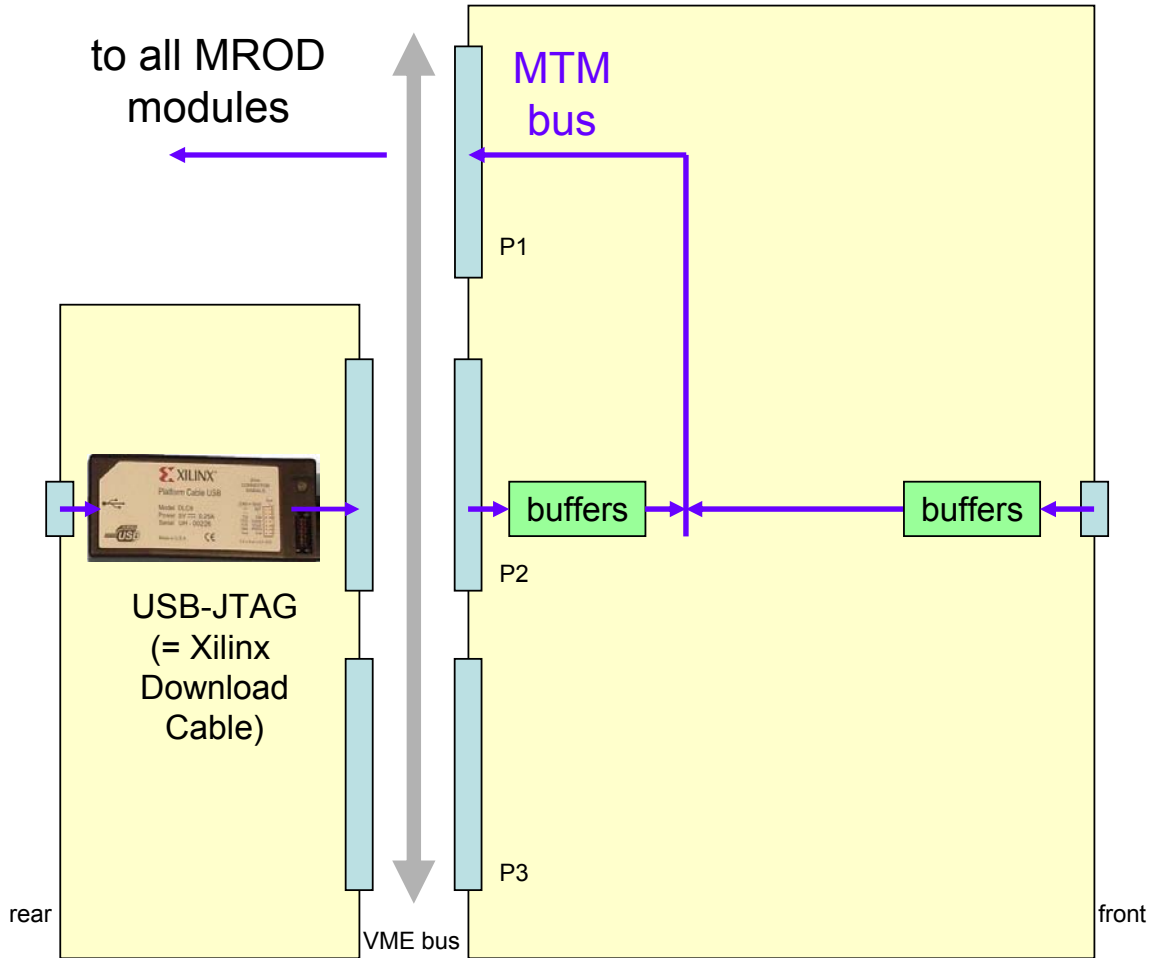
- CSM links unidirectional
- Test generator
- Transparent / Circular mode
- Free running / Triggered
- Internal test mode

Remote Configuration (1)

FPGA JTAG Chain



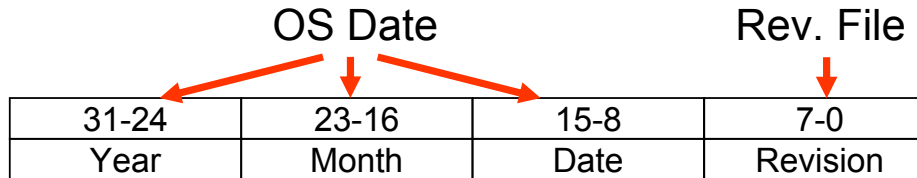
Remote Configuration (2)



Other Extras

FPGA firmware Date and Revision Register

Automatically determined during synthesis of VHDL code (TCL script)



Unique Identifier Registers (DS2401)

	31-24	23-16	15-8	7-0
ID1	ID[31-0]			
ID2	Family-ID	CRC	ID[47-32]	

Temperature Readout for each FPGA (MAX 1618)

Zero Suppress Override

choose to override zero suppression:

- Never
- Once every 'n' [1..65536] events (first event of a run always non zero suppressed)

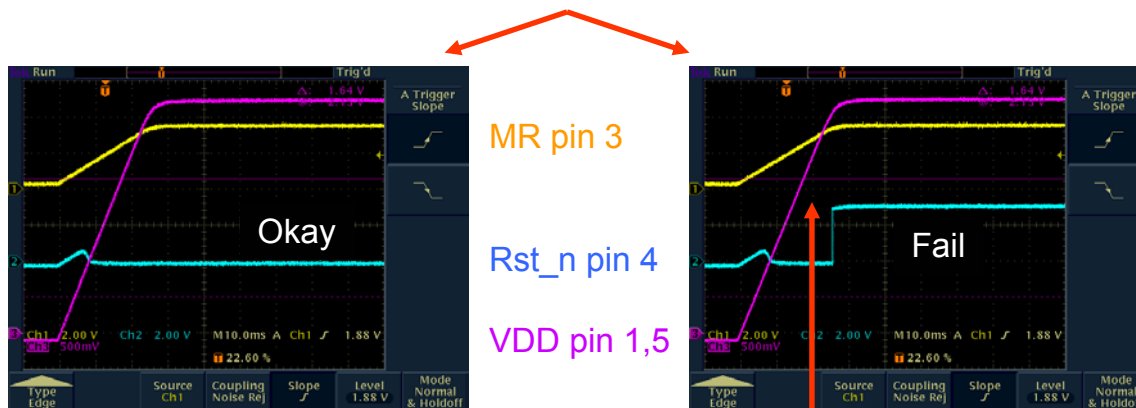
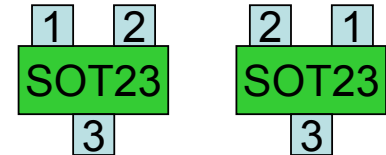
S-Link Flush Mode

Production Readiness Review of the MDT ROD

Prototype issues

Design issues found in prototypes

- Parallel termination for MROD-In FPGA configuration bus
- Pull-up resistor on FPGA TDO
- Wrong polarity for two capacitors
- Small errors in silkscreen (Dip switch SW9, Ref. IC511, Pin 1 marking)
- Footprint for inductors too small
- Short pin 1-2 for SMD LEDs (2 = Anode, 3 = Cathode) →
- Power On Reset circuit: TPS3838



Critical Ramp-Rate ~ 125 mV/ms
Happens to be exactly VME crate power supply Ramp-Rate!

Minor Assembly issues found in prototypes

Assembly house did a great job. Some issues:

- One capacitor misplaced (module 1)
 - Software Test Procedure found 2 open address pins on a Temperature Sensor (module 1)
 - One wrong component placed. IC511 = NC7SZ125 instead of NC7SZ126 (module 3)
 - One IC557 missing (NC7SZ08) (module 5)
 - One wrong component placed. IC564 = NC7SZ08 instead of NC7SZ126 (module 5)
 - Open output pin on buffer, SHARC JTAG chain (module 6)
-

Automatic Optical Inspection would track many, if not all of these failures.

Keep in mind that we asked for assembly of 6 modules (4 different production runs):
2 eight-channel, 1 eight-channel, 1 eight-channel without SHARC-B, 2 six-channel

Changes to be made in PCB

Needed:

- Parallel termination for MROD-In FPGA configuration bus (add 18 resistors)
- Add Pull-up resistor to FPGA TDO
- Change the polarity for two capacitors
- Connect pin 1 and 2 for SOT23 SMD LEDs
- Increase Footprint for inductors
- Power On Reset (still under investigation... Use MAX 6863?)

Needed for MROD-Out @ 50 MHz:

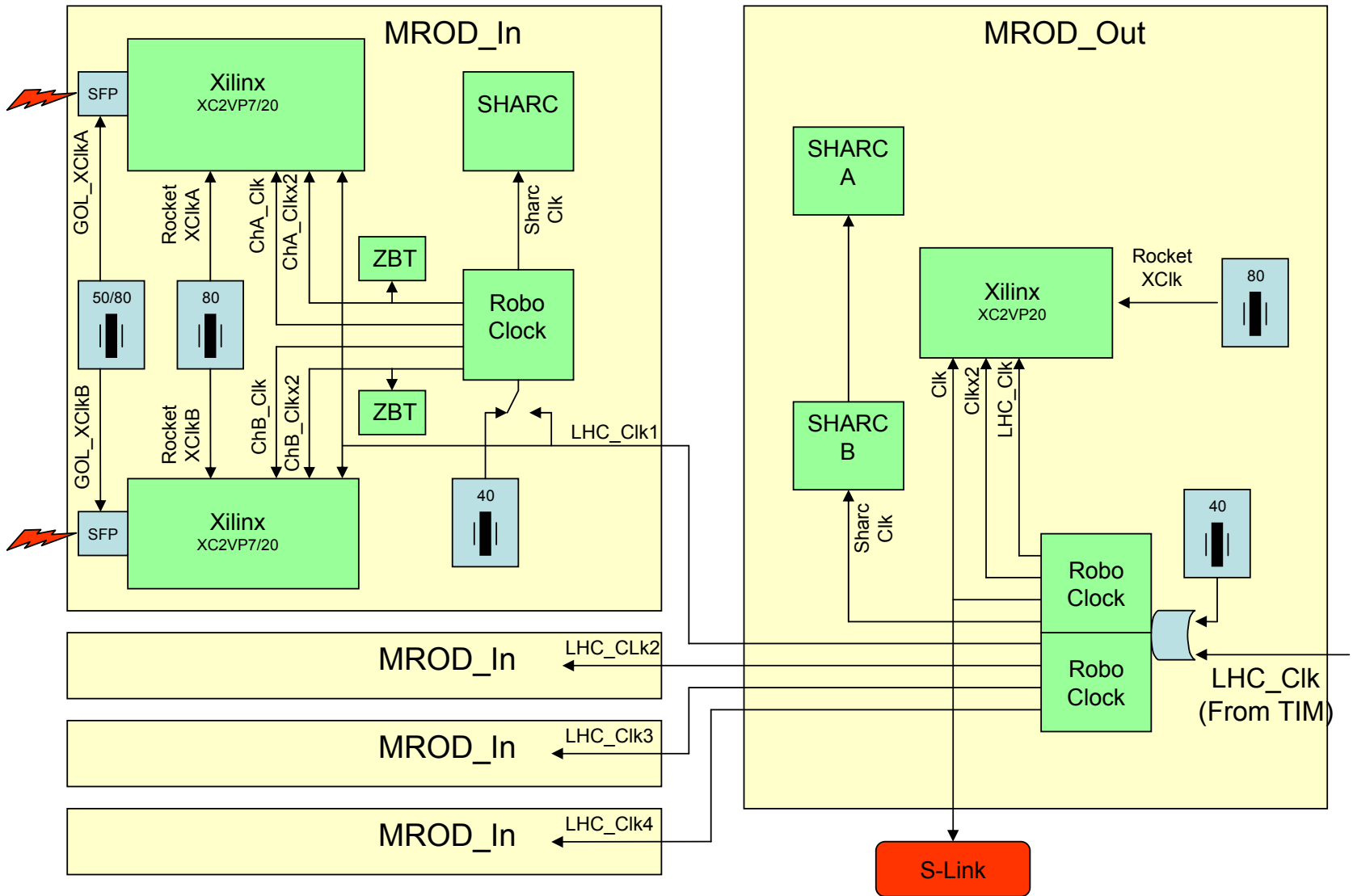
- Review Clock circuit on MROD-Out:
 - Remove automatic Clock switch for selection of LHC-Clock or crystal
 - Re-route one LHC-Clock signal
 - MROD-Out FPGA prepared, system operation still to be demonstrated

Desirable:

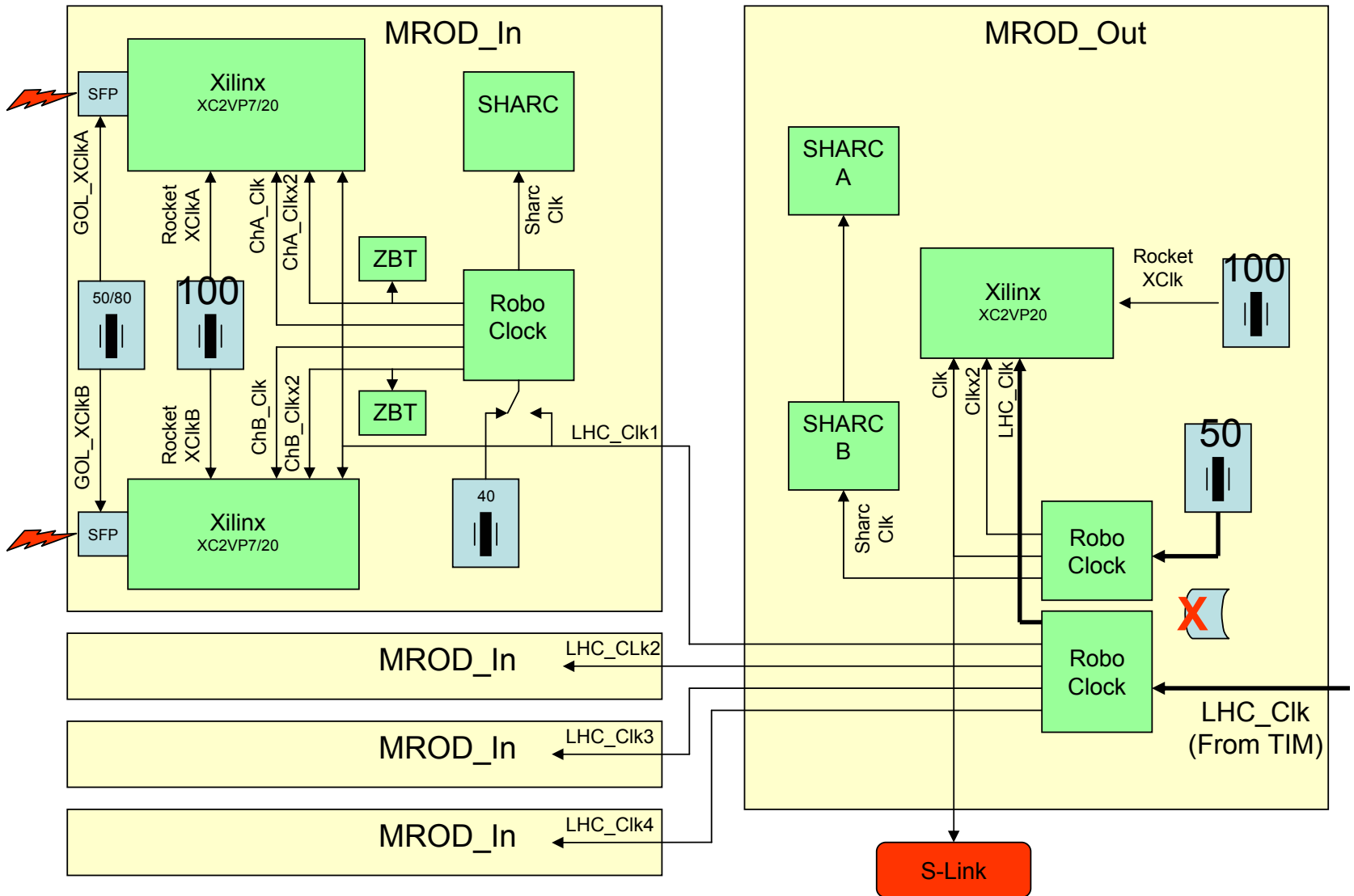
- Inverter for GA[4..0] connected to ASP
- Review silkscreen (SW9 and IC511, Pin 1 marking)

Thank you





MROD-X Clocks



MROD-X Clocks (MROD-Out @ 50 MHz)