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Specification of the LODU trigger input and output

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Abstract

This note specifies the electronics interface between the L0 Decision Unit and the L0 trigger processors (Calorimeter selection board, Muon trigger processor and Pile-up System) via optical links and the Readout Supervisor 'ODIN'.

1 Introduction

The L0DU Unit is connected to:

- the L0 trigger processors (Calorimeter selection board, Muon trigger processor and the Pile-Up System) via high speed optical links running at 1,6 Gb/s [1];
- the Readout Supervisor 'ODIN' via 16 bits LVDS link using a twisted pair ribbon cable with 17-pairs [2];
- L1 via a gigabit Ethernet connection and the TELL1 board;
- HLT via a gigabit Ethernet connection and the TELL1 board;
- ECS via an Ethernet connection and the CCPC.
- an additional control from a PC via an USB interface.

This note specifies the inputs via the High Speed optical link, the output to the Readout Supervisor and the word data format arriving in the L0DU [3].

2 Electronic and connector interface

Electronic interface

The L0 trigger processors data (CAL, MUON, PileUp) are transmitted on optical links. Two parallel optical transceivers HFBR-782BE (pluggable version) with MPO connector convert the 2×12 optical signals in 2×12 low voltage differential signals. Then, 24 deserialisers TLK2501 from Texas Instrument deserialize each optical channel to 16 bits at 80 MHz.

Connector interface

A patch panel will be used to connect the optical links coming from the L0 trigger processors and the Level-0 Decision Unit. It is composed of two modules referred in the figure 1. The front panel receives 12 single optical fibers terminated by a female **SC connector**. The Laboratory of Clermont-Ferrand is in charge of the patch panel and the physical media between the patch panel and the Level-0 Decision Unit. The L0DU plugged on a TELL1 board and the patch panel will be installed in the rack D3B07.

The rear panel is connected to a ribbon of 12 fibers via a MTP/female connector. Each single processor located at various places in the barrack send their data on single optical cable. The end of each connector has to be **SC male**. The patch panel will be connected to the L0DU through a ribbon optical fiber.



Figure 1: Pre-cabled MTP/SC or MTP/LC translators

3 High speed optical link

The emitter part of a high speed optical link is based on the following components:

- QPLL to filter the jitter of the TTC clock;
- GOL from the MIC electronic group or TLK2501 from Texas Instrument, to serialize the data;
- Single optical link transceiver like HBFR-772 from Agilent.

The receiving side is based on:

- Ribbon optical transceiver HFBR-782BE from Agilent [4], connected to a ribbon of 12 fibres, shown on figure 2;
- twelve TLK2501 from Texas Instrument [1] to deserialize the data.



Figure 2: Optical transceiver from Agilent

4 Specification of the L0 trigger processor and the L0DU interface

This part specifies the word data format between the L0DU and the L0 trigger processor.

4.1 Specification of the L0 trigger processor word format

A data word is transmitted as a 32-bit word at 40 MHz on the emitter side. It is seen as two words of 16-bit at 80 MHz on the reception side. To help detection of demultiplexing errors or synchronisation errors, a switch bit is used to identify the LSB and the MSB part of a word. The tables 1 and 2 specify the word data expected on the reception side and on the emission side, respectively.

Bit number	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0:"Switch bit"
1 st Word	LSB Information	0
	MSB Information	1
2 nd Word	LSB Information	0
	MSB Information	1
3 rd Word	LSB Information	0
	MSB Information	1
4 th Word	LSB Information	0
	MSB Information	1

Table 1: Word data format on the reception side

Bit number	Bit[31..17]	16:"Switch bit"	Bit[15..1]	0:"Switch bit"
1 st Word	MSB Information	1	LSB Information	0
2 st Word	MSB Information	1	LSB Information	0
3 st Word	MSB Information	1	LSB Information	0
4 st Word	MSB Information	1	LSB Information	0

Table 2: Word data format on the emission side

Due to the introduction of a switch bit, the effective number of data per link is 30 data bits. Furthermore each data word possibly contains a status bit to flag events containing error. Tables 3 and 4 summarize the bit assignment of the L0DU inputs for each L0 trigger processor.

Data	Muon CU	Muon SU	Cal word	<i>Total Et Cal Word</i>	<i>SPD Multiplicity Cal words</i>
BCID	2	7	7	7	7
Address	2x7	2x6	14	-	-
Computation result	2x7	2x1	8	14	14
Status bit	-	4	1	1	1
Switch Bit	2	2	2	2	2
Unused Bit	-	5	-	8	8

Table 3: L0DU input bit number according to data field assignment (CAL, MUON)

Data	Pile-up word1	Pile-up word2
BCID	7	5
More peak info	4	-
Peak position	8	8
Peak content	8	8
# Hits	-	8
Status bit	1	1
Switch Bit	2	2
Unused Bit	2	-

Table 4: L0DU input bit number according to data field assignment (Pile-up)

Due to the hardware architecture and/or the data definition, the data structure is varying between (and in some extent within) L0 processors. This prevents any fully unified definition of the data pattern to be handled by the L0DU on all links. However, as far as we can, the bit assignment of the data pattern has been tried to be unified and symmetrized between links. The following sections address the detailed bit pattern for each L0 processor.

4.2 L0 calorimeter trigger processor

The L0 calorimeter trigger [5] sends 7 words to the L0DU via the selection board. Five of them bring the information from electron, photon, hadron, local and global π^0 's candidates, respectively, in an identical way. Two specific words contains the HCAL Total Et and the SPD Multiplicity information.

The tables 5 and 6 specify the L0DU input data format for the five common words corresponding to electron, photon, local π^0 , global π^0 and hadron trigger candidates.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
E_T (7 downto 0)	$D(8$ downto 1)	RXD(8 downto 1)
BCID (6 downto 0)	$D(15$ downto 9)	RXD(15 downto 9)

Table 5: LSB CAL word bits assignment

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
Address (13 downto 0)	$D(14$ downto 1)	RXD(14 downto 1)
Status bit	$D(15)$	RXD(15)

Table 6: MSB CAL word bits assignment

The tables 7 and 8 display the specific LSB and MSB data assignment for the "HCAL *Total Et*" word, respectively. A similar data mapping can be drawn for the "SPD Multiplicity" word, as shown on the tables 9 and 10.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
"00000000" (unused bits)	$D(8$ downto 1)	RXD(8 downto 1)
BCID (6 downto 0)	$D(15$ downto 9)	RXD(15 downto 9)

Table 7: $Total E_T$ LSB word bits assignment

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
Total E_T (13 downto 0)	$D(14$ downto 1)	RXD(14 downto 1)
Status bit	$D(15)$	RXD(15)

Table 8: Total E_T MSB CAL word bits assignment

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
"00000000" (unused bits)	$D(8 \text{ downto } 1)$	RXD(8 downto 1)
BCID (6 downto 0)	$D(15 \text{ downto } 9)$	RXD(15 downto 9)

Table 9: SPD Multiplicity LSB word bits assignment

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
SPD Multiplicity (13 downto 0)	$D(14 \text{ downto } 1)$	RXD(14 downto 1)
Status bit	$D(15)$	RXD(15)

Table 10: SPD Multiplicity MSB CAL word bits assignment

4.3 L0 Muon trigger processor

The L0 MUON trigger processor [6] sends 4 pairs of words to the L0DU (2 words per quarter). Each pair of word contains the information corresponding to 2 muon candidates (denoted C1 and C2 hereafter). The two words of each pair come from two separated units (the Control Unit (CU) and the Slave Unit (SU) respectively). The full address of a muon candidate is defined with 13 bits, separated in three fields : 7 bits are defining the "M3 address", 2 bits are defining the Processing Unit (PU) relative to a quarter and 4 bits are defining the Processing Board (PB) relative to a PU. The 2x7 bits defining the "M3 addresses" for C1 and C2 candidates are coming from the Control Units while the 2x6 bits defining the PU and PB are originating from the Slave Units. The tables 11 and 12 specify the LSB and MSB data assignment for the words coming from CU's, respectively.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
P_T C2 (6 downto 0)	$D(7 \text{ downto } 1)$	RXD(7 downto 1)
M3 Address C2 (6 downto 0)	$D(14 \text{ downto } 8)$	RXD(14 downto 8)
BCID (0)	$D(15)$	RXD(15)

Table 11: LSB bits assignment for the Muon word coming from the Control Units

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
P_T C1 (6 downto 0)	$D(7$ downto 1)	RXD(7 downto 1)
M3 Address C1 (6 downto 0)	$D(14$ downto 8)	RXD(14 downto 8)
BCID (1)	$D(15)$	RXD(15)

Table 12: MSB bits assignment for the Muon word coming from the Control Units

The tables 13 and 14 specify the data assignment for the words coming from SU's. This data pattern is similarly for the 4 quarters.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
PU C2 (1 downto 0)	$D(2$ downto 1)	RXD(2 downto 1)
PB C2 (3 downto 0)	$D(6$ downto 3)	RXD(6 downto 3)
muon sign C2 (0)	$D(7)$	RXD(7)
"0" (unused bit)	$D(8)$	RXD(8)
BCID (6 downto 0)	$D(15$ downto 9)	RXD(15 downto 9)

Table 13: LSB bits assignment for the Muon word coming from the Slave Units

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
PU C1 (1 downto 0)	$D(2$ downto 1)	RXD(2 downto 1)
PB C1 (3 downto 0)	$D(6$ downto 3)	RXD(6 downto 3)
muon sign C1 (0)	$D(7)$	RXD(7)
"0000" (unused bits)	$D(11$ downto 8)	RXD(11 downto 8)
Status (3 downto 0)	$D(15$ downto 12)	RXD(15 downto 12)

Table 14: MSB bits assignment for the Muon word coming from the Slave Units

4.4 Pile-up system

The L0 Pile-up system sends information for VETO computation. We propose that L0 Pile-up trigger sends 2 words of 32 bits to the L0DU. The word corresponding to peak1 and peak2 will be sent on two dedicated links. The tables 15 and 16 specify the word data assignment for the Pile-up System peak1 word.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
Peak1 content (7 downto 0)	$D(8 \text{ downto } 1)$	RXD(8 downto 1)
BCID (6 downto 0)	$D(15 \text{ downto } 9)$	RXD(15 downto 9)

Table 15: LSB bits assignment for Pile-up system peak1 word

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
Peak1 position (7 downto 0)	$D(8 \text{ downto } 1)$	RXD(8 downto 1)
More peak info (3 downto 0)	$D(12 \text{ downto } 9)$	RXD(12 downto 9)
"00" (unused bits)	$D(14 \text{ downto } 13)$	RXD(14 downto 13)
Status bit	$D(15)$	RXD(15)

Table 16: MSB bits assignment for Pile-up system peak1 word

The tables 17 and 18 specify the word data assignment for the Pileup System peak2 word.

Field	Bit assignment	TLK output pin
Switch bit = "0" (LSB)	$D(0)$	RXD(0)
Peak2 content (7 downto 0)	$D(8 \text{ downto } 1)$	RXD(8 downto 1)
# hits (1 downto 0)	$D(10 \text{ downto } 9)$	RXD(10 downto 9)
BCID (4 downto 0)	$D(15 \text{ downto } 11)$	RXD(15 downto 11)

Table 17: LSB bits assignment for Pile-up system peak2 word

Field	Bit assignment	TLK output pin
Switch bit = "1" (MSB)	$D(0)$	RXD(0)
Peak2 position (7 downto 0)	$D(8 \text{ downto } 1)$	RXD(8 downto 1)
# hits (7 downto 2)	$D(14 \text{ downto } 9)$	RXD(14 downto 9)
Status bit	$D(15)$	RXD(15)

Table 18: MSB bits assignment for Pile-up system peak2 word

4.5 Status bit

The status bit should be set to '1' when the data is containing an error. Two cases must be differentiated:

- the incoming data could be used in the computation of the decision;
- the incoming data could not be used in the computation of the decision. In order to identify this case, all other bits (LSB + MSB) have to be asserted low.

In case of error, the decision is computed but a flag in the decision word will indicate that the decision could be erroneous.

4.6 Summary of the data pattern

The data pattern for each L0 processor is summarized on the tables 19, 20, 21, 22, 23 and 24 .

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[6-0]							E_t [7-0]							'0'	
MSB Field	Status	Address[13-0]													'1'	

Table 19: Bit pattern of the L0Calo words for the five optical links connected to the electron, photon, hadron, local and global π^0 s candidates, respectively

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[6-0]						'00000000'						'0'			
MSB Field	Status	Total E_T/SPD multiplicity [13-0]										'1'				

Table 20: Bit pattern of the L0Calo words for the two optical links connected to the Total E_t and SPD multiplicity, respectively

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[0]	M3 Address [6-0] C2						P_t[6-0] C2						'0'		
MSB Field	BCID[1]	M3 Address [6-0] C1						P_t[6-0] C1						'1'		

Table 21: Bit pattern of the L0Muon words for the four optical links connected to CU. C1 and C2 refer to the first and the second muon candidate within the considered quarter.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[6-0]						'0'	\pm C2	PB C2			PU C2			'0'	
MSB Field	Status			'0000'			\pm C1	PB C1			PU C1			'1'		

Table 22: Bit pattern of the L0Muon words for the four optical links connected to SU. C1 and C2 refer to the first and the second muon candidate within the considered quarter.

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[6-0]							1st peak content [7-0]							'0'	
MSB Field	Status	'00'	More peak info				1st peak position					'1'				

Table 23: Bit pattern of the first L0Pile-Up words

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB Field	BCID[4-0]					# hits [1-0]		2nd peak content [7-0]							'0'	
MSB Field	Status	# hits [7-2]					2nd peak position					'1'				

Table 24: Bit pattern of the second L0Pile-Up words

5 Specification of the L0DU-ODIN link

The L0 trigger link between the L0 Decision Unit and the Readout Supervisor 'ODIN' transmits the L0 trigger decision at a rate of 40 MHz. Each decision consists of a 16-bit data word [2]:

- Bunch crossing number L0-BCID (12 bits);
- L0 Trigger decision L0-Decision (1 bit);
- L0 force bit L0-force (1 bit);
- timing trigger bit L0-TIM-TRG (1 bit);
- Status (1 bit).

We introduce a status that indicates that the L0DU decision is erroneous or not. This status bit will be asserted high when the hardware detects an error. The table 25 specifies the bit assignment for the output to the Readout Supervisor.

The trigger word is transmitted over a point-to-point parallel 16-bit LVDS link using a 3M pack connector (34-pins) and a twisted pair ribbon cable with 17 pairs. The position of ODIN connector on the L0DU is on the front side of the L0DU and on the front side of the L0DU rack. The figure 3 specifies the connection for the Readout Supervisor output.

Field	Bit assignment
L0-BCID (11 downto 0)	$D(11 \text{ downto } 0)$
L0-Decision	$D(12)$
L0-force	$D(13)$
L0-TIM-TRG	$D(14)$
Status	$D(15)$

Table 25: L0 trigger output to the Readout Supervisor

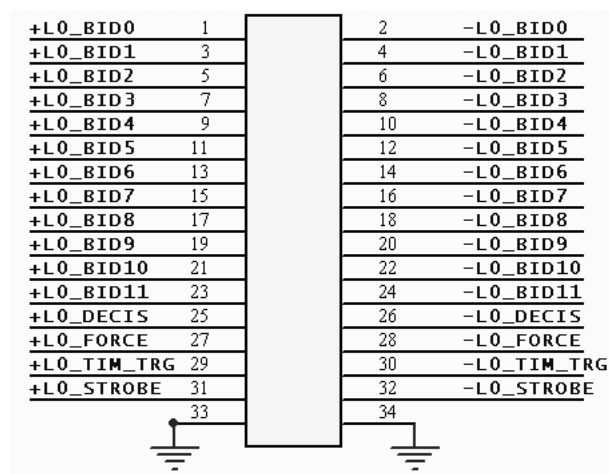


Figure 3: L0DU output to the Readout Supervisor. The pair called L0-Strobe is used for the status information.

6 Conclusion

In this note, we specify the electronics interface and the word bits assignment between the L0 Decision Unit and L0 triggers processors via optical links and the Readout Supervisor. The details concerning the communication protocol will be specified in a specific EDMS.

References

- [1] Texas Instrument “TLK2501 1.5 to 2.5 GBPS transceiver datasheet”.
- [2] R. Jacobsson *et al.* “Specifications of the L0DU-ODIN link” LHCb note,EDMS 478756, 2004.
- [3] R. Cornat “Level-0 Decision Unit for LHCb” LHCb note LHCb 2003-065, TRIG, (2003).
- [4] Agilent Technologies “Agilent HFBR-772B / BE and HFBR-782B / BE plug-gable Parallel Fiber Optic Modules, Transmitter and Receiver” Datasheet.
- [5] M. Bargiotti *et al.* “The selection crate for the Calorimeter Trigger” LHCb note LHCb 2003-095.
- [6] E. Aslanides *et al.* “Specification of the Muon Processing board” LHCb note LHCb 2002-003, TRIG.