SHASLINK tests and test software

v1.4 (30 Nov 1999), Henk Boterenbrood

- **sndr_sl + (PCISHARC) recv_ps** and
  recv_sl + (PCISHARC) sndr_ps
  - to test one link at a time sending data from SHASLINK to PCISHARC, or from PCISHARC to SHASLINK; includes check of every word transferred.
  - **sndr_sl/recv_sl** should be run on a SHASLINK module, **recv_ps/sndr_ps** should be run on a PCISHARC module (**sndr_sl** and **recv_sl** will also run on a CRUSH module).
  - 20 Mbyte (DMA size <20 words) or 40 Mbyte (DMA size >= 20 words) of data is transferred when data check is enabled
  - 100 Mbyte (DMA size <20 words) or 200 Mbyte (DMA size >= 20 words) of data is transferred when data check is disabled
  - data check disable is optional (see options below): either a nibble-pattern (0x0f781e69 and 0x2d5a3c4b) or random data (with known seed) is sent (this is a compile option).
  - link 4 and 5 can not be tested like this as long as there is no NT driver for SHASLINK (because link 4 is needed for booting, and link 4 and 5 form a cable pair).

  Options:

-l<*link*>	use Link Port <*link*> (default: 0)
-s<*size*>	use <*size*> number of words for each DMA (default: 256)
-c<*speed*>	set link speed:<*speed*> =1: 20 MB/s, <*speed*> =2: 40 MB/s (default: 40 MB/s)
-n	disable data check (link transfer rate should now approach 20 or 40 MB/s)
-d	(only if checking enabled) report each individual error in the data, otherwise print a table of errors after completion of the test.

- **ppshsl**
  - 'peek' and 'poke' in SHARC memory map
  - (single) blockmoves from/to PCI: either by SHARC core or SHARC DMA or PCI9054 DMA.
  - SHARC Flag read/write:
    Flag 0, 1, 3: can be tested; use SLIDAD
    Flag 2: PLX fifo 'almost full' status, tested by **shslreg**.
  - some SHARC addresses (word addresses):

0x00000000-0x000000FF	SHARC IOP registers (see SHARC documentation)
0x00020000- 0x0003FFFF	SHARC internal memory (normal word addressing)
0x00400000-0x005FFFFF	PLX Direct Master area (2 MWord, usable range depends on buffersize setting in PLX driver)
0x00600000-…	PLX registers (see PLX PCI9054 documentation)
0x00800000	SHASLINK Control and Status Reg
0x00800001	Burst Counter
0x00A00000	S-LINK data word (write only)
0x00A00001	S-LINK control word (write only)

- **shslreg**
  - (write/)read test of selected registers
  - all values in registers with < 21 bits, about 1 million random values for other registers.
  - tested read: **PCI9054 PCI and Local Configuration Registers** (compare with PLX documentation)
  - test of SHARC **FLAG2**: initiates a Direct-Master to PCI DMA (by SHARC DMA) and polls FLAG2 while this takes place: FLAG2 should change from 0 to 1 and back to 0.
  - tested write/read:
    - **SHASLINK Control+Stat Reg**
      (1 bit: bit 5; other bits to be tested in combination with IRQ0 and IRQ2)
    - **Burst Counter** (16 bits)

- **shslout + (CRUSH) crin** and
  shslout + (CRUSH) crinchck or **shslout + SLIDAD**
  - test of S-LINK connection between SHASLINK (S-LINK output) and CRUSH (S-LINK input) using 'event' data blocks delimited by BOB and EOB S-LINK control words (optionally: SLIDAD mounted on SHASLINK can serve as data drain);
    to be used in combination with the following programs running on a CRUSH:
  - **crin**: receives 64000 events of equal size, checks for error interrupts, prints timing parameters at end of test (MB/s, s/evt, etc…).
  - **crinchck**: receives any number of (consecutive) events, checks for error interrupts, checks FIFO data, checks some of the event data words.

shslout *Options:*

-s<*size*>	use <*size*> number of words for each event including BOB/EOB (2<=*size*<=2048; default: 1000).
-e<*events*>	generate <*events*> events (default: 64000)
-d	use DMA to transfer events to S-LINK (default: word-by-word by SHARC core)

- **shslintr**
  - test of the SHASLINK SHARC interrupt sources:
    1. IRQ0: S-LINK LRL Change (use SLIDAD to test this one!)
    2. IRQ1: Interrupted Burst Transfer
       (sets burst counter to higher value, does a few MS0 accesses and then an MS3 (S-LINK interface) access).
    3. IRQ2: S-LINK LDOWN (use SLIDAD to test this one!)
    4. IRQ2: PCI9054 LSERR
       (makes use of parity error detection through LSERR; PCI9054 parity signals are not implemented so when parity error detection is enabled every Direct Master area access generates an error and LSERR)
    5. IRQ2: PCI9054 LINT
       (uses the BIST interrupt)

Options:

-s	stop after every subtest, show intermediate result
-r<*rep*>	repeat every interrupt test <*rep*> times (default 1x); display summary per interrupt source