

Status report of the L0 Pile Up Veto System

L. W. Wiggers for the LHCb NIKHEF Pile-Up Veto Group
NIKHEF
P.O. Box 41882, NL-1009 DB Amsterdam
Version 1.21

July 17, 2002

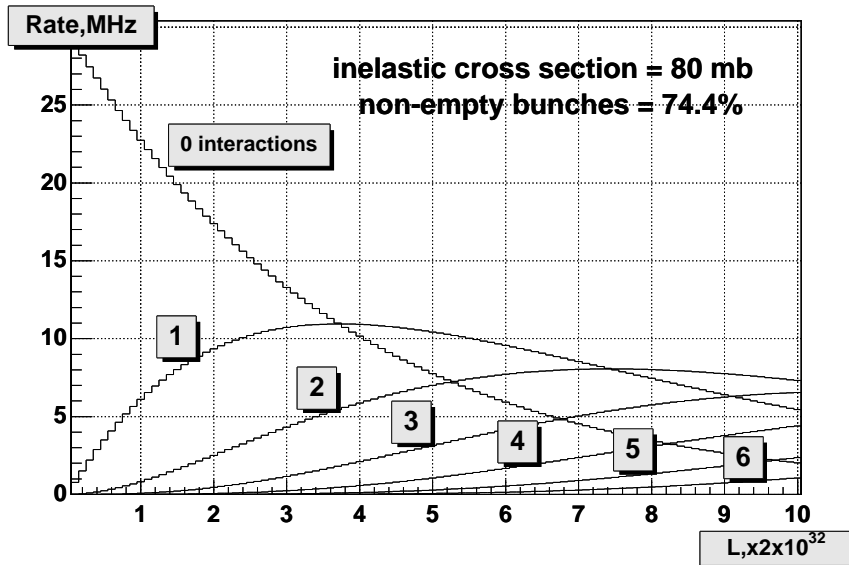


Figure 1: Production rate of events with 0,1,2 etc. interactions as a function of luminosity.

1 Overview

1.1 Introduction

In this report an overview is given of how multiple vertices are found in the L0 Pile-Up VETO system, of the system architecture and of the status of implementation of the system. Since many aspects are similar to that of the VELO system, often the VELO-TDR [1] is referenced. The results of the analysis presented here are mainly based on a study [2] for the TP, the system has been described earlier in [3], [4] and [5]. Moreover, the use of the system for luminosity monitoring has been described separately in [6], [7] and [8].

1.2 Luminosity and pile-up

For most LHCb subdetectors the maximum luminosity considered is $5 \cdot 10^{32} \text{cm}^{-2} \text{s}^{-1}$. Above that, the occupancies are too high and the lifetime of the detectors becomes too short. For the VELO detectors it is concluded [9] for different irradiation models that at the nominal luminosity of $2 \cdot 10^{32} \text{cm}^{-2} \text{s}^{-1}$ they can operate at a depletion voltage of less than 400 V for over 2 years of running. By reducing the number of double events or more specifically events that are difficult to reconstruct, the optimal value for the luminosity can be chosen. The default luminosity in the TP was set to be: $2 \cdot 10^{32} \text{cm}^{-2} \text{s}^{-1}$.

In Figure 1 and 2 results from the analysis of N. Zaitsev [2] are shown. At a nominal L0 trigger rate of 1 MHz the relative contribution of events with multiple interactions increases with luminosity. This conclusion is supported by later results, see fig. 3 [10]. Clearly, the chance of a crossing being accepted by the L0-trigger becomes higher as the number of interactions per crossing increases. The events with multiple interactions are more complicated to analyse offline and are candidates to be eliminated from the data sample at the trigger level.

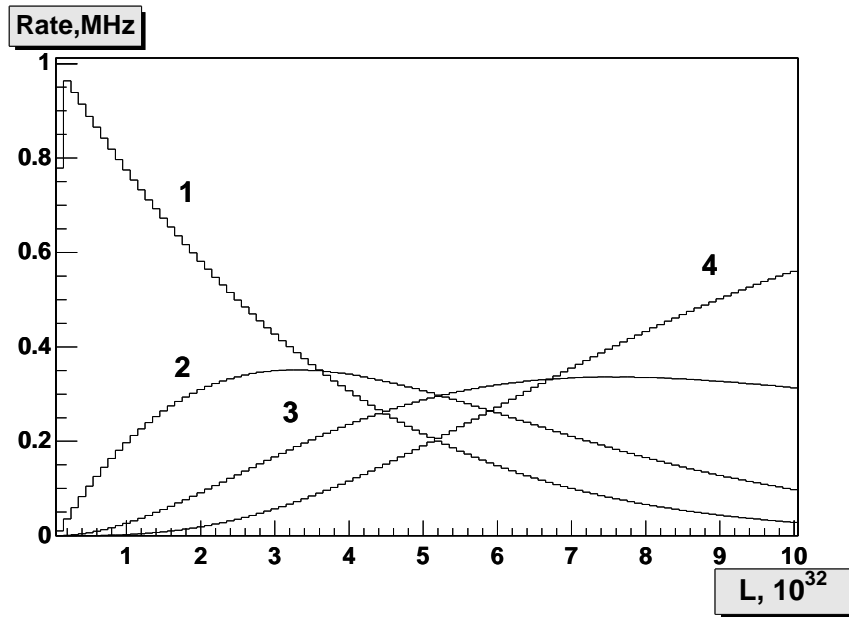


Figure 2: Rate of inelastic events ($x=0.3$) accepted by L0 high- p_t trigger. Events with multiple interactions contribute significantly to the available bandwidth.

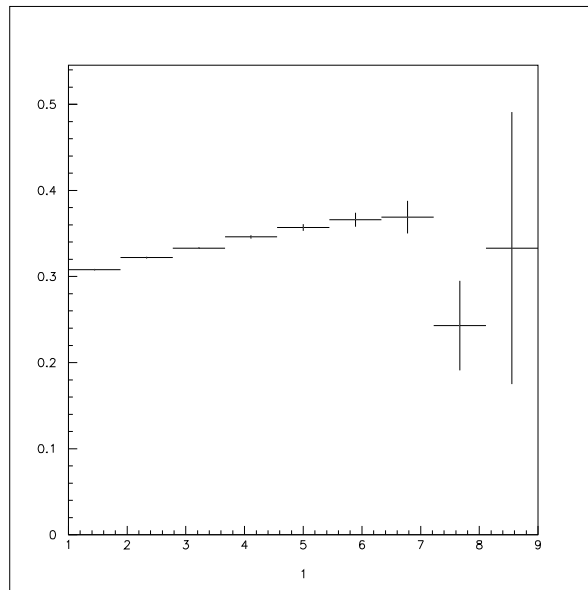


Figure 3: Fraction of interactions per crossing accepted by L0 versus the number of events per crossing at $5 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$.

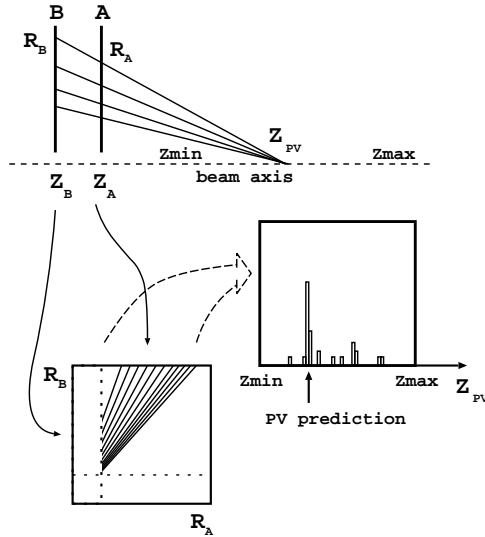


Figure 4: Basic principle of detecting the primary vertex PV . The readout hits of plane A and B are combined in a coincidence matrix. The resulting combinations are projected onto a z -histogram. The largest peak corresponds to the primary vertex (PV).

1.3 Pile-up veto concept

The pile-up detector consists of two planes (A and B) parallel to each other (fig.4). Every plane is a wheel with 2 Silicon strip counters [1]. In both planes the radii of track hits, R_A and R_B , are recorded. The hits belonging to one track have the following simple relation:

$$\frac{R_B}{R_A} = \frac{Z_B - Z_{PV}}{Z_A - Z_{PV}} = k, \quad (1)$$

where Z_B , Z_A are the detector positions and Z_{PV} is the position of the (unknown) track origin on the beam axis (i.e. the primary vertex). The ratio of the two measurements, k , uniquely relates to a certain z -position along the beam axis. The equation is exact if $x = y = 0$. The resolution of Z_{PV} is limited by multiple scattering and the strip width of the detectors. The latter effect dominates.

1.3.1 Coincidence matrix

The coincidence matrix method makes use of relation (1) in a correlation plot of R_A versus R_B . Vertex information can be extracted by summing the entries in a wedge between lines of constant k -ratio. The corresponding z -position is obtained by applying formula (1).

An example of a typical double event is shown in fig.5. A single point in plot 5a corresponds to one track. Tracks from the same origin on the beam axis produce a set of points on a straight line. The lines match with the two vertices in the event. One needs, however, to consider all possible combinations and not just the true combinations, see fig.5b. The lines are now more difficult to detect. In fig.5c the distribution of the z -predictions is histogrammed. The two shaded peaks correspond to the two vertices. The contents of the other histogram bins are of combinatorial origin.

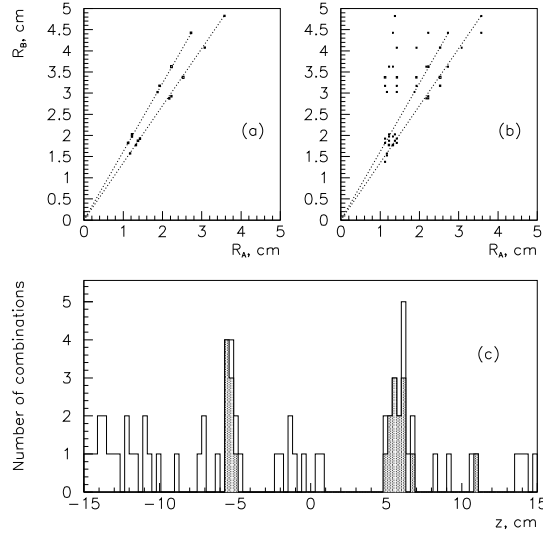


Figure 5: Correlation of the measurements in the two planes. A typical event with two vertices is displayed. True combinations (a), i.e. both hits from the same track, and all combinations (b) are shown separately. The slope of a dotted line corresponds to a z -position of a vertex. The number of entries between lines of constant ratio R_B/R_A is shown in histogram (c) as a function of z (bin size is 5 mm). The true combinations contribute to the shaded peaks.

1.3.2 Masking of hits

The efficiency to find the vertex with the highest track multiplicity (i.e. with the highest correspondent peak) is close to 100%. However, there is a possibility that two interactions produce a very different number of tracks. As a consequence, the height of the two peaks in the histogram can differ considerably and the smallest one can be lower than the overall level of combinatorics.

A few additional steps are introduced to cope with this situation. First, after the largest peak is found the combinations which contributed to this peak are searched for. Then, those hits in both stations are masked. Finally, the hits are correlated in the coincidence matrix again. Some hits from tracks having the second vertex as an origin will also be removed by masking. However, the height of the correspondent vertex peak is well above the combinatorics level that is reduced as well. See fig.6 for a typical example of the above category.

The two peaks are considered as candidates for primary vertices. Their positions are determined by:

$$Z_{PV} = \frac{\sum_{i=-1}^1 Z_{PV}^i \cdot h_i}{\sum_{i=-1}^1 h_i}, \quad (2)$$

where Z_{PV}^i are the coordinates of the histogram bins around the maximal one ($i = 0$), h_i is a count of the number of combinations in these bins.

An extension of the method to recognise more vertices is under study. A gliding bin size over the z -scale of -15 cm to +15 cm and the combination of the histograms of top and bottom detectors is simulated.

In fig.7 the positions of the VETO Si-detectors are shown. Compared to the TP design the

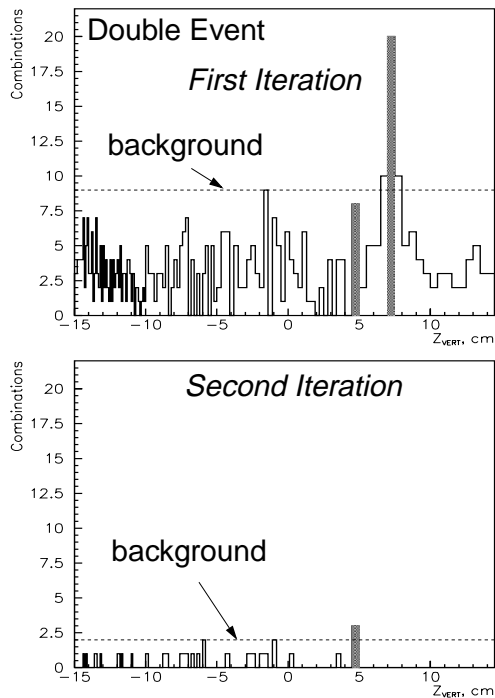


Figure 6: Z-vertex histogram in double event, before (top) and after (bottom) hit masking. The shaded bins represent the two interaction vertices.

detectors are smaller, they are closer to the beam and the left and right detectors are displaced over a larger distance with respect to each other.

1.4 Other methods

The total energy seen in calorimetry is another parameter for rejecting pile-up events. Earlier this method was found [6] to be less effective for rejection of double events due to the large overlap in E_{tot} distributions for single and double events.

1.5 Requirements

The L0 and L1 parameters, as defined in [12] for FE-electronics, are summarised in Table 1. The principle of readout is illustrated in fig. 8. For the output stage of the Pile-Up VETO system these parameters have to be taken into consideration. In addition, the latency of the L0 VETO subsystem should be shorter than the longest latency in the L0-system ($latency < 2175 ns$).

2 Simulation

2.1 Introduction

Instrumental effects that have been taken into consideration in simulations [2] are: noise, shaping, overspill, cross talk, strip mask, detector alignment, beam position stability, radiation effects and track multiplicity. The conclusions were:

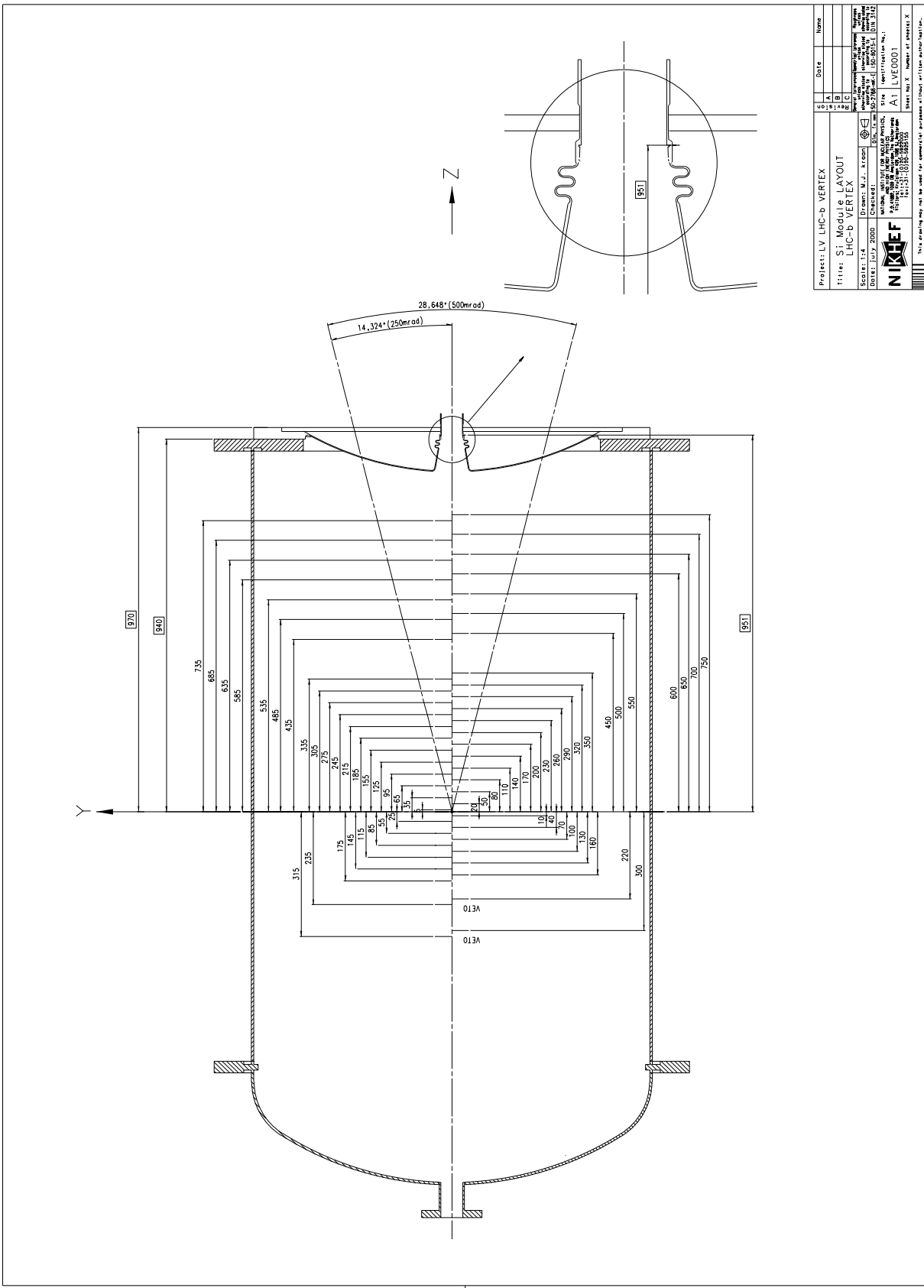


Figure 7: Layout of the Vertex tank with indicated the 2 sets of VETO counters.

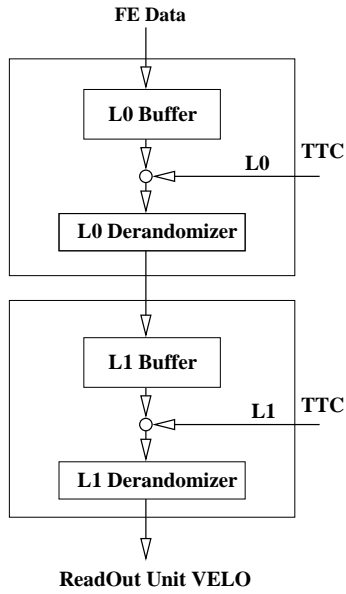


Figure 8: Generic view of FE DAQ.

L0 Rate	1.1 MHz
L0 Readout latency	4.0 μ s
L0 Consecutive triggers	Max. 16
L0 Derandomiser depth	16 events
L0 Derandomiser readout time	900 ns
L1 Rate	40-100 kHz
L1 buffer depth	1927
L1 Derandomiser depth	15 events

Table 1: L0 and L1 parameters for LHCb FE electronics.

Analysis	MC generator
[2]	Pythia 5.7 (default and IM=3) Pythia 6.134 default
[10]	Pythia 6.134 default

Table 2: MC physics generators

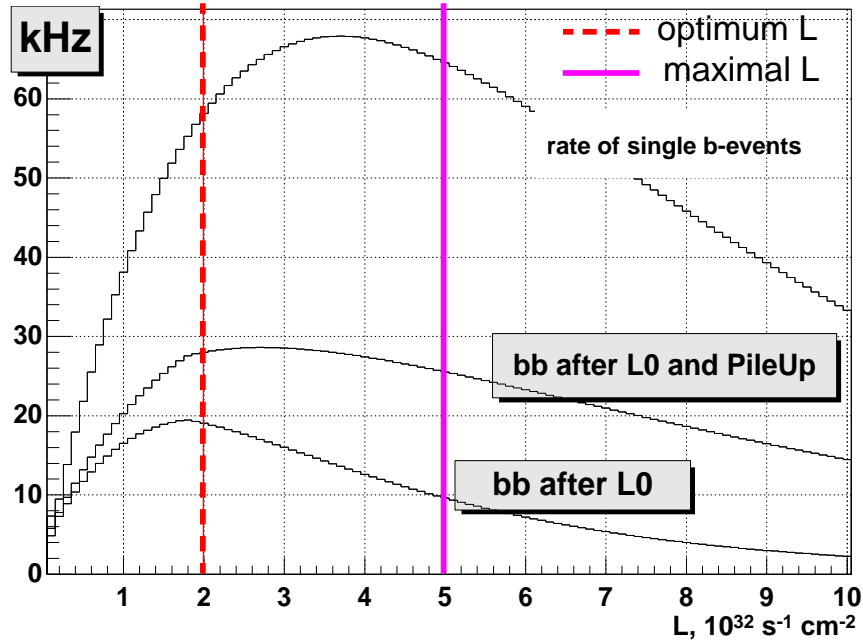


Figure 9: Rate of single b-events as function of luminosity. The upper curve is the rate of single b-events at LHC, the lowest curve is the rate of b-events after applying the L0 p_t cuts, the middle curve show the increase in rate of b-events after applying the pile-up cuts while relaxing the L0 cuts.

- The intrinsic resolution caused by fluctuations in the ionisation has no effect on the trigger performance
- The algorithm can tolerate high noise levels before having effect. For a $300 \mu\text{m}$ thick detector: $S/N > 5-6$
- Beetle and SCTA shaping is satisfactory, overspill should be less than 25%
- Cross talk (strip to strip coupling) can be tolerated at a high level, it should be less than 30%
- The detector alignment is not critical: $< 100 \mu\text{m}$
- Twice the expected level of radiation can be tolerated without effect on performance
- A track multiplicity change of $\sim 5\%$ has just a marginal effect.

2.2 Results

In fig. 9 the gain in the number of b-events is shown as function of luminosity, as found in the study of N. Zaitsev [2]. Under the assumption that when a crossing contains multiple events it will be disregarded, a gain of 30% was found .

Since this study the situation has somewhat changed:

- in the L1 system also double events events can be handled
- the bunch crossing time is prolonged to 75 ns for the LHC starting period

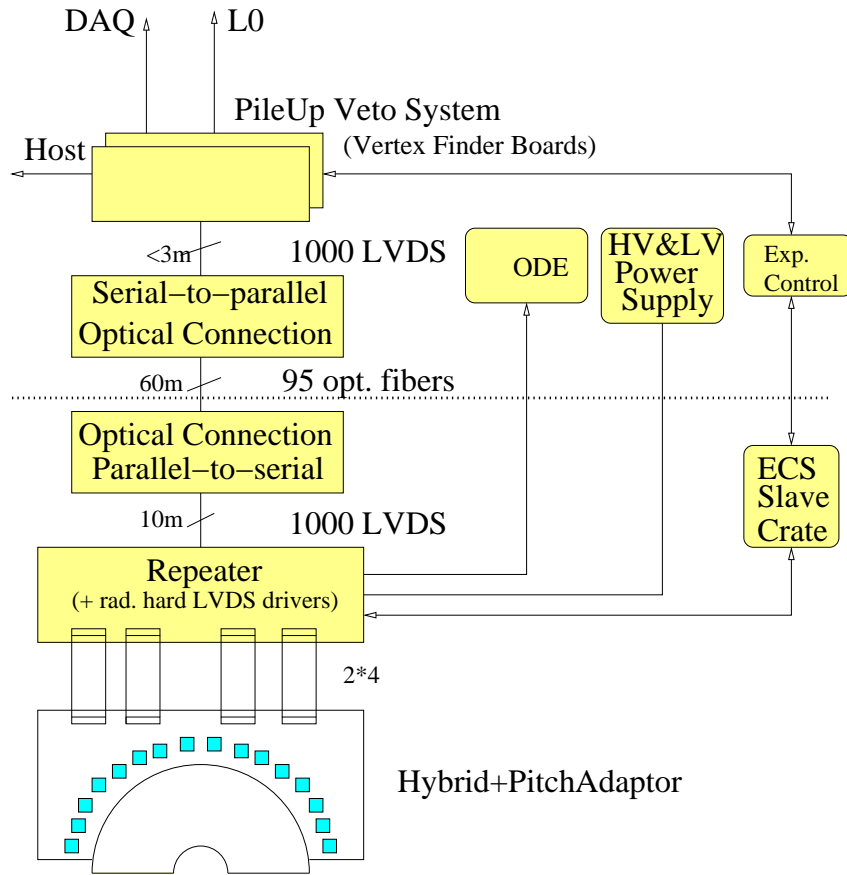


Figure 10: Overview of the Pile-Up VETO system.

Hybrid	Repeater Station	10 m off tank
200 kRad/y	20 kRad/y	<100 Rad/y

Table 3: Radiation levels at several locations of the Pile-Up VETO System electronics.

This leads to the requirement to recognise multiple events in a different luminosity regime. The algorithm will be changed accordingly and simulations will be redone.

3 Technical Design

In fig. 10 an overview is given of the system. The digital signals from the comparators of the 16 Beetle chips on the hybrid are buffered in the Repeater Station on the vertex tank (if necessary) and led to a LVDS to Optical Transmitter Station. Behind the shielding wall the receiver ends of the optical links are located. There the serialised data will be fanned out in parallel again. A single crate will house the Pile-Up Veto System: LVDS input boards, 5 Vertex Finder Boards and an Output Board. The other output paths of the Beetle and ECS connections are as described in the VELO-TDR [1]. The decision to locate the processor part behind the shielding wall was taken to avoid radiation induced effects (dose effects, SEU's and SEL's) that could occur when the system would be located near the vertex tank (see Table 3 based on [1] [9]).

3.1 Si-detectors

The detectors used are identical to the ones to be installed for the VELO system. Only R-detectors and no Phi-detectors will be installed.

As specified in the VELO-TDR the R-detectors will have a $40\mu\text{m}$ pitch below a radius of 18.5 mm. At larger radii the pitch gradually increases to a maximum of $92\mu\text{m}$ at a radius of 42 mm. At radii of < 24.1 mm the strip lengths are halved, giving an angular coverage of 45 degrees. In the input boards of the Pile-Up VETO processing these strips could be combined. An alternative is to use dedicated masks for the R-detector for the pile-up veto system where this division is not made. The number of channels can then be much lower ($1024 \rightarrow 640$). Although the decrease only partly helps in reducing the complexity of the hybrid, this is the preferred solution for this type of detector.

Another VELO option is to use detectors with 45 degree sectors with increasing strip distances as function of R. If the strips of these sectors can be combined on the detector into 90 degree sectors, this will result in a total number of output channels that decreases by a factor 2 from 1024 to 512. The number of readout chips on the hybrid decreases accordingly from 16 to 8. This solution is even more preferable.

In the Beetle 4 detector input channels are combined at the comparator stage. This implies a vertex accuracy in the order of 3-4 mm from geometrical considerations alone. The sets of detectors of both halves are displaced by 1.5 cm with respect to each other. As a consequence a correction has to be made before combining the results of both halves.

The mechanical infrastructure in the vertex tank will be the same as for the VELO system, the heat production is a factor 2 less. In contrast to the VELO system the material budget is not important in the backward direction.

3.2 Beetle chip

The requirements on the readout chip for the Pile-Up VETO system are less strict than for the VELO system: an S/N ratio of 6 is sufficient. The Beetle chip [13] (fig. 11) is selected for this particular application because of the presence of a comparator output per 4 input channels to be used in the Pile-Up VETO processing. The strip signals are also stored in the analog pipeline and can either be forwarded to the ODE in analog or binary mode by the Beetle chip. The common mode noise contribution to the signal should be small.

The present Beetle chip of generation 1.1 is under test [14]. The next generation 1.2 will have an improved preamplifier part [15]. This version has been submitted in Spring 2002. These chips will be mounted on a hybrid and tested. Radiation hardness already has been shown for up to 10 Mrad.

3.3 Hybrid design

The design for the Pile-Up VETO system follows the criteria as described for the VELO system [1]. Compared to the VELO system the number of signal paths is higher by the extra LVDS signal pairs from the comparators. The number of connections for 16 Beetle chips per hybrid is:

- 64 analog signal pairs
- 256 LVDS comparator signal pairs (extra compared to VELO)

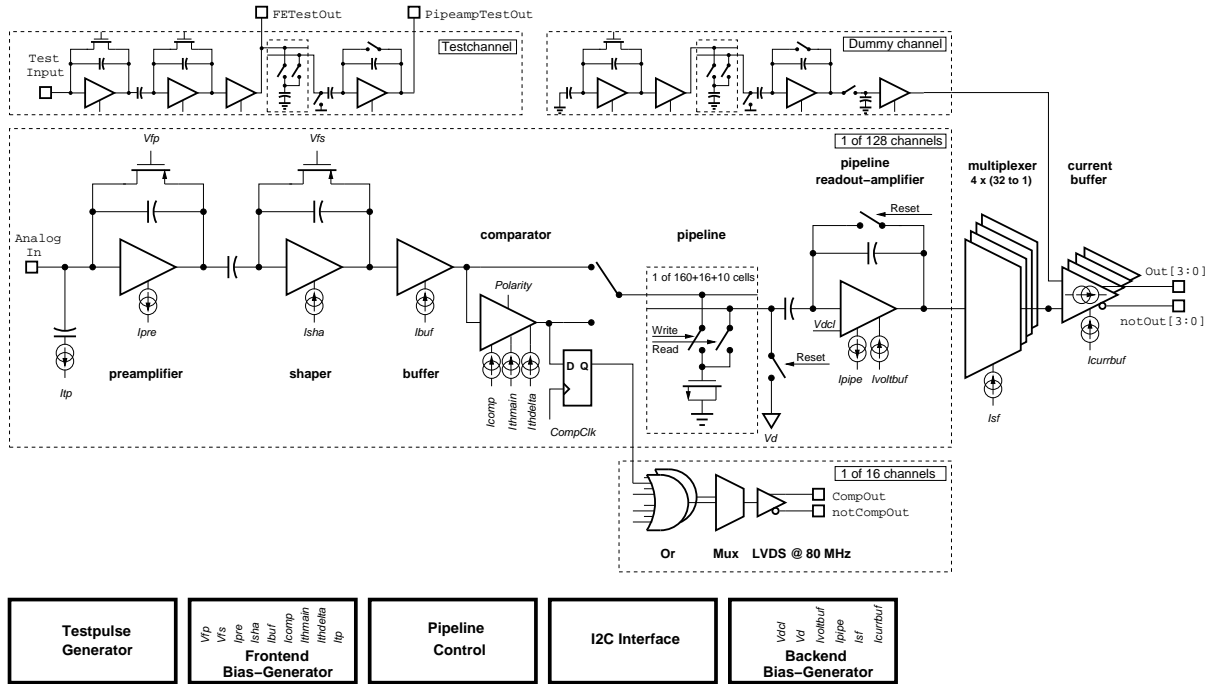


Figure 11: Beetle schematics.

Because of these extra connections the complexity of the hybrid is higher.

Features of kapton based technology as selected as baseline option, are:

- ≥ 8 layers
- 100 μm traces and spacing
- 350 μm vias (through holes)
- 500 μm vias (by spacing)

An 8-layer prototype hybrid has been designed [16] (see fig. 12) and is now in production. A R-detector will be bonded to it. This combination will be extensively tested for crosstalk and noise.

3.4 Cabling

The output lines of the Beetle chip are LVDS conform. As for the hybrid crosstalk is a concern. A careful analysis has to be made to select the correct conductor width and pitch to minimise signal loss and crosstalk. Also for selecting the required characteristic impedance as close as possible to 100 Ohm, this is important.

Apart from electronic requirements other constraints for the cable are:

- **Out-gassing:** in the secondary vacuum the vacuum properties of the cable material should be excellent to avoid additional residual pressure.
- **Flexibility:** for a lifetime of 15 years the cables are compressed and stretched about 5000 times

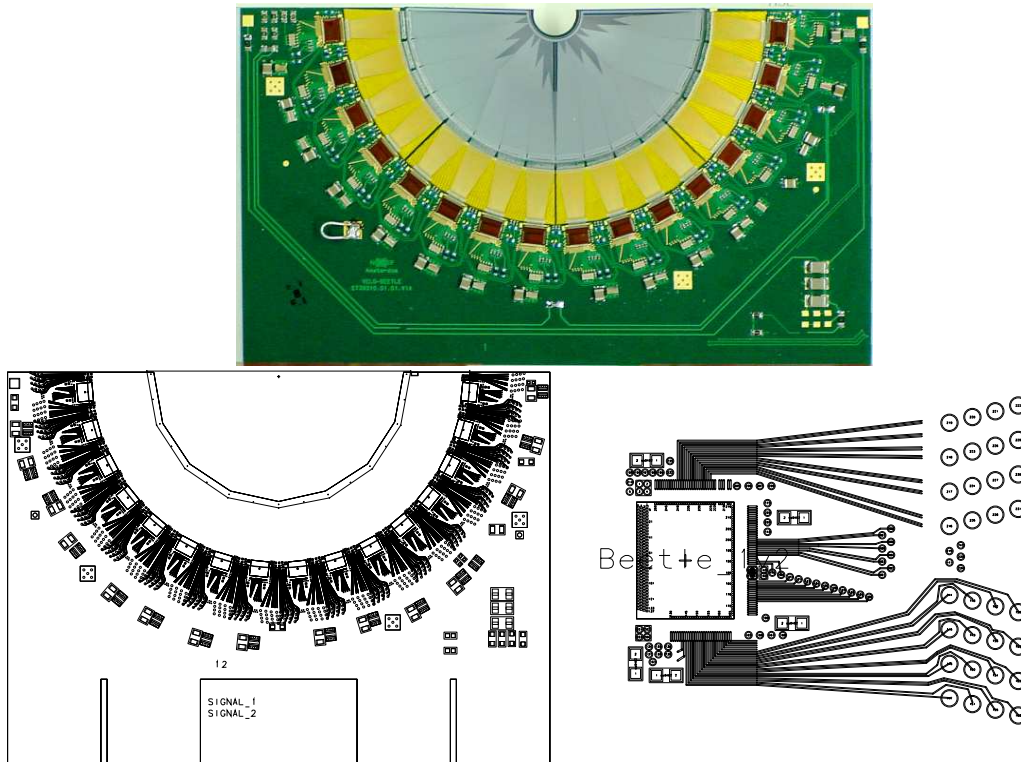


Figure 12: Beetle Velo prototype hybrid (above) and PileUp VETO hybrid design with detail (below).

- Radiation hardness: the radiation level at the connector side of the hybrid is estimated to be about 200 kRad/year. The hybrid and cables should be able to sustain that rate for the lifetime of detectors and Beetle chips (> 2 years).

When comparing two different possibilities: differential microstrip and stripline, the latter has the following advantages:

- well defined impedance independent of routing trajectory
- good shielding

and disadvantages:

- lower characteristic impedance
- less flexible

Considering the different requirements Kapton stripline has been selected as baseline option because of its good electronic properties and because of the folding endurance of Kapton films. Moreover, Kapton has excellent radiation properties, withstanding MRads of radiation. The properties of Kapton microstrip cables will be tested further to see whether they are indeed acceptable for use in the LHCb environment.

3.5 Repeater Station

If the characteristic impedance of the Kapton cable is 100 Ohm, the Beetle chip might be able to drive about 10 m of cable. In that case no Repeater Station modules are needed for transmitting

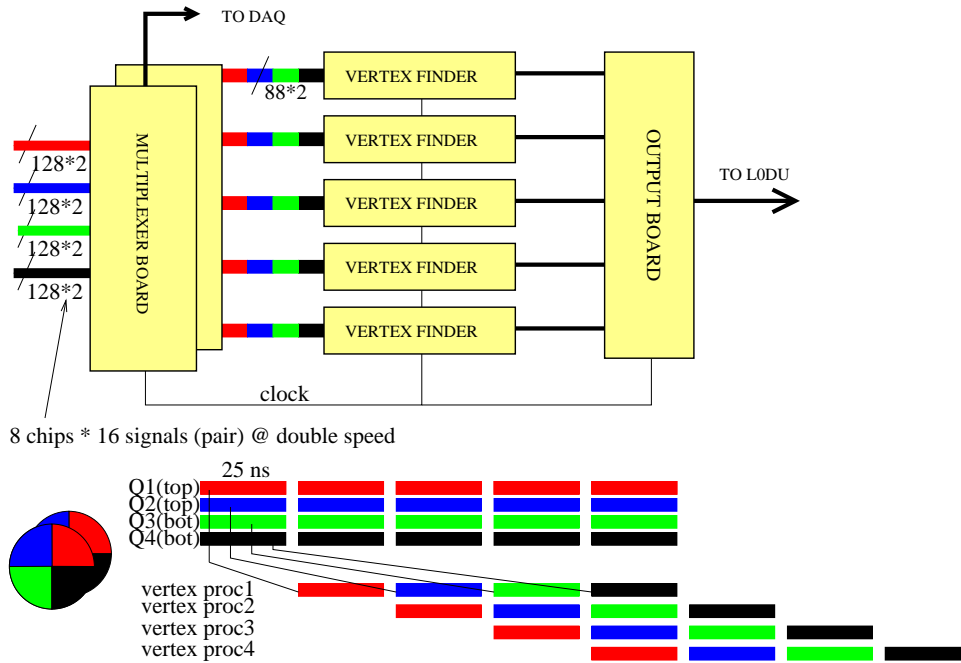


Figure 13: Schematic overview of the pile-up veto processing, assuming 512 input signals. The process of multiplexing and serialising of the data is also indicated.

the digital output, provided the optical transmission boards can be placed at that distance in a more or less radiation free environment (estimated rate at 10 m: < 100 rad/y). Otherwise the Repeater Station should contain modules with radiation hard LVDS drivers (estimated rate: ~ 20 kRad/y) to bridge the additional distance.

LVDS radhard drivers are available from Aeroflex [17], devices from other manufacturers will be tested for radiation hardness as well.

3.6 Optical link

As for the L0-Mu system optical transmission is seen as the baseline solution for transporting the signals to the VETO-system. Using LVDS for distances of about 60 m is not feasible at a rate of 80 MHz without applying line equalisers.

For the L0-Mu trigger prototype tests have been performed using a TLK2501 (16-bit, 80 MHz) Serializer chip and Method optical transceiver module. The Method transceiver has been replaced in the meantime by an Ribbon Optical Transceiver from Agilent. The bit error rate is negligible ($< 10^{-14}$ up to 2.5 GB/s). The synchronisation with the LHCb clock is foreseen by using a VALID pulse signalling the beginning of a LHC cycle. The effect of SEU on the system should be studied further.

The development work by the L0-Mu group will be followed closely.

3.7 Architecture of the Veto processing system

The processing of the vertex finding algorithm (fig. 13) is performed in the Vertex Finder Boards. Input data are multiplexed and serialised by the Multiplexer Boards. Processing results are de-multiplexed by the Output Board. Each Vertex Finder Board processes one event as indicated. In case of 1024 input signals the number of Multiplexer Boards will double and the

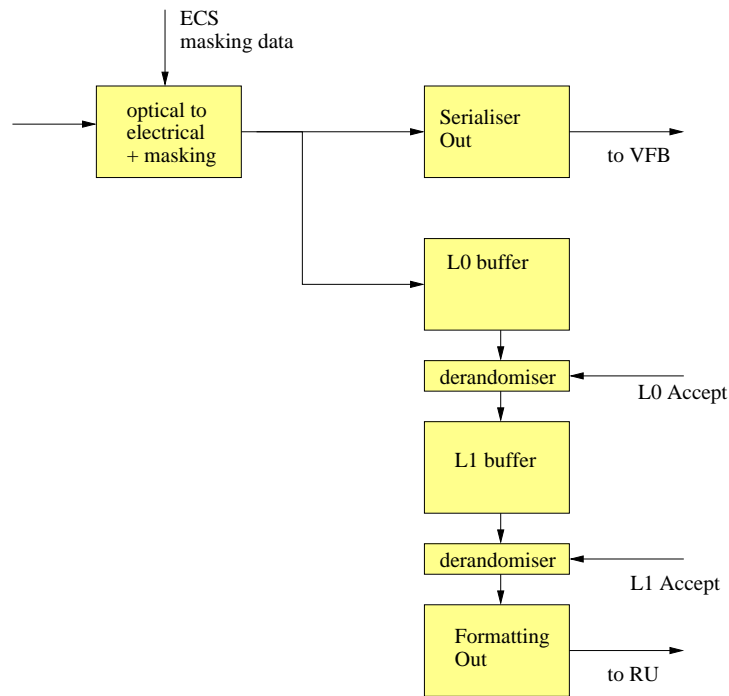


Figure 14: Functionality of the Multiplexer Board.

input signals will then be OR-red at the Multiplexer Board level. Just one 9U crate is needed for the processor system.

A standard solution for a SC host (i.e. Credit-Card PC) will be used (see also Appendix A) for :

- Loading configurations
- Checking data
- Debugging the system
- Reading data when stand-alone
- SC monitoring

3.7.1 Multiplexer Board

The number of input signals is 1024 if the signals are not combined at the Si-detector level (see 3.1). In case detectors with combined 45 degree sections will be used, the number of input channels is 512. So either 8 or 4 optical ribbons will be connected to 4 or 2 Multiplexer Boards. The optical to electrical transition will be directly at the Multiplexer Board level (fig. 14). Each Multiplexer Board is connected to all Vertex Finder Boards. In the Multiplexer Board the data will be round-robin routed to the Vertex Finder Boards. Planned is to copy the input data directly into memory (L0/L1 buffer) from where the data are sent out to a DAQ Read-Out Unit (RU) over an S-link.

3.7.2 Vertex finder

In total 5 Vertex Finder Boards are planned to be used. Four of them handle subsequent events. The fifth one is a spare processor board that can be used for checking the results of the others. Minor configuration constants as threshold levels should easily be changed. That will not be the case for different types of algorithms. Therefore, algorithms for different situations will be pre-programmed and loaded on demand.

For the prototype development the vertex processor algorithm (see section 1.3) has been described in VHDL and, since the code is too big for just one FPGA, has been translated in code for several large FPGA's. Xilinx FPGAs have the advantage of having many LVDS inputs and outputs. The XCV3200E is the largest at the moment of the Xilinx Virtex-E 1.8 FPGA family with 4 M system gates. In practice the device utilisation is about 70%. The number of differential input/output pairs is large: 256. Timing analysis shows that the required 40 MHz operation is feasible. Future FPGA's are expected to be even larger than the XCV3200E, giving perhaps the possibility to combine all tasks in just one FPGA.

In fig. 15 and fig. 16 the schematics of the prototypes of the Vertex Finder Board (FVB) and Test Board are shown. All functionality of the VFB is contained in 2 Xilinx Virtex XCV3200E devices. A third, smaller FPGA on the Test Board houses the VME-interface and the logic to supply test patterns to the VFB. All LVDS input and output signals of the Vertex Finder Board go via connectors on the front-panel, providing an opportunity to input external test patterns directly. The input data are 192-bit wide at 40 MHz of which 32 bits are reserved for data labelling and synchronisation (BCID etc.). The test patterns are loaded via VME into the FPGA on the Test Board, that stores the patterns in memory. The left FPGA on VFB correlates the patterns of the 2 Si-wheels and searches for the highest peak in the histogram. Then the input bits related to the peak are removed from the data stream that is passed on further to the right FPGA. Here second and third highest peaks are searched for. Upon receipt of a software trigger the patterns are sent to the VFB at full speed. The minimum memory depth for storing the patterns is 64 (192*2 bits wide). This is larger than the depth of the pipeline in the VFB. To monitor processing in both FPGAs on VFB several registers are added to these FPGAs that capture part of the data stream. The data of those registers are shifted into the FPGA on the Test Board that in turn is read via VME.

The layout on the 12-layer PCB was complicated because of the large number of inputs/outputs. Critical parts of the layout were hand routed, while the rest was done by dedicated automatic routing software. The results are shown in fig. 17. The board is now ready for tests.

3.7.3 Output Board

The Output Board interfaces the processor system to:

- L0DU [18]: data are sent over copper RJ45 cables in 32-bit words. The data format for the Pile-Up VETO is given in Appendix B.
- Host Board: input and output data can be spied upon via the VME-bus for debugging purposes. Clearly, this alternative data stream should not block the normal data-acquisition.

3.7.4 Latency

The total latency, as estimated for the TP, is specified in Table 4. The exact implementation in the FPGA code will strongly influence the final outcome. First results for the prototype VFB

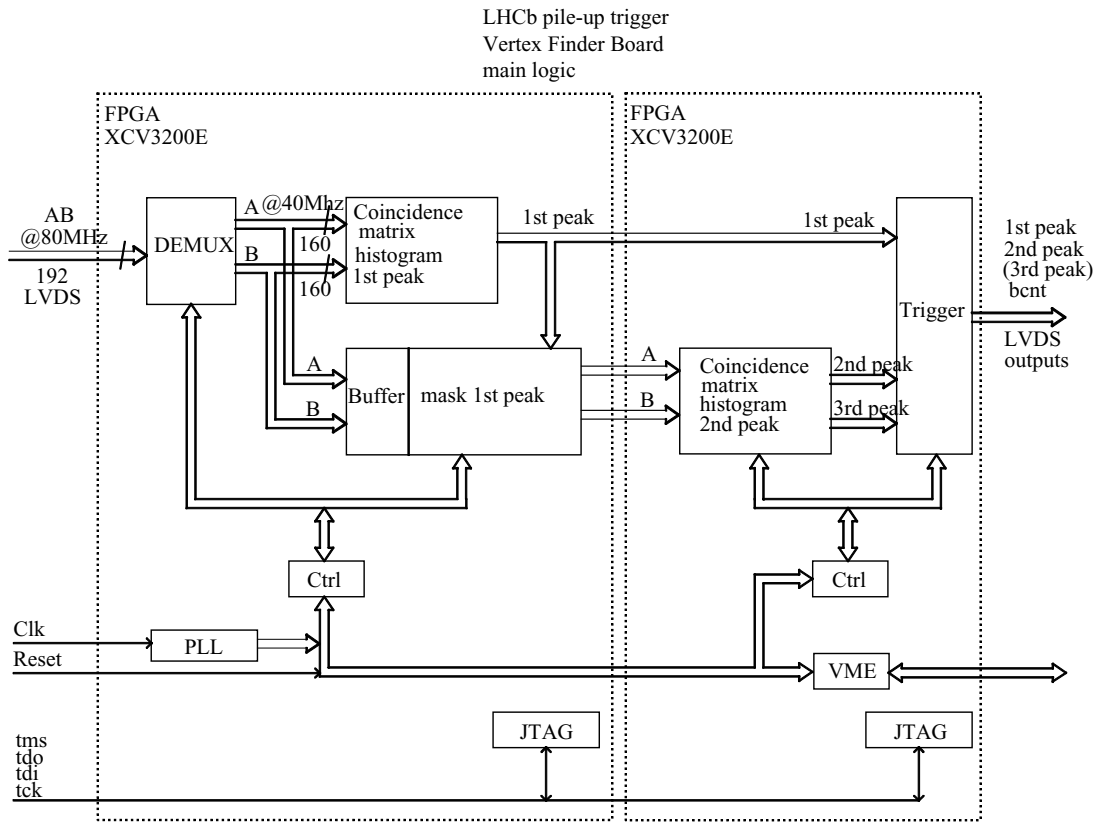


Figure 15: Prototype Vertex Finder Board diagram.

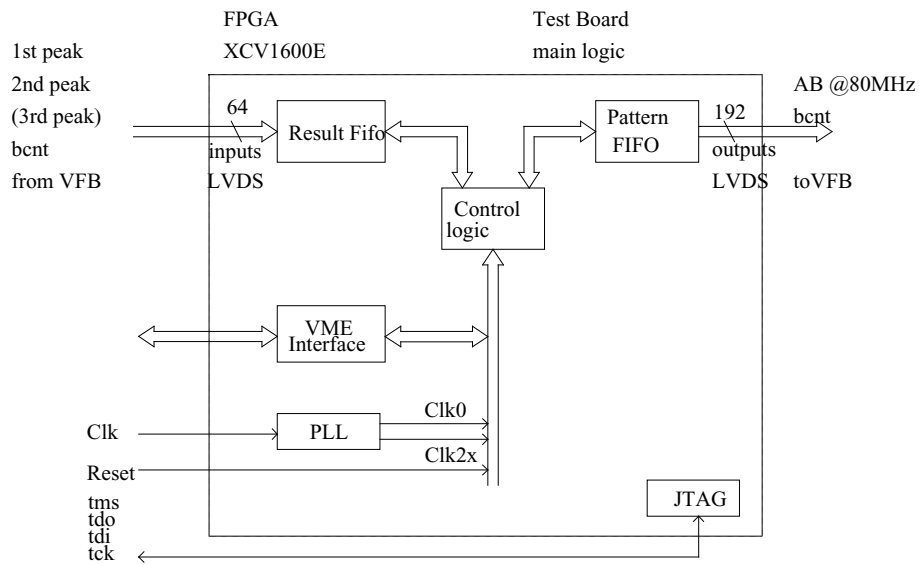
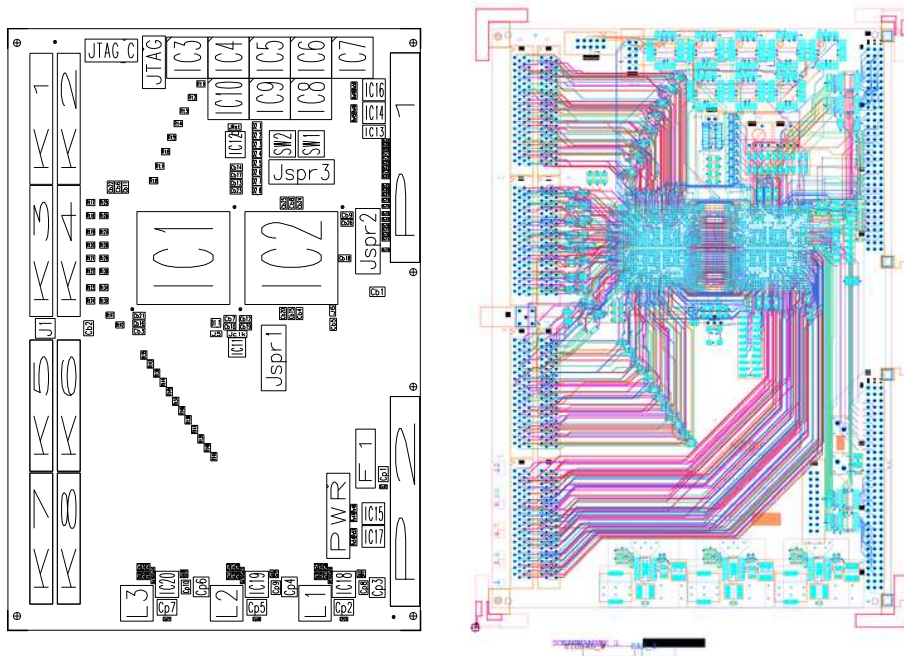


Figure 16: Test Board diagram.





 Amsterdam

 LHCb Pile-up Beetle

 Vertex Finder

 ET39350_01_01_v1

Figure 17: Vertex Finder Board component placement and routing.

Step	Latency (ns)
Time of flight	0.6
Detector to Beetle	1.0
Beetle to Pile-Up VETO system	364
Pile-Up VETO processing	$(2 \times) 625$
Synchronisation	75
Pile-Up VETO system to L0DU	16 ns
Total	1082 (or 1707)

Table 4: TP Latency of the Pile-Up VETO processing.

show a latency as expected.

3.8 Other Interfaces

3.8.1 DAQ

The input data to the Pile-Up VETO system are part of the L0 data stream, the output data are part of the L1 data stream. The Beetle comparator data part will be read-out and input into the L1 DAQ.

The Pile-Up VETO system is part of the Trigger partition. This means that the data has to be included in the Trigger data stream. The Beetle L1 data is part of the VELO partition. Moreover, in case the VELO is running its own partition the trigger data should preferably be available in that partition as well.

Envisaged is to use as much as possible standard components of the VELO or the central DAQ system. An ODE board (fig. 18 [19]) can be used for the Beetle output, either in selectable binary or analog readout mode. The data to be included in the LHCb data stream flows via the L1 Buffer. The other route could in principle be used to spy on Beetle data for debugging

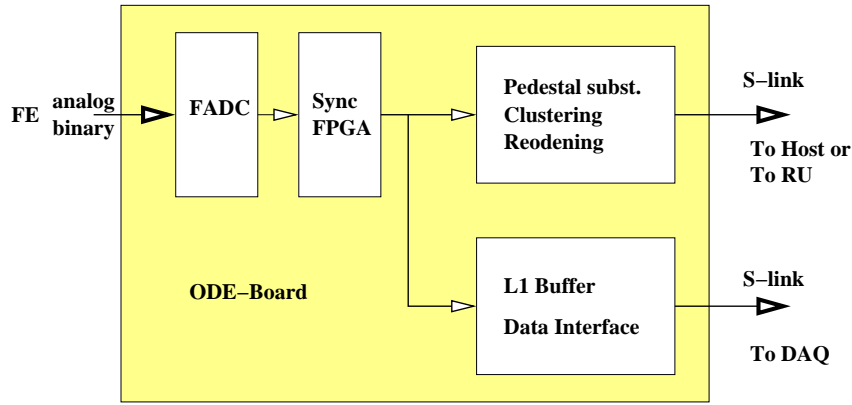


Figure 18: Simplified schematics of the ODE-board.

purposes. Four ODE modules are needed for the two planes.

The Output Board (fig.19) provides data to the DAQ. Standard Read-Out Processor Modules [20] [21] should combine all data of the PileUp VETO system.

4 Calibration and monitoring

User interaction is needed for several purposes:

- Alignment: after reaching luminosity the detectors will be put in place. Although the requirements on alignment are not very stringent, a check should be made whether the detectors are at the correct positions. The check should in principle be similar to that for the VELO.
- Noisy channels: channels that give spurious hits could flood the processing system with uncorrelated entries. Automatically these channels should be looked for and removed from the input of the processing system.
- Readout: the input signals for the VETO system can be recreated from the Beetle binary or analog output. Regularly an offline check has to be performed to see whether the results of online and offline processing agree.
- Checks: the number of entries in the histograms and the location of the vertices should be followed closely to check the behaviour of the system and the machine background conditions.
- Tests: test patterns can be fed into the Beetle chips and in the processing system to check the overall processing of the system.

5 Luminosity Monitoring

For periods of in the order 5 to 60s the output of the Pile-UP VETO system has to be counted for the number of vertices: 0/1/2(/more). This counting is performed in the Output Board. The data will be part of the ECS data stream.

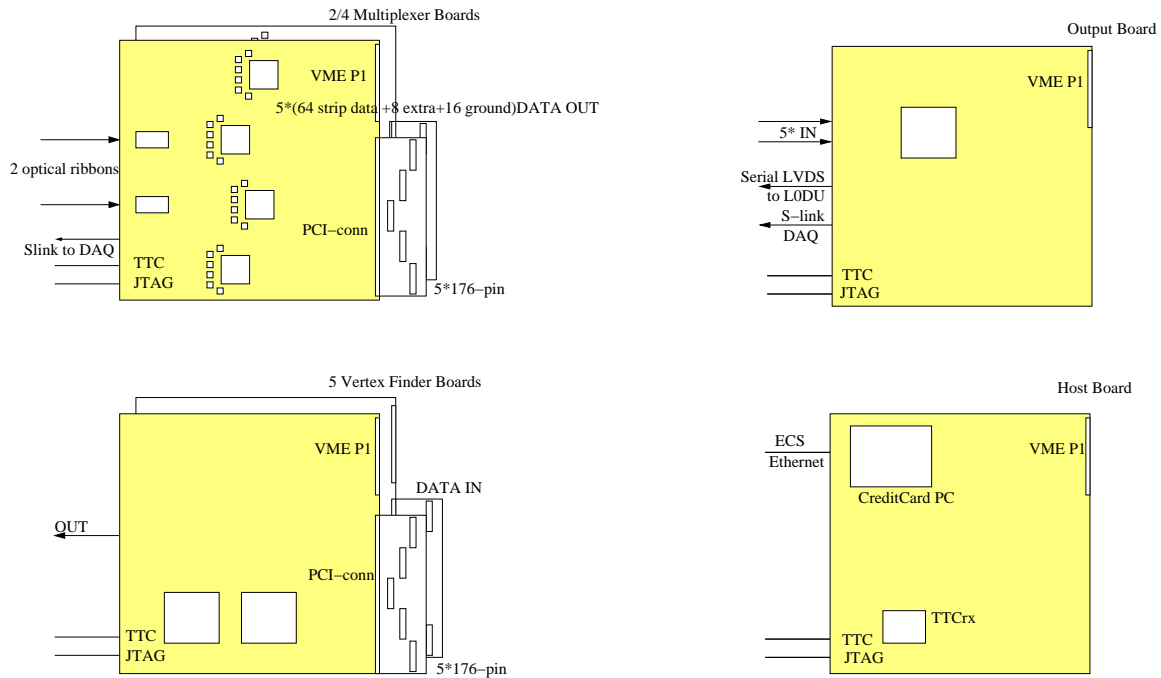


Figure 19: Data connections.

Whether the algorithm can be used when the detectors are in an intermediate position and not in the final position, is under study.

References

- [1] LHCb collaboration, "The VELO TDR", CERN/LHCC 2001-0011.
- [2] N. Zaitsev, "Study of the LHCb pile-up trigger and the $B_s \rightarrow J/\psi \phi$ decay", Thesis, University of Amsterdam, 2000.
- [3] W. Hoogland et al., "Status report on the development of the primary vertex fast reconstruction", LHCb-97-004.
- [4] W. Hoogland et al., "The use of silicon detectors for fast primary vertex reconstruction and pile-up rejection", LHCb-97-016.
- [5] N. Zaitsev and L. Wiggers, "The LHCb Vertex Triggers", NIM A 447(2000)235.
- [6] G. Wilkinson and N. Zaitsev, "Choice of running luminosity for LHCb and performance of pile-up tag", LHCb-97-014.
- [7] N. Zaitsev, "The luminosity measurement at the LHCb", LHCb-98-053.
- [8] N. Zaitsev, "The luminosity optimization and level 0 trigger control", LHCb-2000-008.
- [9] T. Bowcock and G. Casse, "Operating conditions for the VELO silicon", LHCb-2001-069.

- [10] H. Dijkstra, private communication.
- [11] R. Bernier et al., "SPAC: Serial Protocol for the ATLAS Calorimeter, 1998.
- [12] J. Christiansen, "Requirements for the L0 front-end electronics", LHCb 1999-029 Trigger.
- [13] N. van Bakel et al., "The Beetle Reference Manual", LHCb-2001-046.
- [14] Tests underway at CERN, note to be produced.
- [15] Tests underway at NIKHEF, note to be produced.
- [16] M. van Beuzekom, private communication, note to be produced.
- [17] Documentation: www.utmc.com
- [18] P. Perret, private communication, note to be produced.
- [19] A. Bay et al., "LHCb VELO off detector electronics preprocessor and interface to the Level 1 Trigger", LHCb VELO 2001-043.
- [20] IBM PowerNP 4GS3 network processor datasheet.
- [21] J-P Dufey et al., "Use of Network Processors in the LHCb Trigger/DAQ system", presented at LEB2001.

who	always	non-active state	active state
expert	read configuration data view hw status prepare configuration files	debug system initialise/reset load configuration	get spy data check consistency data

who	begin of run	active state	end of run	debugging mode
shift	select configuration check overall system	check data histogram vertices error logging	get summary results	interact with expert run debug tools

Table 5: Tasks for expert or person on shift.

Content	no. bits
BCID	8
error	4
more peak info	4
peak position1	8
content1	8
BCID	8
no. hits	8
peak position2	8
content2	8

Table 6: LODU data format.

A Slow Control

Outside users must be able to log-in to the system, monitor the system from their home laboratory and change software when the systems are offline. In detail, the expert or person on shift must be able to do the tasks as described in Table 5.

B Data Format

The format, aligned on 8/16/32 bits, of the PileUp VETO data sent to the LODU, has preliminary been defined (see Table 6).