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RasMuX

The multiplexer for the RasNik alignment system.

The RasMuX is the multiplexer of the RasNik alignment system. It connects a maximum of 8 cameras and 12 LEDs. Using JTAG commands, power of the connected components can be switched on and off. One of the video inputs is selected, buffered and send to the framegrabber, which is part of the total system. The card also convert JTAG commands to I²C standard to send instructions to a sensor or read its settings.

PRELIMINARY

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Introduction

The basic idea is to create an image of a coded mask on an optical sensor by means of a lens. The mask is lit by an infrared LED. In this set up the relative position in X and Y direction is measured along the line mask, optical center of the lens and the sensor. Also the (relative) rotation of the mask or the sensor can be measured. By calculating the actual image spot size and comparing this with the mask spot size, the position of the lens along the Z-axis is calculated. Also the relative rotation around the X and Y-axis of the mask in respect to the CCD sensor can be calculated.

The system can be split into three major components

1. The optical system:

- a coded mask
- a lens
- an optical sensor

2. The sensor and framegrabber combination (video):

The optical sensor is a commercially available B&W observation camera, without a lens. This can be a CCD type or CMOS.

The framegrabber is a commercially available 8 bit grayvalue type E.G. Data Translation DT3152. The RasMux connects a number of sensors to the framegrabber.

3. The reconstruction software ICARAS.

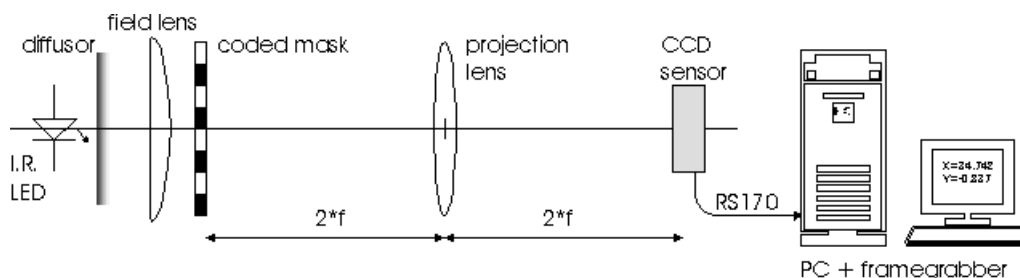


Figure 1: Basic RasNik system

This paper describes the multiplexer (RasMux), which connects a number of sensors to the framegrabber. Details of the coded mask can be found at:

http://www.nikhef.nl/pub/departments/et/ccd_rasnik/restricted/code.pdf or printed as NIKHEF paper ETR 94-10.

The multiplexer described here is a prototype that can be used during chamber production and in test set-ups. This version is not radiation tolerant. Furthermore we are still investigating the optimum number of RasCam and RasLed connections per RasMux.

A maximum of 12 LEDs (RasLeds) can be connected of which maximum 2 can be switched on at the same time. A maximum of 8 RasCams can be connected of which maximum 2 can be switched on at the same time. This limited on the board and cannot be changed by commands. The video and pixel clock signal from one of the active sensors is transmitted to the output. Commands are given using a differential JTAG interface port. Settings can be read via the same interface.

Specifications:

The video standard used is CCIR. The video signals from the sensors are semi differential. The output to the MasterMux is fully differential. For test set-ups a BNC connector can be mounted to interface to a frame-grabber directly (1 V video).

The clock from the RasCams uses LVDS (Low Voltage Differential Signalling) levels. The output to the MasterMux uses RS485 (differential) levels. For test set-ups a LEMO connector can be mounted to obtain a TTL compatible output.

For slightly larger test set-ups two RasMuxes can be cascaded using the RJ45 output connector. This reduces the number of sensor inputs on the other RasMux by one.

The RasMux converts certain JTAG instructions to I²C commands. The I²C bi-directional bus is used to control and monitor various settings on the RasCams.

The module requires three supply voltages, which are supplied by the MasterMux or MasterBrico. If these modules are not available, the required supplies are 8, 15 and 28 V. The RasMux draws app. 250 mA from the 8 V input, 20 mA plus 100 mA for each active RasCam from the 12 V input and 20 mA plus 70 mA for each active RasLed from the 28 V input.

RasCam connections (RJ45 connector)	
Pin	Function
1	SDA: The data signal of the I ² C bus.
2	9 to 12 V power supply input.
3	+Video output.
4	+Pixel clock output.
5	-Pixel clock output.
6	-Video output.
7	Ground, 0 V
8	SCL: The clock signal of the I ² C bus.
Case	The shield of the cable is connected to sensor housing. Shield is connected to ground via 10 kΩ.

RasLed connections (RJ11 connector)	
Pin	Function
1	Shield
2	24 V
3	0 V
4	Shield

RasMux

MasterMux connections (D25 male connector)		
Pin		Function
1		Shield
16		28 V
21		15 V
23		8 V
4, 9, 11, 13, 25		Ground
Pos.	Neg.	Note: All active signals are differential.
14	2	Spare. Bi-directional spare pair, RS485.
15	3	TCK (JTAG)
17	5	TMS (JTAG)
18	6	TDI (serial JTAG data to the RasMux)
19	7	TDO (serial JTAG data from the RasMux)
20	8	Trigger. A spare line to the RasMux, RS485.
22	10	Pixel clock, RS485.
24	12	Video out, differential 1V.

JTAG

The serial protocol to communicate with the RasMux follows the JTAG standard. The electrical implementation is fully differential (RS485). All lines are terminated at one end. The interface is used to control the power supplies of the sensors (RasCam) and LEDs (RasLed) and to send commands or read settings of the sensors. RasMux translates the JTAG commands to the I²C protocol understood by the sensors and stores result data into a buffer that can be read via JTAG again.

JTAG registers		
IR	Name	Bits
0000	SelCam	8
0001	SelLed	8
0010	Write I ² C	24
0011	Read I ² C	32
0100	Status	8
0101	Generation date	24
Others	Bypass	1

SelCam register (IR=0000)

The *select camera* register determines which RasCams are switched on. The lower half of the register also determines of which sensor the video and clock signals are transmitted by the RasMux. The upper half determines which sensor is switched on to be used next in the sequence. In this way the automatic gain and exposure settings of the sensor have time to stabilize during the period an other sensor is digitized. Also the RasLed to be used next in the sequence should be switched on.

To save on power, all cameras can be switched off.

Bits	power-up	Result
3:0	1111	Select sensor to be used.
7:4	1111	Select sensor to be used next.
1000...1111 disables this output.		
The bits 3:0 also switch the video multiplexer and pixel clock multiplexer.		

SelLed register (IR=0001)

The *select LED* register determines which RasLeds are switched on. Two RasLeds may be switched on at the same time.

Bits	power-up	Result
3:0	1111	Select a LED to be switched on.
7:5	1111	Select a LED to be switched on.
1100...1111 disables this output.		

RasMux

The RasMux translates some of the JTAG commands into I²C commands, for the protocol part and for the electrical interface part. Also settings of the RasCam can be read from this I²C bus via RasMux. Communication is only possible when the addressed RasCam is switched on. On power up the RasCam hardware generates a continuous pixel clock which is phase locked on the pixel valid output of the sensor (see RasCam description). When any I²C bus operation is performed, this circuit is disabled and the sensor settings apply. For normal operation one should first enable the free running pixel clock. This, for proper operation of the framegrabber.

Write I²C (IR=0010)

Data written into this register will be send to the selected RasCam. Or it may start a read out sequence on the selected I²C bus. If the cycle starts a read out sequence the data is ignored. Power of this RasCam must be switched on. Once the power of a RasCam has been off, it returns to its default settings. A write operation takes app. 700 μs (6 ms when the clock divider is set to 8). A read instruction takes app. 1.2 ms (9.6 ms when the clock divider is set to 8).

Bits	Result
15:12	I ² C header code, don't care when bit 16=0.
11:0	I ² C write data, don't care when bit 16=0.
16	1 Start a write cycle.
	0 Start a read cycle.
18:17	I ² C sub address. Default on RasCam 00.
20:19	Must be 00.
23:21	RasCam selection.

Read I²C (IR=0011)

From this register the data can be read after the read operation on the I²C bus has finished. This is initiated by a write operation and it's termination can be monitored via the status register.

Status register (IR=0100)

From this register status and errorbits can be read.

Bit	Result
7	I ² C operation in progress.
6,5	00
4	Write attempt to reg. 0010 while I ² C operation in progress failed.
3	Address acknowledge on I ² C bus failed.
2	Data acknowledge on I ² C bus failed.
1	RasLed driver failed.
0	RasCam driver failed.
These bits are reset by the JTAG read operation (destructive read), except when the condition persists.	

RasMux

Generation date (IR=0101)

From this register the generation date of the firmware can be read.

Bit	Result	Last version
23:20	0000	0000.
19:9	11 bits for year	11111001111: 1999.
8:5	4 bits for month	1011: October.
4:0	5 bits for day of month	01010: 10 th .

RasMux

Important notice: The following information is largely taken from Vision's¹ VV5430 documentation. Though the most important features have been tested, there may be some inaccurate or incomplete data here. There are -at some points- differences with the original VVL documentation due to our specific implementation of the sensor on the RasCam.

I²C

I ² C registers		
Headercode	Name	Comments
0000	Invalid	
0001	Set-up 1	Basic functionality
0010	Set-up 2	Pixel control and read
0011	Coarse exposure	AEC must be 0
0100	Fine exposure	AEC must be 0
0101	Gain control	AEC must be 0
0110	Invalid	
0111	Invalid	
1000	Lower exposure threshold	
1001	Upper exposure threshold	
1010	Analog control	
1011	Invalid	
1100	Invalid	
1101	Invalid	
1110	Set-up 3	Pixel synchronization
1111	Invalid	

¹ VLSI Vision Limited - A company of the ST Microelectronics group.

Setup register_1

The setup register_1 is used to select different basic operating modes:

Setup register_1, header code = 0001, valid data bits: 11			
Bit	Default	Function	Comment
0	0	Normal/Backlit	Selects between normal and backlit exposure modes. The power-on default is normal mode. See below.
1	0	Linear mode ²	Selects between a linear (LIN=1) or gamma corrected video signal.
2	1	Auto gain enable	When set 0, the current gain value selected is frozen. With AGC=0 a new gain value can be written to the gain register via the serial interface (header code 0101).
3	0	Inhibit black calibration	Disables automatic gain control
4	1	Enable Auto exposure Control	When set 0, the current exposure value is frozen. When automatic exposure control is inhibited then automatic gain control is also disabled. With AEC=0 a new exposure value can be selected by writing to the coarse and fine exposure registers via the serial interface (header codes 0011 & 0100).
5	0	Horizontal shuffle enable	Shuffles the read out of the horizontal shift register. Even columns read out together then odd columns.
6	0	Vertical shuffle enable	Shuffles the readout of the vertical shift register. Even lines read out together then odd lines.
7	1	Force black calibration	Requests a re-calibration of the black level while bit is low.
8	0	Clock divisor DIV0	System clock division ³ : 00= $\div 1$; 01= $\div 2$; 10= $\div 4$; 11= $\div 8$
9	0	Clock divisor DIV1	
10	1	Internal Register	must be set for correct operation.
11	0	Not used	

The backlit mode reduces the area that is used by the auto exposure algorithm from 80 to 25 % of the active area. This mode improves the contrast of the foreground objects in scenes with a bright background.

² The gamma corrected mode is disabled by hardware on the sensor board. See the RasCam description under *options*.

³ Decreasing the system clock rate proportionately increases sensor sensitivity (by increasing exposure time), but also decreases frame frequency. System clock must be x1 for standard CCIR or EIA framing.

Setup register_2

The setup register_2 is used to select read data, valid pixels and video output operating modes:

Setup register_2, header code = 0010 valid data bits: 12			
Bit	default	Function	Comment
0	0	Read mode A	Select shadow read mode, bits 0,1 are mutually exclusive.
1	0	Read mode B	
2	PVE	Pixel sample clock select.	Pixel sample clock mode. See table below. Bit 1 is set by the PVE pin level. ⁴
3	0		
4	0	Not used	Must be set to 0 for correct operation.
5	0	Enable free running pixel clock	Overrides bits 3 and 2.
6	0	External pixel thresholds	Use external algorithm thresholds in exposure controller.
7	0	Not used	Must be set to 0 for correct operation.
8	0	Not used	Must be set to 0 for correct operation.
9	0	Shuffle Modes, bits 2, 1 and 0.	Video output enable control bits. See table <i>Shuffle Modes</i>
10	0		
11	0		

Bit 0 and 1 show a problem, needs further investigation (use 00 for mode A).

Pixel sample clock mode (bits 3 and 2 of set-up register 0010)			
Bit			Pixel clock pin output.
5	3	2	
0	0	0	Disable pixel valid clock pin output.
0	0	1	Qualify image area only (as defined for CCIR or EIA)
0	1	0	Qualify central 256 x 256 pixels (CCIR only)
0	1	1	Pixel valid active only during interline periods of visible image lines.
1	X	X	Enable free running pixel clock

A more extensive description will follow after testing.

Shuffle modes (bits 11, 10 and 9 of set-up register 0010)			
Bit			Area where the video output is active.
11	10	9	
0	0	0	All (normal operation)
0	0	1	None. Video output in tristate.
0	1	0	Sync only.
0	1	1	Sync plus Q1 image.
1	0	0	Q1
1	0	1	Q2
1	1	0	Q3
1	1	1	Q4

Four times
192 * 142 pixels

Q1	Q2
Q3	Q4

For more detailed information (timing etc.) see the VV5430 datasheet.

⁴PVE is set to one by hardware on the sensor board. See the RasCam description under *options*.

Coarse and fine exposure registers.

For external exposure control (AEC = 0) the exposure value can be set via the serial interface (header codes 0011 and 0100). The 18 bit exposure control value is formed from two 9-bit values, coarse and fine. Values written that exceed the mode dependant maximum will be ignored and the maximum will be used.

Header code	Function	CCIR		EIA	
		Min	Max	Min	Max
0011	Coarse, 9 bits	0	310	0	260
0100	Fine, 9 bits	0	404	0	325
Bits 11:9 are not used.					

Lower and upper pixel count thresholds

The lower and upper pixel count thresholds are used by the automatic exposure controller. The power-on default values for TL and TH are exposure mode and video mode dependant. If the external pixel threshold control bit (bit 6 in setup register_2) is set the internal default values for T1 and T2 are overridden by the serial interface values. Note that only the most significant nine bits of each seventeen bit threshold can be controlled.

Header code	Function
1000	Lower pixel count threshold, 9 bits.
1001	Upper pixel count threshold, 9 bits.
Bits 11:9 are not used.	

Gain register

The gain register is used to select an external gain value when automatic gain control is inhibited (AGC = 0) and to set the gain ceiling while automatic gain control is active (AGC = 1).

Gain and gain ceiling, header code = 0101, valid data bits: 4					
bit				Gain	Comment
G3	G2	G1	G0		
0	0	0	0	1	Default setting
0	0	0	1	2	
0	0	1	1	4	
0	1	1	1	8	Default gain ceiling
1	1	1	1	16	
Other settings				invalid	
Bits 11:4 are not used.					

Analogue control register

The analogue control register is used to control a number of parameters that define internal operations.

analogue control register, header code = 1010, valid data bits: 10		
Bit	Default	Function
0	1	Internal, must be set to 1 for correct operation
1	0	Internal, must be set to 0 for correct operation.
2	0	Internal, must be set to 0 for correct operation.
3	0	Disable anti-blooming protection
4	0	Internal, must be set to 0 for correct operation.
5	0	Internal, must be set to 0 for correct operation.
6	0	Enable external black reference
7	0	Enable external white threshold
8	0	Internal, must be set to 0 for correct operation.
9	0	Enable binairisation of video output. The threshold level above which a pixel is deemed to be white is set via the serial interface, header codes 1001 and 1000 (Upper and Lower Exposure Control Thresholds).

Setup register_3

The setup register_3 is used during sensor synchronization and when the pixel counter in the video timing logic is reset, either at the end of a video line or when the sensor is forced to synchronize externally.

setup register_3, header code = 1110, valid data bits: 7			
Bit	Default	Function	Comment
5:0	3	Video timing pixel counter offset	Variable offset that is added to the fixed pixel counter preset value when the counter is reset, at the end of a video line or when an external synchronization is applied
6		Enable SNO	Synchronizing signal to other cameras in multi-camera applications ⁵
Bits 11:7 are not used			

⁵ Enable SNO adjusts the timing of the FST signal (see the documentation of RasCam, the *options* section) to correctly synchronize external slave cameras. Alternatively, the synchronizing signal for all cameras can be generated externally, which may be more useful in image processing applications.

Read data

Data read from the sensor depends on the setting in Setup register, bits 1 and 0, see table *Setup register_2*.

Read mode A, 32 bits	
Bit	Function
3:0	Camera ID code.
4	Undefined.
5	Backlit mode. This bit only reflects the state of the BKLIT pin, not the combined result of the pin and the serial interface BKLIT control bit. This is set 0 on the RasCam.
6	Gamma correction mode. This is set 0 on the RasCam.
7	Auto gain control.
8	Internal black calibration enabled.
9	Auto exposure enabled.
13:10	Gain value
22:14	Fine exposure value
31:23	Coarse exposure value

Read mode B, 32 bits	
Bit	Function
16:0	White pixel count.
17	Black level monitor in progress.
31:18	Undefined