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ATMega128

A plug-on processor board.

**A general purpose plug-on board.
Most processor pins are accessible from the
main-board on which it is plugged. It contains
an RS232 converter and provides room for
extra EEPROM.**

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http://www.nikhef.nl/pub/departments/et/misc/atmega128/atmega128_wrd.pdf

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Specifications

Board size: 76 * 64 mm.

Processor ATMega128-16AI, Atmel documentation (5 MB):

http://www.nikhef.nl/pub/departments/et/misc/atmega128/atmega128_dat.pdf

Crystal: 14.7456 MHz.

RS232 via 2 * 5 pin connector, flat cable connection to standard DB9 (female) connector.

Programming via 2 * 5 pin connector from STK200/300 programmer (LED indication).

Two 26-pin connectors on the back of the board to connect to the main board (spaced 1.7 inch).

Connector for LCD display (or remaining port pins).

Power supply: 5 V or 7 to 9 V.

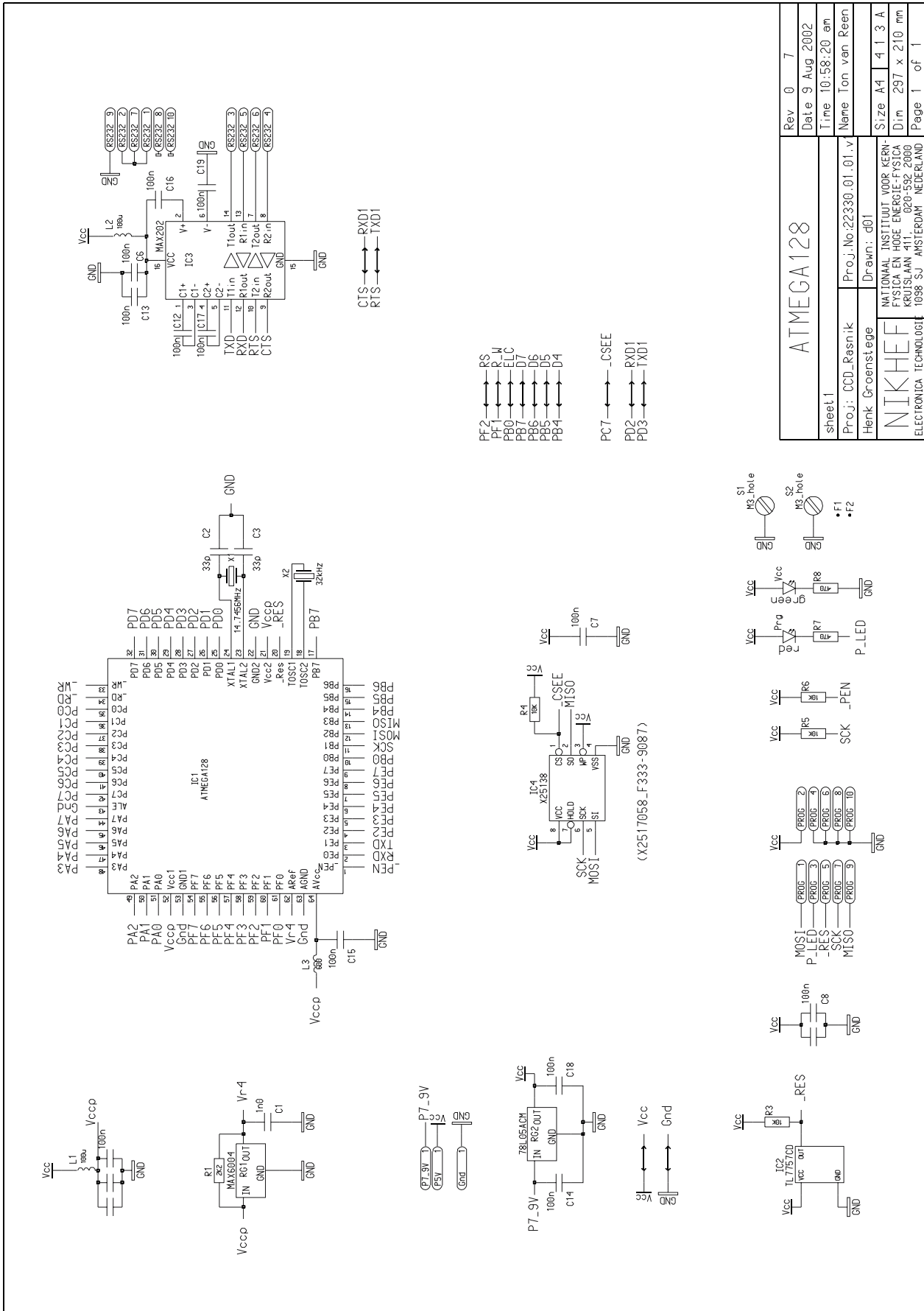
On board power-up reset.

32 kHz watch crystal.

Room for 8 pin SMD EEPROM with SPI interface.

A 4.096 V reference for the processors' ADC. If RG1 is not installed (using the processors' internal reference) remove R1 also.

ATMega128



ATMEGA128		Rev 0	7
sheet 1		Date	9 Aug 2002
Proj.No:22330.01.01.v		Time	10:58:20 am
Henk Groenst.ege		Name	Ion van Reen
Drawn: d01		Size	A4 4 1 3 A
NATIONAAL INSTITUUT VOOR KERN- FYSICA EN HOGE ENERGIE-FYSICA KROUSSLAN W11, 020-532 2000 ELECTRONICA TECHNOLOGIE 1958 SJ AMSTERDAM NEDERLAND		Dim	297 x 210 mm
		Page	1 of 1

Figure 1: Schematic

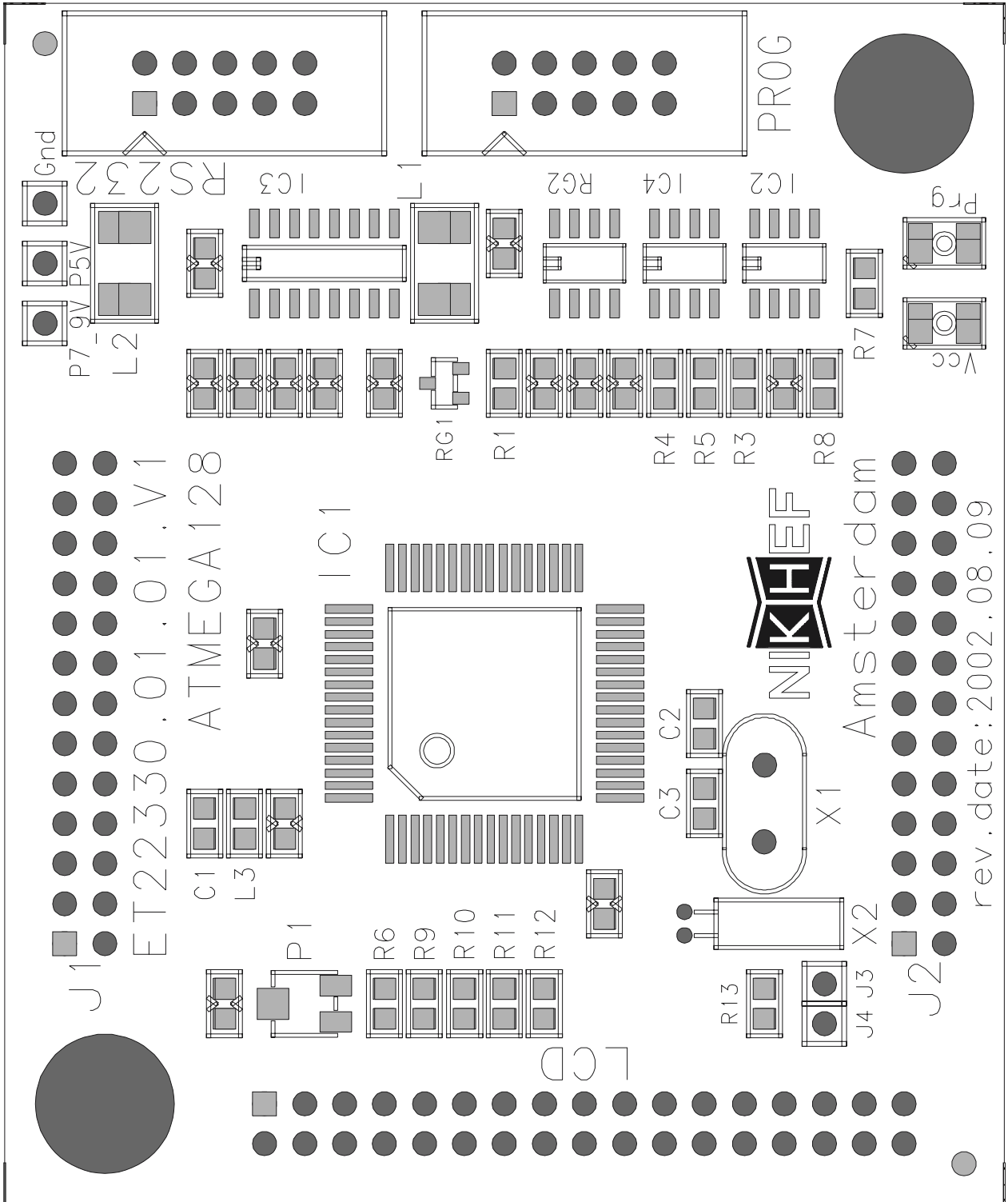


Figure 3: PCB layout

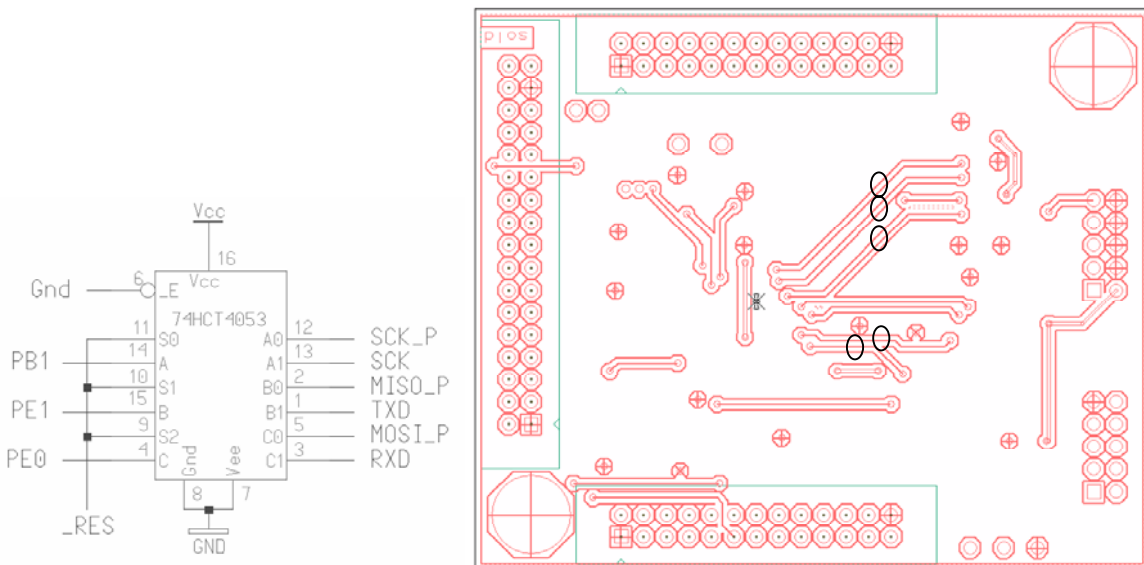
Modifications

The coil L1 is too big, compared to the capacitance behind it. The varying processor current introduces large power supply variations. L1 is now short circuited.

Load capacitors (C2, C3) of the main oscillator probably too big. This results in very small signal amplitude. Changed the capacitors from 33 pF to 18 pF.

The ALE output was connected to ground. Now connected to J3, which in turn connects to J2 pin 2.

The programming data signals of the ATMega128 are connected to PE0 and PE1 (RXD and TXD) instead of the old fashioned MOSI and MISO pins. An 74HCT4053 is added to split the ports to the RS232 connector and the programming connector. It is switched by the _RES signal.



Cut five lines on the bottom of the board and connect the 4053 according to the list.

IC-pin	4053
1-2	4
1-3	15
1-11	14
2-1	9,10,11
3-11	1
3-12	3
4-2	2
4-5	5
4-6	12
J2-4	13
GND	6,7,8
Vcc	16

Great care must be taken when programming the *lock* and *fuse* bits. There is a separate note on this issue: http://www.nikhef.nl/pub/departments/et/misc/atmega128/fuse_lock.pdf

Pin list

JP1			JP2			LCD
Pin	Function	Alt. function	Function	Alt. function	PCB	
1	GND		GND			GND
2	VCC		TESTPIN	ALE ¹		NC
3	PE7	IC3/INT7	PB3	MISO		VCC
4	PE6	T3/INT6	PB1	SCK		NC
5	PE5	OC3C/INT5	PB2	MOSI		POTMETER
6	PE4	OC3B/INT4	PB0	_SS		NC
7	PE3	OC3A/AIN1	PD1	SDA/INT1		RS/PF2
8	PE2	XCKO/AIN0	PD0	SCL/INT0		NC
9	PF0	ADC0	PD3	TXD1/INT3	CTS/TXD1	R_W/PF1
10	PF1	ADC1	PD2	RXD1/INT2	RTS/RXD1	NC
11	PF2	ADC2	PD5	XCK1		ELC
12	PF3	ADC3	PD4	IC1		NC
13	PF4	ADC4/TCK	PD7	T2		R9
14	PF5	ADC5/TMS	PD6	T1		NC
15	PF6	ADC6/TDO	PG1	_RD		R10
16	PF7	ADC7/TDI	PG0	_WR		NC
17	PA0	AD0	PC1	A9		R11
18	PA1	AD1	PC0	A8		NC
19	PA2	AD2	PC3	A11		R12
20	PA3	AD3	PC2	A10		NC
21	PA4	AD4	PC5	A13		D4/PB4
22	PA5	AD5	PC4	A12		NC
23	PA6	AD6	PC7	A15	_CSEE	D5/PB5
24	PA7	AD7	PC6	A14		NC
25	P7_9V		_RES			D6/PB6
26	GND		GND			NC
27	-		-			D7/PB7
28	-		-			NC
29	-		-			R13
30	-		-			NC
31	-		-			GND
32	-		-			NC

RS232	
1	Loop
2	Loop
3	TXD
4	RTS/TXD2
5	RXD
6	CTS/RXD2
7	Loop
8	NC
9	GND
10	NC

Prog	
1	MOSI
2	Vcc
3	P_LED
4	GND
5	_RES
6	GND
7	SCK
8	GND
9	MISO
10	GND

¹ See chapter modifications on page 7

Connector remarks

For the alternate function description see the Atmel documentation (link on page 3).

The signals listed under *PCB* are routed on the board, so some care should be taken on how to use them. E.G. PD2, PD3 can be used to implement hardware handshaking. If they are used to create a second (hardware) serial port the signals from the 2 * 5 pin connector must be externally split to two serial cables.

The LCD connector is mounted on top of the board normally. The odd pin numbers are used to carry the LCD signals. It can be connected to an LCD display via a flat-cable. On the LCD display both rows may be short circuited since the even row is not used, see connector diagram. A single row connector can be used at the LCD end of the cable, which is less bulky.

The port pins not found on JP1 and LP2 are found on this connector. When these are used on the main board via a connector on the bottom of processor board, one should take care of the swapping of odd en even rows.

The R_W signal to the LCD should be driven from the processor. Many applications never read the display. It should be set to *write* in that case (PF1 = '0'). When starting using the display set the potentiometer value to app. 2...3 k Ω (to ground) and adjust the contrast when text is displayed.

The _RES signal may pulled low from the main board (10 k Ω pull-up).