

Report on feasibility study of a front-end chip design in 0.25 μ CMOS technology for the LHCb Outer Tracker.

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Abstract.

We have conducted a feasibility study of a Preamplifier-Shaper-Baseline Restorer design in 0.25 μ CMOS technology for the LHCb Outer Tracker.

The basis of the design specification is described along with circuit optimization procedures that have been carried out to meet the specification. Simulation results of the Preamplifier-Shaper-Baseline Restorer circuit are presented and discussed.

Introduction.

The LHCb Outer Tracker detector at CERN will employ a straw proportional wire chamber. A basic cell of the detector consists of a straw tube and an anode wire located in the center of a conductive tube [1].

The small diameter straw tubes offer excellent potential for efficient and high precision particle track reconstruction when provided with appropriate signal processing electronics [1].

Intrinsic noise of the electronics ought to be diminished to provide low threshold and therefore efficient operation at minimum values of gas gain.

Pulse response rise time has to be chosen thus to avoid track position resolution degradation due to effect of time jitter.

The requirement of high rate operation stipulates for careful ion tail cancellation by means of dedicated signal processing techniques.

Input impedance of the electronics is to match characteristic impedance of the straw tube to save from after pulsing and avoid ghost hits presence in read-out system [2].

The electronics must be a set of electrically separated channels to guarantee low cross-talk between different cells of the detector.

Power dissipation is an issue because of the enclosed space for the electronics and large number of channels.

The electronics is being foreseen to operate in mixed analog-digital environment. For this reason particular attention must be paid to making a solid connection between detector signal ground plane and analog ground of the electronics.

The electronics is expected to run under severe radiation conditions and therefore to be designed in a radiation tolerant technology.

Among technologies available nowadays .25 μ CMOS seems to satisfy the requirements listed. It is an up-to-date radiation hard technology, giving a wide variety of components.

The tiny CMOS transistors (minimum channel length 250nm) with thin oxide layers (few nanometers) are able to stand voltages at the most 2.5V. This limit constrains maximum supply voltage rail applicable in the technology and hence restricts number of schematic solutions.

The availability of a well developed set of models and tools, has made it possible to accurately predict the performance of the circuit.

Owing to the broad spread of the .25 μ CMOS technology in the LHCb community it seems to be realistic to share the chips mass production with another project. Thus considerably reducing cost of the front-end electronics.

A preliminary study on the possible schematic solutions is being undertaken. The goal of the study is to check the feasibility of designing a Preamplifier-Shaper-Baseline_Restorer-Discriminator integrated circuit for the LHCb Outer tracking detector in 0.25 μ CMOS technology.

Inputs for the design.

Straw module layout, geometry of the straw tube as well as parameters of its operation have been developed on the basis of the physical task the LHCb Outer Tracker is going to perform [1]. The parameters important for the electronics design are listed below.

.gas mixture Ar(75)CF₄(15)CO₂(10)

.high voltage $V_{HV}=1600$ V

.total gas gain $G_T=20000$

.signal size distribution is Landau with most probable value of 25fC (effective charge) [2].

.drift velocity in magnetic field $V_{dr} \approx 78 \mu\text{/ns}$

.drift velocity outside magnetic field $V_{dr} \approx 100 \mu\text{/ns}$

.straw tube diameter $D=5$ mm

.straw tube conductivity $R_s < 1 \Omega\text{/m}$

.anode wire diameter $d=25 \mu$

.anode wire conductivity $r_s=110 \Omega\text{/m}$

.length of the straws $L \approx 2.4$ m

Specification of the electronics.

1. Ion tail cancellation.

For cylindrical proportional chambers the output current is usually expressed as

$$I(t) = I_0/(1+t/t_0),$$

with $t_0 = d^2 \ln(D/d)/2V\mu$, where μ is the ion mobility, V is the voltage on the straw.

For the chosen gas mixture $\mu \approx 1.7 \text{ cm}^2\text{s}^{-1}\text{V}^{-1}$.

It yields $t_0 \approx 6\text{ns}$.

To be able to calculate pole/zero compensation circuit the current function $I(t)$ has to be fitted by a sum of exponent functions as follows

$$I_f(t) = -Q_e \delta(t) - Q_i [A_1 \exp(-t/\tau_1) + A_2 \exp(-t/\tau_2)],$$

where the first item represents electron component with a charge Q_e , the second is an ion component with a charge Q_i . These components are in ratio $Q_e/Q_i \approx 0.03$ [3]. Function $\delta(t)$ is Dirac δ -function.

By using fitting procedures parameters A_1, τ_1, A_2, τ_2 have been determined and the fitting function specified as

$$I_f(t) = 1.49\delta(t) + [\exp(-t/13.2\text{ns}) + 0.2\exp(-t/163\text{ns})],$$

Both the output current $I(t)$ and fit of the current $I_f(t)$ are given in Fig.1

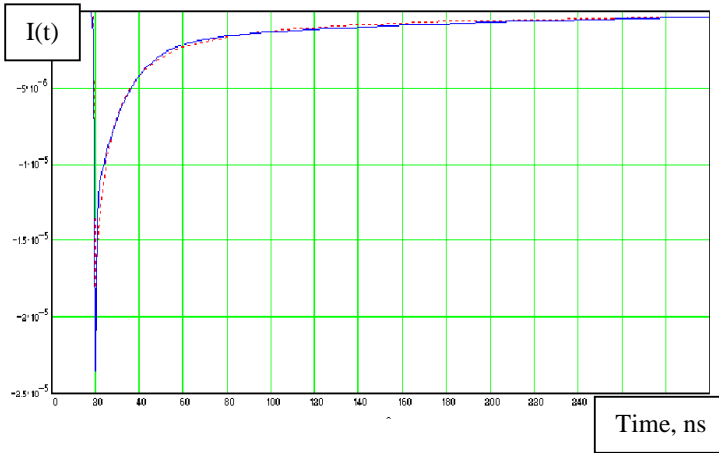


Fig.1 The straw output current $I(t)$ (dashed curve) and fit of the current $I_f(t)$ (solid curve).

Function $I_f(p)$ represents Laplace of the fitting function $I_f(t)$ as follows:

$$I_f(p) = L\{I_f(t)\} = -1.49 - 13.2/(p13.2\text{ns}+1) - 32.95/(p163\text{ns}+1)$$

Next step is to define transfer function of the circuit which completely compensates the straw output current.

$$F_c(p) = I_f(p)^{-1} = - [(p13.2\text{ns}+1)(p163\text{ns}+1)] / [(p1.15\text{ns}+1)(p58.82\text{ns}+1)]$$

2. Analogue signal output parameters.

If the electronics realizes $F_c(p)$ then the output signal becomes δ -function as long as its Laplace image equals to unity according to expression:

$$U_{\text{out}}(p) = I_f(p) F_c(p) = 1.$$

To reduce the output noise the electronics frequency bandwidth must be restricted. On the other hand the restriction causes slowing of the electronics and hence changing of the analogue signal output parameters.

Detail studies of the dependencies have been carried out by ATLAS TRT Detector group [4].

It has been shown that shortening of the peaking time improves drift-time measurement accuracy, however the efficiency decreases rapidly for peaking times below 7.5ns. Therefore value of 7.5ns was found as an optimum.

An additional circuit is necessary to give a desired shape to the output signal. It is common to utilize $(RC)^n$ integration stages to provide semi-gaussian of the shaped signal. Laplace transform of the circuit is given as

$$F_s(p) = (p\tau + 1)^{-5}.$$

Whereas the output signal in time is

$$U_{\text{out}}(t) = (t/\tau)^4 \exp(-t/\tau).$$

The parameters of interest are peaking time ($4\tau = 8\text{ns}$) and full shaping time ($\approx 13\tau = 26\text{ns}$). Being coupled by scaling factor (τ), both of them have a major impact on basic detector properties such as track position resolution and efficiency.

Now we can define the overall transfer function of the electronics as

$$F(p) = F_c(p) F_s(p) = - [(p13.2\text{ns}+1)(p163\text{ns}+1)] / [(p1.15\text{ns}+1)(p58.82\text{ns}+1)(p2\text{ns}+1)^5]$$

Only 12% of the total charge coming out of the straw will be utilized since the straw output current collection time is much longer (hundreds of nanosecond) than the full shaping time (26ns). So, effective or visible gas gain is given as:

$$G_v = 0.12 * G_t = 2400$$

3. Double pulse resolution.

Since the LHCb Outer Tracker will operate at 2MHz counting rate, some tracks will be lost if they occur within the detector dead time. It is determined on one hand by cluster-drift time in the straw tube and on the other hand by the full shaping time of the electronics. Minimization of the electronics contribution to the detector dead time is needed. For the optimum value of $\tau = 2\text{ns}$ the full shaping time is $13\tau = 26\text{ns}$, whereas the total drift time is $D/2V_{\text{dr}} = 32\text{ns}$. Apparently the electronics is not the main contributor to the overall detector dead time.

4. Intrinsic noise.

With the purpose to get the best track position resolution the electronics should be ready to trigger on the first cluster arriving at the anode wire. It means that the threshold referred to the input charge ought to be set at the level of

$$\text{THR} = 1e * 2.5 * G_v = 6000e,$$

where G_v is visible gas gain, 2.5 is secondary ionization factor.

Intrinsic noise determines the lowest threshold value. To keep noise trigger rate at appropriate level the threshold cannot be lower than

$$\text{THR} = 5 \text{ ENC},$$

where ENC- equivalent noise charge or root mean square (RMS) parameter for input referred noise distribution.

In that way the lowest noise level needed for the best detector performance is being estimated as

$$\text{ENC} = 6000e/5 \approx 1200e.$$

However a long resistive anode wire (224 Ohm for 2m straw) in itself gives 1300e of noise even when the electronics is noiseless. Therefore the electronics noise level has to be at the most **1300e**. Then the total noise will be 1800e, that is quite sufficient for the successful operation of the detector.

5. Input impedance.

The straw characteristic impedance as a function of frequency is known from theory of transmission lines as follows:

$$W(\omega)=[(j\omega L_{st}+R_a)/(j\omega C_{st})]^{0.5}.$$

Where transmission line parameters per unit length derived from the straw tube structure are:

$$L_{st}=1.1\mu Hn/m, C_{st}=10.5pF/m, R_a=1120\Omega/m.$$

With the purpose to avoid reflections in long (up to 2m) straw tube, input impedance of the electronics must approach the straw characteristic impedance as good as possible in the frequency band of interest (2MHz...100MHz) [2]. Because of the square root behavior there is no circuit with input impedance that matches to the function $W(\omega)$ for all frequencies.

The characteristic impedance goes to the value of 300Ohm at high frequencies, so resistive part of the electronic input impedance must go to the value as well. A serial capacitor in front of it delivers the low frequency rise (see Fig.2). Value of the capacitor in range 50pf...200pf could be chosen depending on criteria of fit.

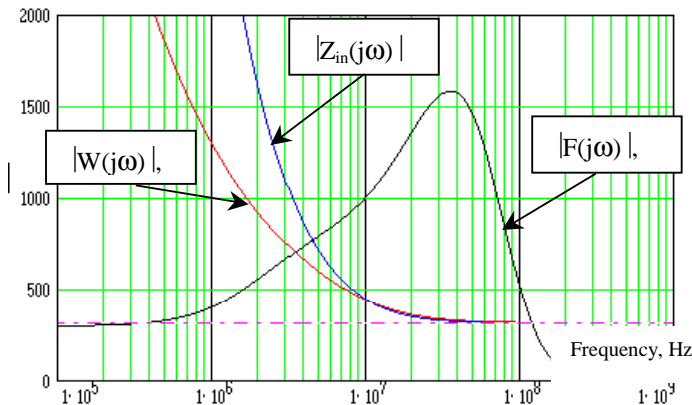


Fig.2. Characteristic impedance of the straw tube transmission line $|W(j\omega)|$, input impedance of the circuit $|Z_{in}(j\omega)|$ consisting of 50pf capacitor in series with a 300 Ohm resistor, the electronics frequency bandwidth $|F(j\omega)|$.

Besides the matching function the serial capacitor provides high voltage separation between straw anode wire and the electronics. From point of view of spark breakdown safety it is highly preferable to keep value of the capacitor as low as possible.

The electronics input impedance appears as a equivalent resistance of **300 Ohm**.

6. Base line restorer.

The 0.25μ CMOS technology we have been chosen to use for the design of the electronics can not guarantee tolerances of absolute values of resistors and capacitors better than 30%. That means the tail cancellation circuit cannot be tuned precisely and residuals always exists. For the purpose of an additional suppression of the residuals and better base line recovering a base line restoration circuit is needed. Actually it does nonlinear differentiation of the signal almost breaking dc-path and essentially suppressing the slow residuals.

Moreover it helps to keep the discriminator threshold level independent from dc-offsets and temperature drifts occurring in input part of the electronics.

By the principle of operation the base line restorer (BLR) causes a small overshoot in the signal. The overshoot might result in loss of some pulses [5]. On the other hand it helps to save from ghost hits coming from imperfect matching between the straw and the electronics [2].

On the ground of all the arguments listed above it looks necessary to design a **BLR** as a separate part of the electronics.

7. Power consumption.

As it was mentioned above the electronics will operate in enclosed box therefore low power design is highly preferred. In addition heavy current consumption will cause extra troubles for power distribution due to voltage drop on the wire. We estimate that consumption less than **30mW/channel** would be quite affordable.

Circuit design.

1. Preamplifier.

Transimpedance or current-to-voltage transactor is for the most part used to realize function of preamplification (see Fig3).

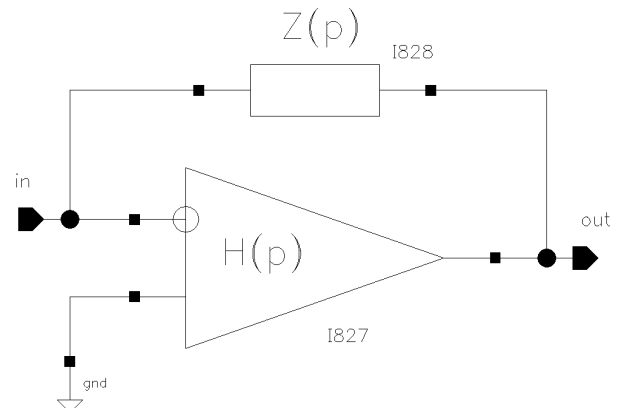


Fig.3. Basic structure of the preamplifier.

Input impedance of the preamplifier is known as

$$Z_{in}(p) = Z(p) / (1 + H(p)),$$

Where $Z(p)$ is Laplace image of the feedback circuit impedance, $H(p)$ is open loop transfer function.

For the one stage amplifier transfer function is

$$H(p) = A_0 / (1 + p\tau_0),$$

where A_0 is dc-gain, τ_0 is frequency roll-off constant.

Feedback circuit is formed by a resistor (R_1) and a bypass capacitor (C_1) therefore

$$Z(p) = R_1 / (1 + pR_1C_1)$$

Summarizing the expressions input impedance can be represented as:

$$Z_{in}(p) = [R_1 / A_0] [(1 + p\tau_0) / (1 + pR_1C_1)],$$

where the first term is a dc input impedance, which must be equal to 300 Ohm. The second determines high frequency behavior (see Fig.4). For very high frequencies input impedance goes down anyway because of the second order parasitic capacitors at the input.

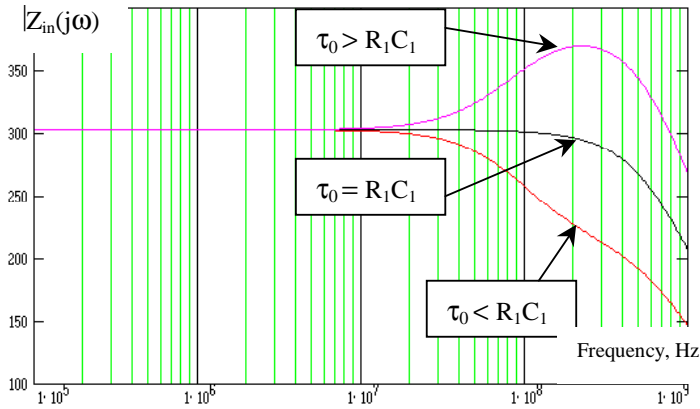


Fig.4. Frequency behavior of the input impedance.

The input impedance demonstrates uniform behavior in wide frequency band if $\tau_0 = R_1C_1$.

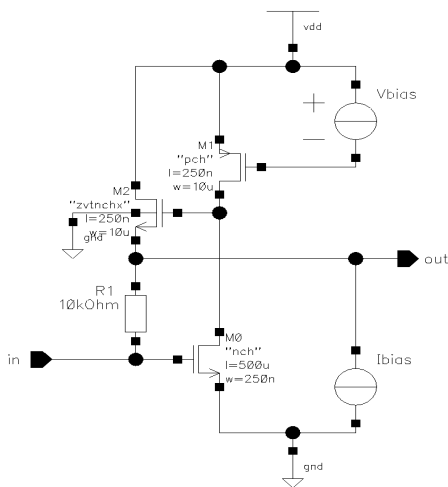


Fig.5. Schematics of the preamplifier.

Schematics of the preamplifier is given in Fig.5 Transistor M0 converts input voltage into drain current by transconductance factor g_m^{M0} . Active load is realized by M1 having $g_m^{M1} \ll g_m^{M0}$, transistor M2 is a voltage follower.

From common mode noise rejection point of view, a dummy part is necessary to be in the preamplifier design. At the same time it brings extra noise, increasing the overall preamplifier noise by factor of $\sqrt{2}$.

Taking into account the noise of the dummy part, and the electronics bandwidth, the total noise of the electronics connected to 2m long straw is

$$ENC = 145e \sqrt{2} [310^2 / R_1 + 1 / (2 g_m^{M0})]^{0.5}$$

To meet the requirement for intrinsic noise we come to values

$$R_1 = 10k\Omega, \quad g_m^{M0} = 20mS.$$

To be able to reach specified g_m for the minimum drain current (I_d), M0 ought to operate in weak inversion or sub-threshold mode. That means V_{gs}^{M0} has to be shifted below the threshold along with scaling the transistor up in such a way that W/L ratio increases.

For a CMOS transistor, there is limit of g_m / I_d at the level of about 25mS/1ma. The higher W/L ratio is the closer we are approaching the limit but on the other hand the bigger the parasitic capacitors are. The parasitics will deteriorate high frequency performance of the preamplifier. For this reason a equivalent small-signal circuit needs to be looked at (see Fig.6)

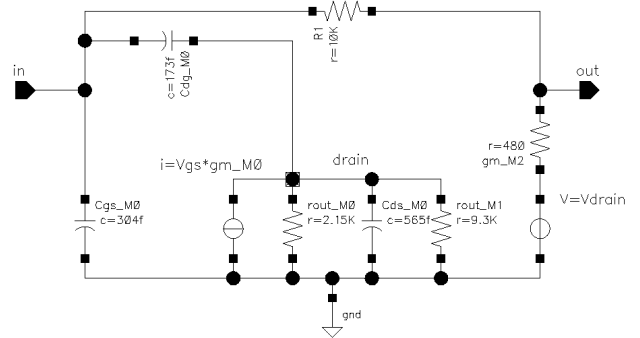


Fig.6 Equivalent small-signal circuit of the preamplifier for $I_d = 1.3ma$

The input impedance in this configuration can be determined through the terms discussed above as follows

$$A = g_m^{M0} (r_{out_M0} \parallel r_{out_M1}) = 37$$

$$Z_{in}(\omega=0) \approx 300 \text{ Ohm.}$$

$$\tau_0 = (r_{out_M0} \parallel r_{out_M1}) (C_{ds_M0} + C_{dg_M0}) = 1.2ns$$

$$\tau_1 = R_1 C_{dg_M0} = 1.7ns$$

To meet condition $\tau_0 = \tau_1$ a capacitor should to be added to the drain node. Thus uniform behavior of the

input impedance can be achieved in range up to 200Mhz (see Fig7).

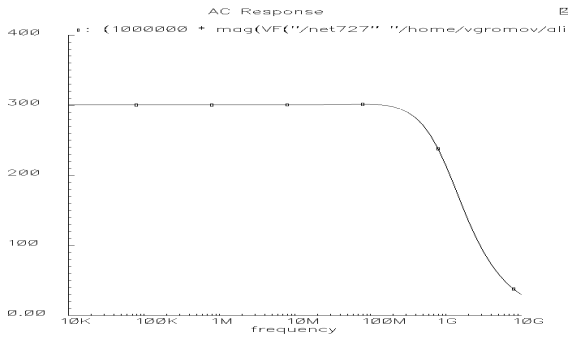


Fig.7. The preamplifier input impedance. HSPICE simulations.

The signal transfer function of the preamplifier is being represented by a first order integration set by the feedback circuit

$$F_{pr}(p) = R1 / (1 + pR1 Cds_M0) = 10k / (1 + p2ns).$$

Signals at the input and at the output of the preamplifier are plotted in Fig.8.

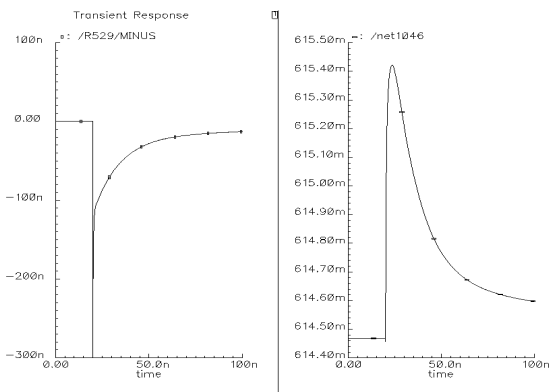


Fig8. Signals at the input (left) and at the output (right) of the preamplifier. HSPICE simulations.

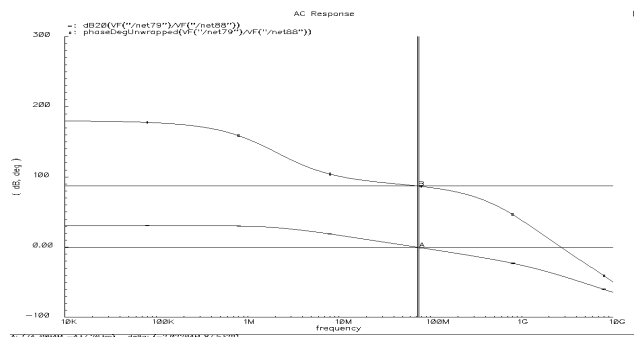


Fig9. HSPICE simulations of the preamplifier open loop gain. Magnitude (lower curve) and phase (upper curve). Phase margin is 87.5°.

A one stage configuration constitutes the best stability performance. As it is shown in Fig.9 the phase margin for the preamplifier feedback solution is almost ideal (87.5°).

The preamplifier consumes 3.5ma from 2.5V supply source.

2. Shaper.

The goals for the shaper are to remove long tail from the signal, shape and amplify the signal, reject common mode disturbances. Transfer function the shaper ought to realize is

$$F_{sh}(p) = F(p) [F_{pr}(p)]^{-1} = - \frac{0.27(p13.2ns+1)(1.15ns+1)(p2ns+1)}{[(p13.2ns+1)(p163ns+1)] / [(p1.15ns+1)(p58.82ns+1)(p2ns+1)^4]}$$

Block diagram of the shaper if given in Fig.10.

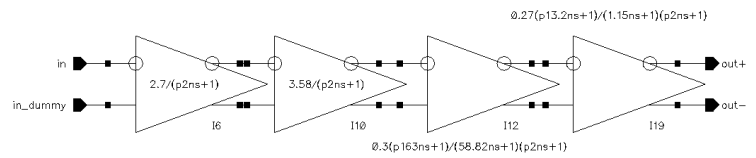


Fig.10. The shaper block diagram.

The shaper consists of four fully differential stages. Each of them realizes part of the overall transfer function. The first and the second stages perform amplification and integration by means of poles. The third and fourth ones contain zeros along with poles.

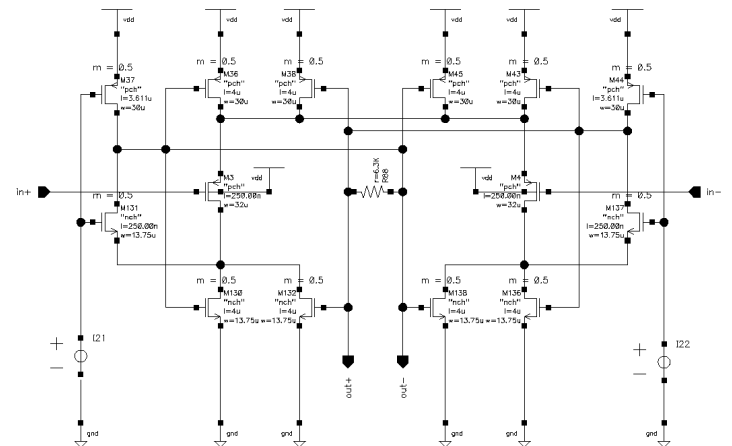


Fig.11. Schematics of the first stage. $F_{sh}^{-1}(p) = (p2n+1)^{-1}$.

The first stage (see Fig.11) shifts the operational point from 0.614V up to 1.25V. The output level is firmly fixed by common mode feedback at the middle of the supply voltage rails. Thanks to large output capacitance ($\approx 700fF$) formed by C_{gs} of transistors M130, M132, M36, M38, M138, M136, M45, M43 dominant

pole of the common mode feedback is shifted far away in low frequency domain. That gives perfect stability (phase margin is 88.7°), whereas dc-gain is 49Db (see Fig.12).

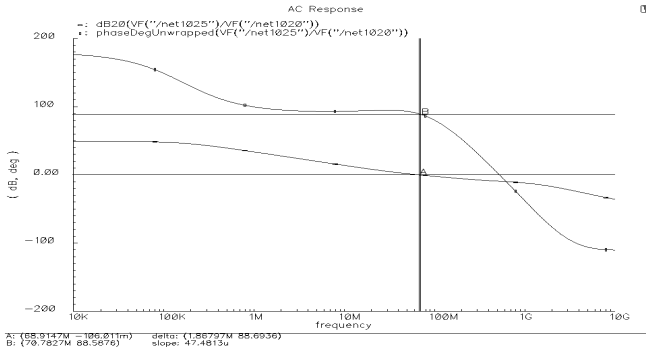


Fig.12. First stage of the shaper. Open loop gain. Magnitude and phase as functions of frequency.

The common mode suppression factor equal to U_{cm}^{out}/U_{cm}^{in} is -59Db at low frequency and goes up to -27Db at the worst case (at frequency of 316MHz) (see Fig.13).

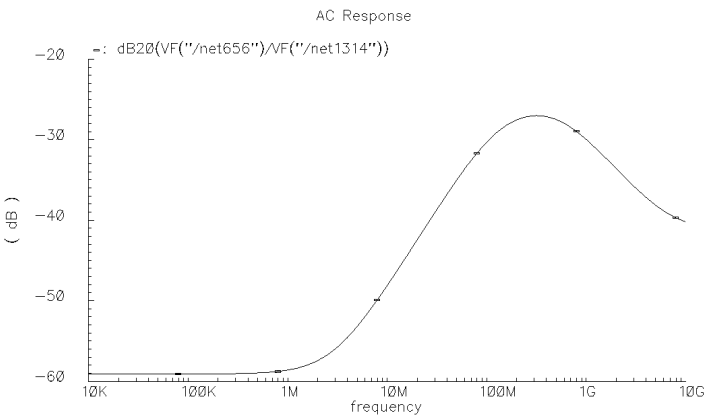


Fig.13. First stage of the shaper. Magnitude of the common mode suppression factor as a function of frequency.

Differential dc-gain of the stage is determined by the ratio

$$R88 g_m^{M3} 0.5 = 2.7.$$

Signal transfer function is set by integration at the output of the stage as follows:

$$F_{sh}^1 = (p0.5 R88 C_{out} + 1)^{-1} = (p2ns + 1)^{-1}.$$

The first stage consumes 0.232ma from 2.5V power supply source.

The second stage of the shaper is almost identical to the first one. Although it has 1.25V operational level at

input as well as at the output, provides higher dc-gain (3.58) and consumes 0.289ma from 2.5V supply source.

The fourth stage (see Fig.14) is designed to realize transfer function

$$F_{sh}^4(p) = 0.27(p13.2ns + 1) / [(p1.15ns + 1)(p2ns + 1)]$$

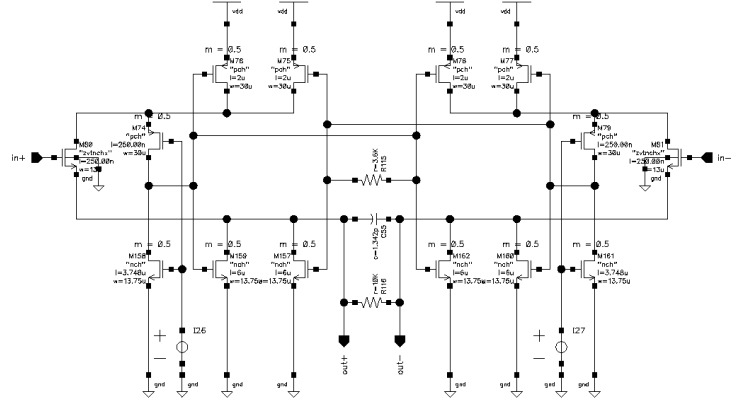


Fig.14. Schematic of the fourth stage.

The signal differentiation is done by resistor R116 in parallel capacitor C55. These elements form zero with time constant $R116 C55 = 13.2ns$.

$$(p R116 C55 + 1) = (p13.2ns + 1).$$

The same capacitor C55 in serial with transconductances of transistors M80, M81 constitute a pole with time constant $2C55/g_m^{M80} = 2ns$.

$$(2 p C55/g_m^{M80} + 1)^{-1} = (p 2ns + 1)^{-1}.$$

A pole at the output is given by impedance R115 in parallel with impedance of the stage output capacitance as follows:

$$(p 0.5 R115 C_{out} + 1)^{-1} = (p 1.15ns + 1)^{-1}.$$

DC-gain of the stage determined by ratio

$$R115 / (R116 + 1/g_m^{M80} + 1/g_m^{M81}) \approx 0.27.$$

The fourth stage consumes 0.289ma from 2.5V power supply source.

Stage number three must realize transfer function

$$F_{sh}^3(p) = 0.3(p163ns + 1) / [(p58.82ns + 1)(p2ns + 1)].$$

It seems to be not so easy because we get into troubles trying to create capacitors larger than 1pF and resistors bigger than 10kOhm in the 0.25u CMOS technology. That is why we have to use output impedance of transistors to get a high ohmic impedance. Being coupled to a capacitor of order of 1pf it gives possibility to provide signal differentiation with a time constant of 163ns and integration with a time constant of 58.82ns on the chip.

However the output impedance of a transistor is not stable due to dependency on bias condition and the signal size. This instability leads to imperfect compensation of the ion tale and hence a residual appears. The only thing we can do is to optimize the circuit on minimization of the sensitivity of the transistor output impedance to the biasing conditions and signal size variations.

Schematics of stage number three is given in Fig.15. Output impedance of transistors M125-M128 in parallel with impedance of capacitor C13 is used to form zero.

$$(p C_{13} / g_{ds}^{M125} + 1) = (p 163ns + 1).$$

To minimize variations of the value of g_{ds}^{M125} V_{ds}^{M125} must be kept higher than 1V. To meet this condition we use zero-voltage transistors M34, M35 at the input of the stage. Since V_{gs} of the transistors is just 213mV and their inputs are at 1.25V, drains of transistors M125-M128 are biased at 1V in respect to their sources. This solution allows to diminish g_{ds}^{M125} variation due to input bias level shift to 2%/10mV, variation caused by supply voltage instability are of order of 0.2%/10mV, temperature variation are 1%/10°C.

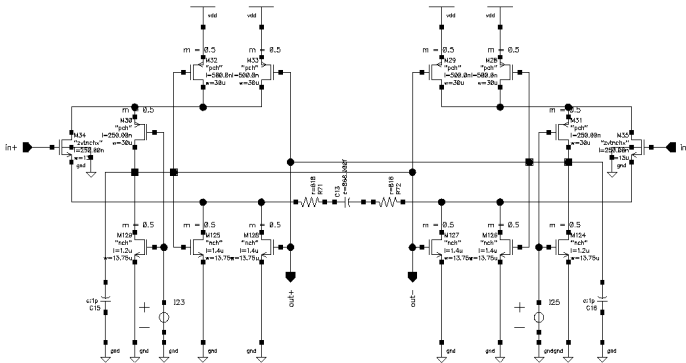


Fig.15. Schematics of the third stage of the shaper.

In this stage the high frequency pole is determined by C13, R71, R72 and g_m^{M34} , g_m^{M35} as given

$$(2 p C_{13} / [R_{71} g_m^{M34}] + 1)^{-1} = (p 2ns + 1)^{-1}.$$

The other pole is formed at the output of the stage by the stage output impedance itself and capacitors C15, C16.

$$(0.5p R_{out} [C_{out} + C_{15}])^{-1} = (p 58.85ns + 1)^{-1}.$$

The current consumption of the third stage is 1.1mA from 2.5V supply source. Total shaper current consumption yields to 1.91mA.

Signals at the input and at the output of the shaper are plotted in Fig. 16. Specification requirements on ion tail cancellation as well as on analogue signal output

parameters have been fulfilled (peaking time is $\approx 7.5ns$, full shaping time is $\approx 26ns$).

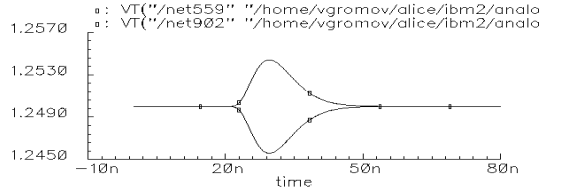
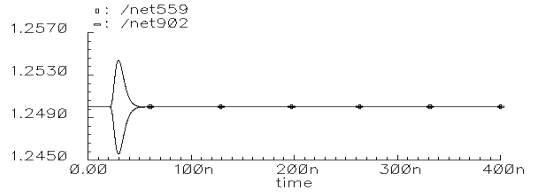
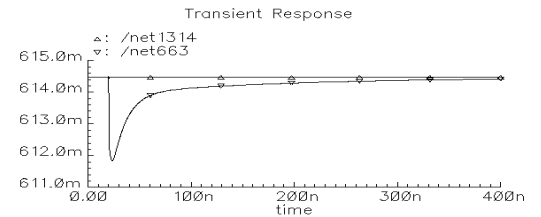


Fig.16 Signals at the input (on the top) and at the output (in the middle and at the bottom) of the shaper for a 2fC straw detector hit.

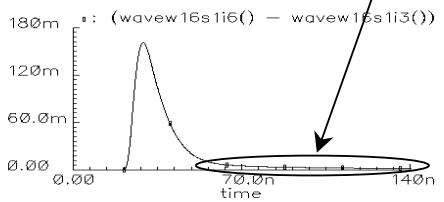
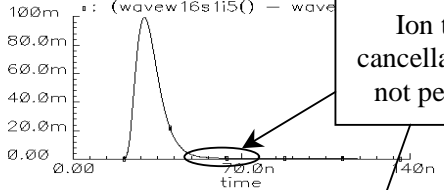
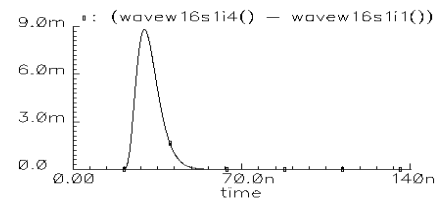


Fig.17. The shaper output signals for a 2fC (top), 25fC (middle), 60fC (bottom) hits.

Imperfect ion tail cancellation caused by nonlinear behavior of the compensation component (transistors output impedance, discussed before) is demonstrated in Fig.17. For small signals (2fC) the compensation is perfect, while for bigger signal it is not as good. As result residuals of the long ion tail are still there for signal bigger than 25fC. An additional residual suppression circuit is needed to cope with this.

3. Base line restorer.

As we pointed out a circuit is needed to remove the ion tail residuals occurring due to imperfect compensation in the shaper. To be able to remove the residual with minimum signal distortion, and to give an output signal to be used for discrimination, differences between the signal and the residuals need to be highlighted. First, the residuals are slower (are of order of hundred nanosecond) than the real signal (full shaping time is $\approx 26\text{ns}$) (see Fig. 16). This probably means a high frequency filter or differentiation circuit must be somehow used. When the time constant of the differentiation circuit is big (hundreds of nanosecond) it does not distort shape of the signal but is not very effective as the residual remover. If the time constant is small (tens of nanoseconds) it removes the residuals quite efficient at the same time distorting the shape of the signal. The residuals are much smaller in magnitude than the signal (see Fig.17). Hence we can think of nonlinear circuit which provides fast differentiation for small signals (effective zone) and slow differentiation for bigger signal (ineffective zone) (see Fig.18).

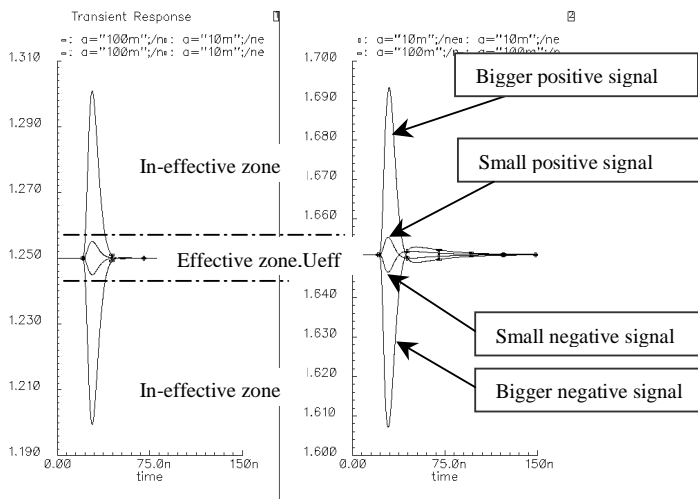


Fig.18. Principle of base line restorer operation. Complementary small signals (completely sitting in the effective zone) together with bigger ones (most part of which is sitting outside the effective zone) at the input (left) as well as at the output (right).

Signals of both sizes at the output of base line restorer (BLR) are given in Fig.19. The positive lobe of

a small signal is followed by a large overshoot while for the big signal the overshoot is considerably smaller. In the case of the small signal, the area of the positive lobe is almost equal to the area of the overshoot. This is caused by the fact that the small signal is completely sitting in effective zone and has been processed in the way of classical RC-differentiation circuit. The circuit does not pass dc and therefore the area of output signal is zero. That in turn means that area of positive lobe is equal to the area of overshoot.

For the big signal this is not valid because most of it is outside the effective zone where differentiation is not effective. Overshoot of the big signal is determined by its part still sitting within effective zone. Area of its overshoot equals to the area of its in-effective zone part (see Fig.19). The bigger the signal is, a relatively lower part of it is within effective zone and the relatively smaller the overshoot at the output of BLR becomes.

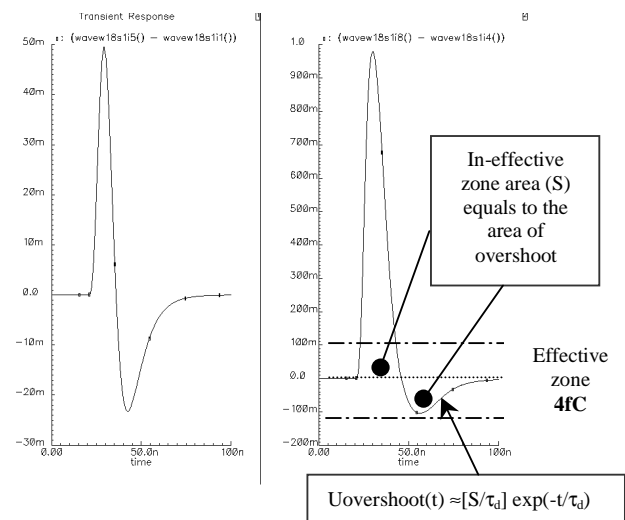


Fig.19. Small (2fC hit) output signal of BLR (left) and big (50fC hit) output signal of BLR (right).

We have chosen an active base line restorer to implement the principle of nonlinear differentiation (see Fig.20).

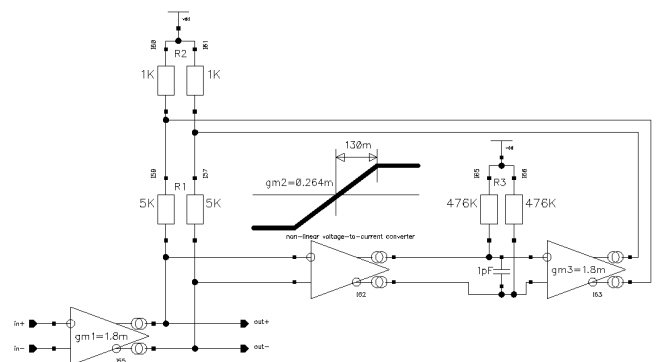


Fig.20. Block diagram of the active base line restorer.

Nonlinear low frequency pass feedback is the key feature of the design. Linear range of the feedback chain (130mV) determines the width of the effective zone. A small signal (less than 130mV) will be differentiated coming through the base line restorer. Small signal transfer function is

$$F_{blr}(p) \approx (R1+R2) gm1 [1/Ao+p\tau_d]/[1+p\tau_d], \text{ where}$$

$$\begin{aligned} \text{dc-gain } Ao &= 1+[gm2 R3 gm3 R2] = 250, \\ \text{differentiation time constant is} \\ \tau_d &= C/[gm2 gm3 R2+1/R3] = 5.8\text{ns} \end{aligned}$$

High frequency part of the input signal is almost not distorted whereas low frequency part of the signal is being suppressed by factor of 1/Ao(see Fig.21).

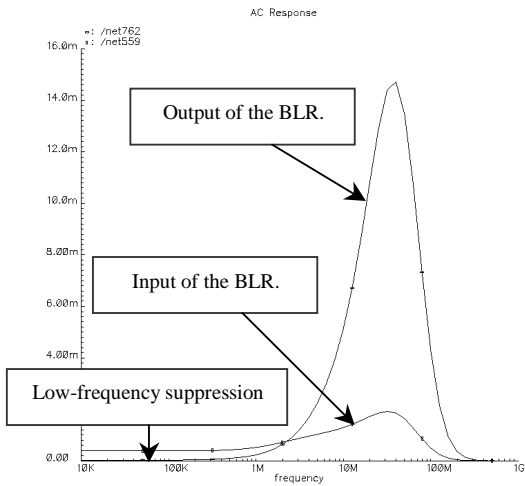


Fig.21. Small signal frequency response of the base line restorer.

If an input signal goes outside the linear range, output current of the nonlinear voltage to current converter saturates at the level of 10ua. That means gm2 decreases to a low value as well as time constant of differentiation τ_d . The BLR goes to non-linear mode of operation where the signal is being almost not distorted. However the saturation current is charging capacitor while the signal is staying outside the linear range. The stored charge causes overshoot when the signal returns into linear range (see Fig.19). Shape of the overshoot is given as

$$U_{overshoot}(t) \approx [S/\tau_d] \exp(-t/\tau_d), \text{ where}$$

τ_d is differentiation time constant,
S is in-effective zone area (see Fig.19).

Width of the linear range must be adjusted to the expected base line fluctuation range. It should not be too narrow since the BLR will not remove base line

fluctuation coming out of the range. At the same time it does not make sense to enlarge it groundless as long as the overshoot of the signal becomes bigger (see Fig.19). For the present BLR linear range referred to the input is set at the level of 4fC.

Schematics of the active BLR is given in Fig. 22. A differential stage is surrounded with serial feedback consisting of nonlinear integrator and an output differential pair.

Linear range of differential stage consisting of transistors M235, M239 determines range of linear operation (130 mV).

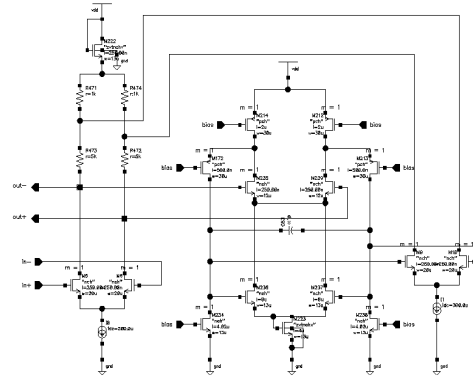


Fig.22. Schematics of the active base line restorer.

Fig.23 shows how effective the base line restorer is for slow signal suppression.

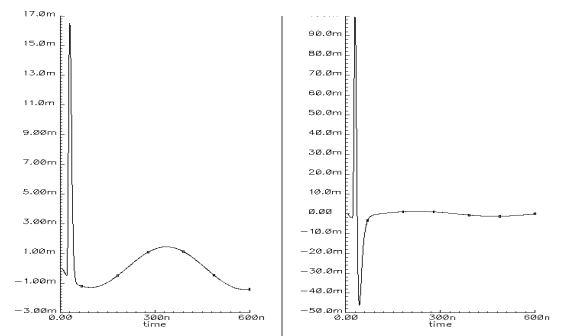


Fig.23. Signals together with slow disturbances at the input (on the left) and at the output (on the right) of the base line restorer.

The current consumption of the base line restorer is 0.84ma from 2.5V supply source.

Conclusion.

A preliminary study of schematics of Preamplifier-Shaper-Baseline_Restorer circuit targeted on LHCb Outer tracking detector has been carried out. The study indicates that 0.25 μ CMOS technology is pretty suitable for designing of the circuit. Schematics presented above gives the following performance.

- a) intrinsic noise 2000e RMS
- b) input impedance 300 Ω (within 200MHz range)
- c) analogue signal output parameters : peaking time 7.5ns, full shaping time 25ns.
- d) provides ion tale cancellation.
- e) overall small signal gain of the circuit 32mV/fC (effective charge).
- f) contains active base line restorer (effective zone width referred to the input=4fC, in-effective zone differentiation time constant $\tau_d=5.8$ ns, open loop gain=250).
- g) consumes 6.25ma from 2.5V supply source. Total power consumption 15.6mW.

Discriminator and LVDS output stage are commonly used circuits and can be added without too much research.

Radiation hard layout techniques are known and can be applied to the proposed circuit.

We would probably have several experimental submits (a half year between them) to reach a final submit.

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