

# Characterization of DTMOST Structures to be used in Bandgap Reference Circuits in 0.13μm CMOS Technology.

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## Abstract.

This document describes objectives and method used to characterize DTMOST structures in the 0.13μm CMOS technology. The temperature dependence of the  $I_d(V_{gs})$  relationship is measured and parameterized into a simple mathematical model. On the basis of this model performances of two basic Bandgap reference (BGR) circuits have been evaluated.

The classical voltage summing BGR circuit demonstrates  $V_{ref}=464mV \pm 1.25mV$  in the temperature range from 0°C up to 80°C when ideal opamp and current sources are used. Theoretically this circuit is capable to operate at power supply voltages ( $V_{dd}$ ) as low as  $V_{ref}+V_{ds_{sat}} \approx 600mV$ .

The classical current summing BGR circuit delivers a current as well as a voltage, both remaining stable within a  $\pm 0.3\%$  margin in the temperature range from 0°C up to 80°C when ideal opamp and current sources are used. Because of the current summing architecture theoretically this current summing BGR circuit can operate with a  $V_{dd}$  down to 350mV.

## Introduction.

An on-chip reference circuit insensitive to temperature and power supply variations is a crucial component for high quality A/D and D/A converters. With lower power supply voltages in present deep submicron CMOS technologies (0.13μm) a design of a reference on-chip becomes an important objective.

The classical voltage summing BGR (see Fig.1) featuring a parasitic p-n-p [1] (p-diffusion in N-well) does not fit into a 0.13μm CMOS technology with a maximum  $V_{dd}$  of 1.2V.

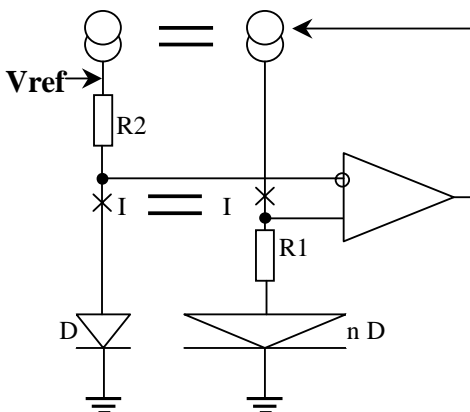


Fig.1. Classical voltage summing Bandgap reference.

A current summing architecture (see Fig.2) can operate at  $V_{dd}$  down to 0.84V [2]. On top of it, this solution provides both a stable voltage and/or a stable current at the output. This circuit could be successfully implemented in 0.13μm CMOS technology. There is a fundamental limitation here due to the voltage drop across a silicon p-n junction. The minimum  $V_{dd}$  is therefore given by:

$$V_{dd_{min}} = V_{be_{p-n \text{ junction}}} + V_{ds_{sat}} \approx 800mV.$$

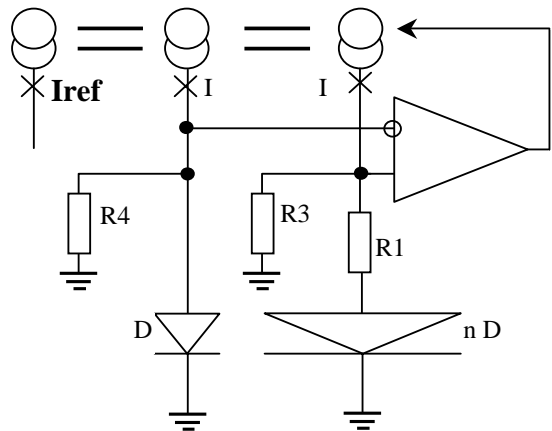


Fig.2. Classical current summing Bandgap reference.

Recently Anne-Johan Annema among others proposed to use a new structure called a dynamic threshold MOS transistor (DTMOST) [3]. A DTMOST is in fact a p-channel MOS (PMOS) transistor with gate, drain and substrate contacts connected together (see Fig.3).

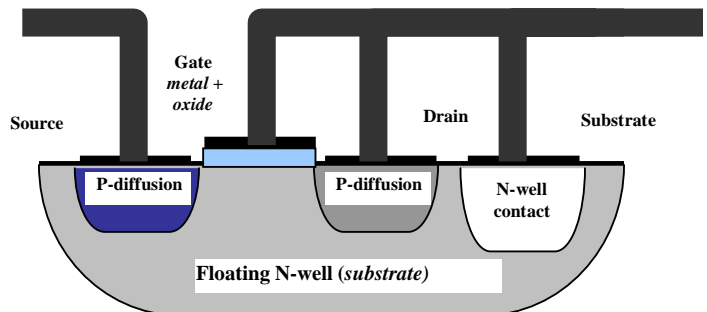


Fig.3. Cross section of a DTMOST structure.

According to Annema, this device can be seen as a PMOS with a dynamically regulated threshold: every change in  $V_{gs}$  causes a change in threshold voltage. The drain current is primarily determined by the voltage across the source-substrate junction. This results in an

ideal exponential relationship between  $V_{gs}$  and  $I_d$ . We can consider this two-terminal device as a diode, but with much lower threshold voltage ( $V_{thr}=200\text{mV}$ ) than a conventional diode ( $V_{thr}=650\text{mV}$ ). This fundamental feature can be combined with a bandgap compensation technique to design a stable reference circuit. Another feature of this device is that the matching of the DTMOST's is about twice as good as the matching between PMOSTs of the same size operating at the same current. Moreover batch-to-batch variations of DTMOST's are about half the value of their PMOST counterparts [3]. He has successfully implemented various BGR circuits featuring DTMOST's in  $0.35\mu\text{m}$  CMOS technology in 1999 [3].

Nowadays we step into  $0.13\mu\text{m}$  CMOS and face the challenge to keep our design within the  $1.2\text{V}$  power supply rails. The DTMOST structure seems to be interesting to look at thanks to its remarkable diode-like behaviour in combination with its low voltage threshold feature. These features let us consider the DTMOST as a key component in future very low supply voltage BGR designs.

In order to design and verify a complete BGR circuit the DTMOST structure needs to be parameterized and modeled.

### The test structures.

Although many various structures were available on the chip we limited ourselves to the enclosed-gate ones. One reason is their better radiation hardness, which needs in our applications, the other reason is that the symmetrical layout will result in better matching properties and might exclude some unwanted and unexpected effects.

The measured structures are (see Fig.4, Fig.5):

- 4-terminal enclosed-gate PMOS with gate width of  $10\mu\text{m}$  and gate length of  $0.12\mu\text{m}$ ,
- 4-terminal enclosed-gate PMOS with gate width of  $10\mu\text{m}$  and gate length of  $0.6\mu\text{m}$
- 4-terminal enclosed-gate PMOS with gate width of  $10\mu\text{m}$  and gate length of  $2\mu\text{m}$ .

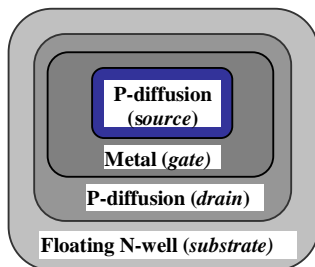


Fig.4. Top view of the Test Structure.

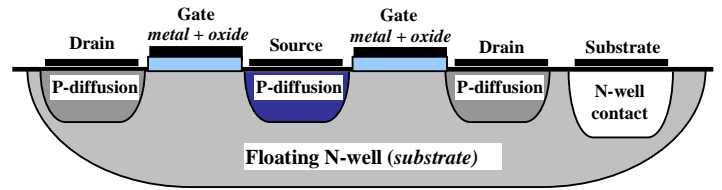


Fig.5. Cross section of the Test Structure.

### Test set-up.

The DTMOST structure characterization consists in the determination of the  $I_d(V_{gs})$  relationship at various temperatures. A chip with various test structures from an experimental  $0.13\mu\text{m}$  CMOS submission was measured in a temperature chamber. A Picoammeter/voltage source device carried out the measurements under control of LabVIEW software. A high precision thermometer with a remote probe is used for accurate monitoring of the temperature (see Fig.6).

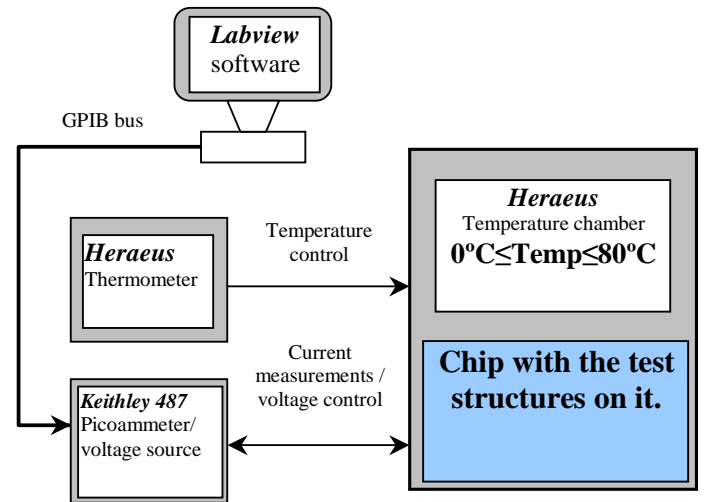


Fig.6. Diagram of the Test Set-up.

The photograph below shows the lay-out of the test set-up. (see Fig.7).

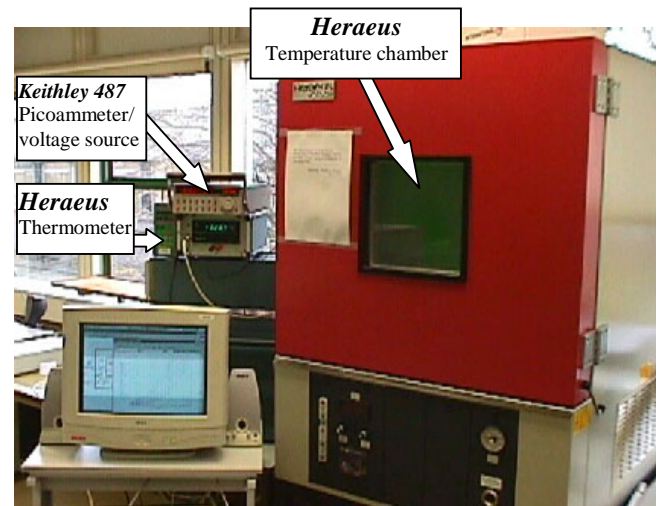


Fig.7. Measurement Set-up.

**DTMOST device compared with a conventional diode.**

In order to illustrate all the features already mentioned it is interesting to compare the  $I_d(V_{gs})$  relationship of a conventional diode with that of a DTMOST structure in 0.13 $\mu\text{m}$  CMOS technology (see Fig.8, Fig.9).

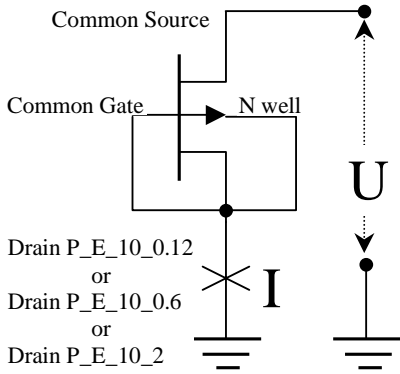


Fig.8. DTMOST configuration on the basis of a PMOS structure.

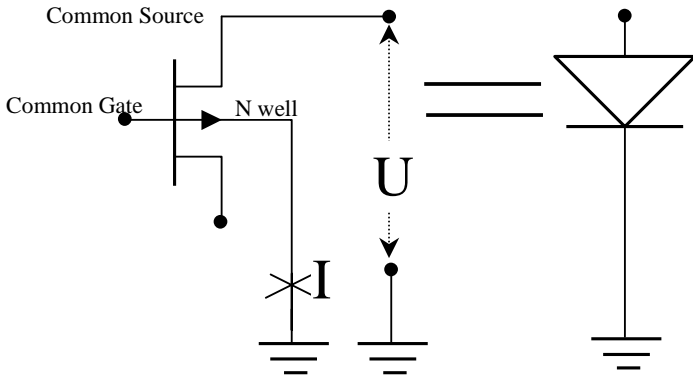


Fig.9. Conventional diode configuration (p-diffusion in N-well) on the basis of a PMOS structure.

The measured current-to-voltage characteristics are given in Figure 10 and 11. The operational threshold of a DTMOST is about 200mV whereas that of a conventional diode is in the vicinity of 650mV (see Fig.10). This feature is crucial in modern low-voltage CMOS circuit designs.

The exponential behaviour of the  $I_d(V_{gs})$  relationship is of primary importance because it enables us to construct a current source which delivers a current that is proportional to the absolute temperature (PTAT). This can be used to implement a mechanism to compensate temperature drift [4]. The conventional diode has an exponential  $I_d(V_{gs})$  relationship above

650mV while the DTMOST configuration is exponential within a region from 100mV to 220mV (see Fig.11).

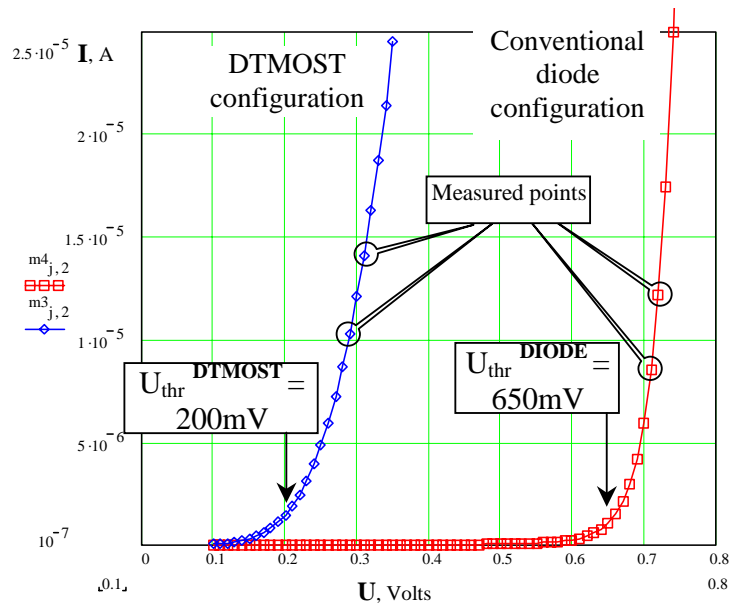


Fig.10. Current-to-voltage characteristics for both DTMOST configuration and conventional diode configuration. Gate area is 10 $\mu\text{m}$ /0.6 $\mu\text{m}$ .

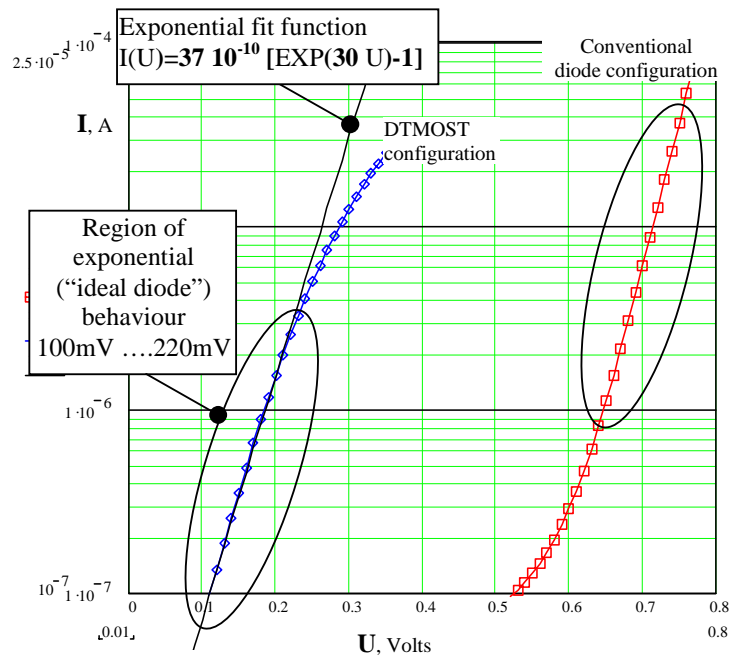


Fig.11. Logarithmic scale. Current-to-voltage characteristics for both DTMOST configuration and conventional diode configuration. Gate area is 10 $\mu\text{m}$ /0.6 $\mu\text{m}$ .

**DTMOST structures on the chip.**

The measured points of the  $I_d(V_{gs})$  relationship are given in Figure12 for all the test DTMOST structures.

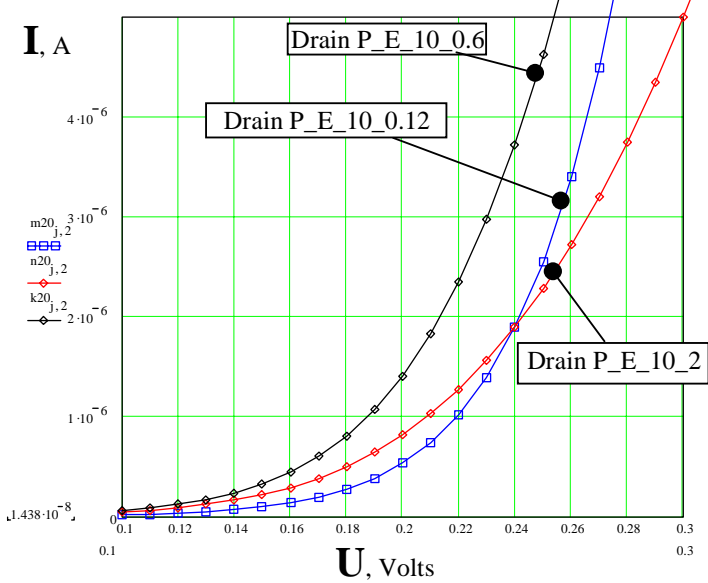


Fig.12. Current-to-voltage characteristics of the DTMOSTs at room temperature (gate areas are:  $10\mu\text{m}/0.6\mu\text{m}$ ,  $10\mu\text{m}/0.12\mu\text{m}$ ,  $10\mu\text{m}/2\mu\text{m}$ ).

The width of the region of the exponential behaviour is the criteria to determine the best candidate for a bandgap reference circuit.

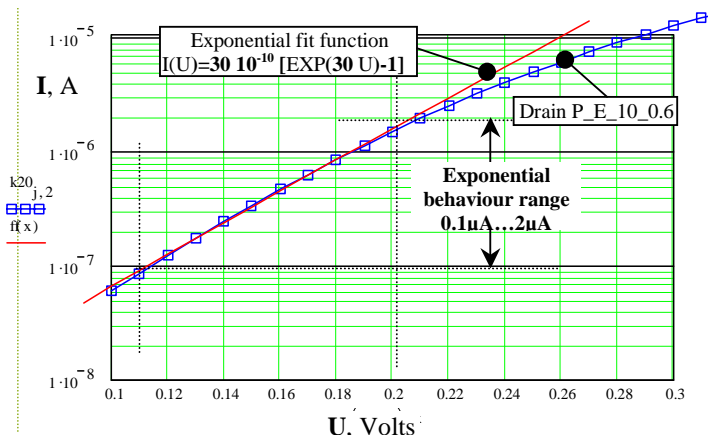


Fig.13. Current-to-voltage characteristic of the DTMOST in logarithmic scale. (gate area is:  $10\mu\text{m}/0.6\mu\text{m}$ )

The minimum channel length DTMOST structure (gate dimensions are  $10\mu\text{m}/0.12\mu\text{m}$ ) shows the widest region of exponential behaviour in the range from  $0.07\mu\text{A}$  up to  $3\mu\text{A}$  (see Fig.13-Fig.15). On the other hand it seems to be risky to use it for a high quality analogue design from the point of view of spread and mismatch. The DTMOST with a gate  $10\mu\text{m}/0.6\mu\text{m}$  is the most

preferable candidate (region of exponential behaviour is from  $0.1\mu\text{A}$  up to  $2\mu\text{A}$ ).

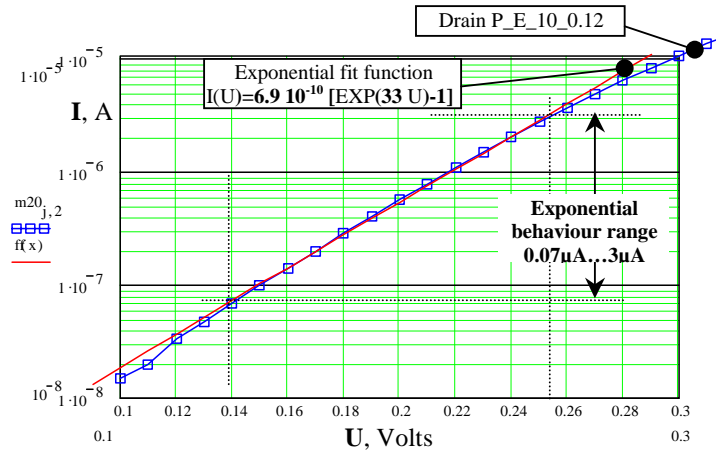


Fig.14. Current-to-voltage characteristic of the DTMOST in logarithmic scale. (gate area is:  $10\mu\text{m}/0.12\mu\text{m}$ )

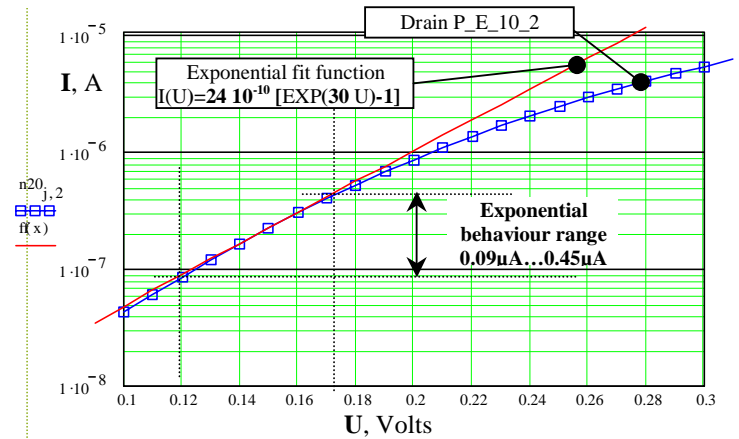


Fig.15. Current-to-voltage characteristic of the DTMOST in logarithmic scale. (gate area is:  $10\mu\text{m}/2\mu\text{m}$ )

**Current-to-voltage characteristics at various temperatures.**

To be able to construct an appropriate model, the DTMOST current-to-voltage characteristic must be measured at various temperatures. The theory predicts that the voltage drop on a DTMOST is Conversely Proportional To the Absolute Temperature (CTAT) at a constant bias current see Figure.16-Figure.18. The steepness of the  $U(T)$  relation depends on the bias current and on the geometry of the DTMOST device and varies between  $4\text{mV}/10^\circ\text{C}$  and  $10\text{mV}/10^\circ\text{C}$  (see Fig.16-Fig.18).

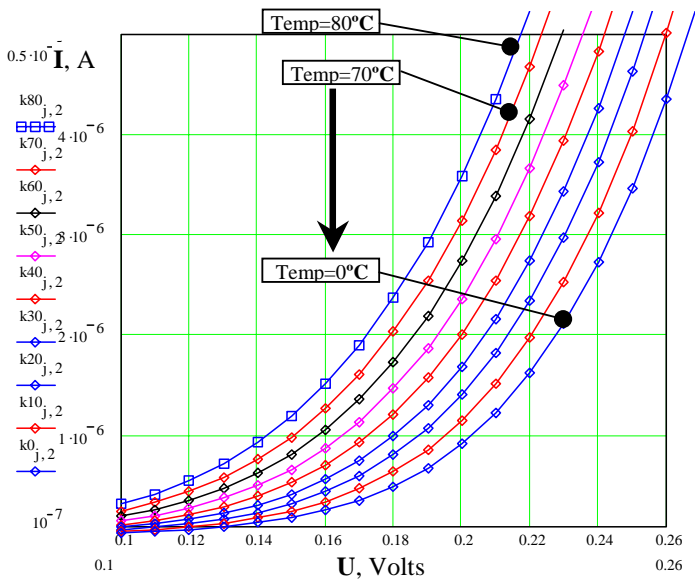


Fig.16. Current-to-voltage characteristic of the DTMOST at various temperatures in the range 0°C ... 80°C with 10°C interval (gate areas is 10µm / 0.6µm).

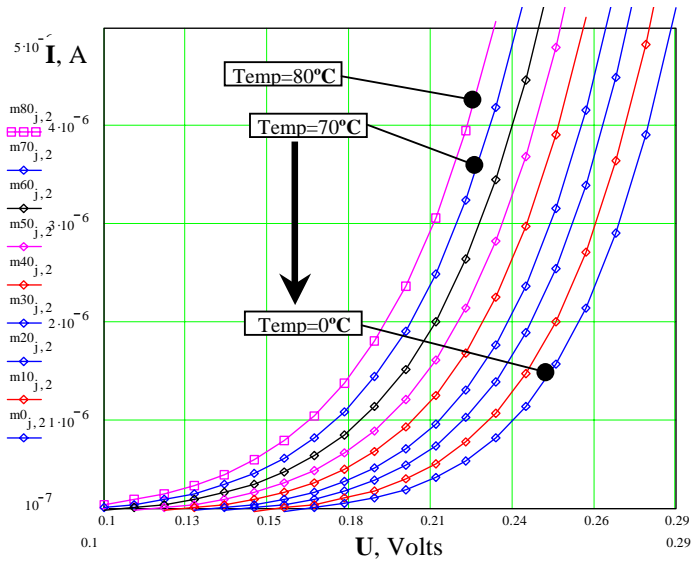


Fig.17. Current-to-voltage characteristic of the DTMOST at various temperatures in the range 0°C ... 80°C with 10°C interval (gate areas is 10µm / 2µm).

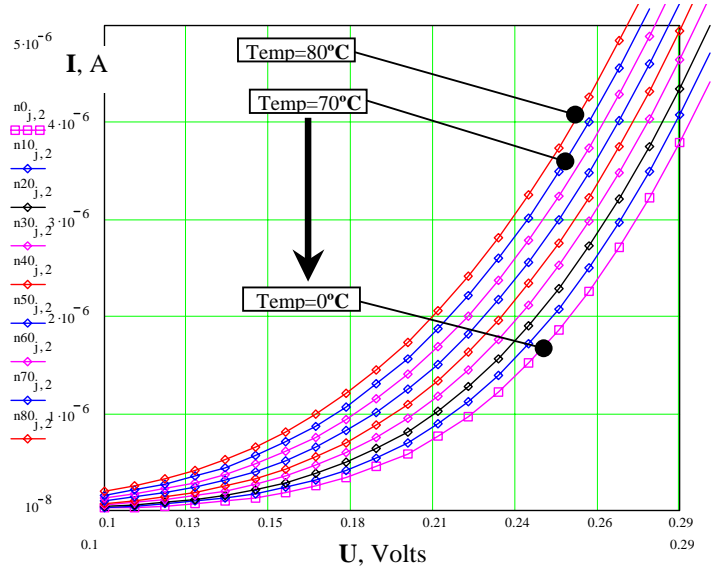


Fig.18. Current-to-voltage characteristic of the DTMOST at various temperatures in the range 0°C ... 80°C with 10°C interval (gate areas is 10µm / 0.12µm).

The extrapolation of the  $U(T)$  dependence down to absolute zero temperature gives an estimation of the bandgap voltage in the DTMOST device (see Fig.19). The estimated bandgap voltage is approximately 410mV for the DTMOST with gate dimensions 10µm/0.6µm.

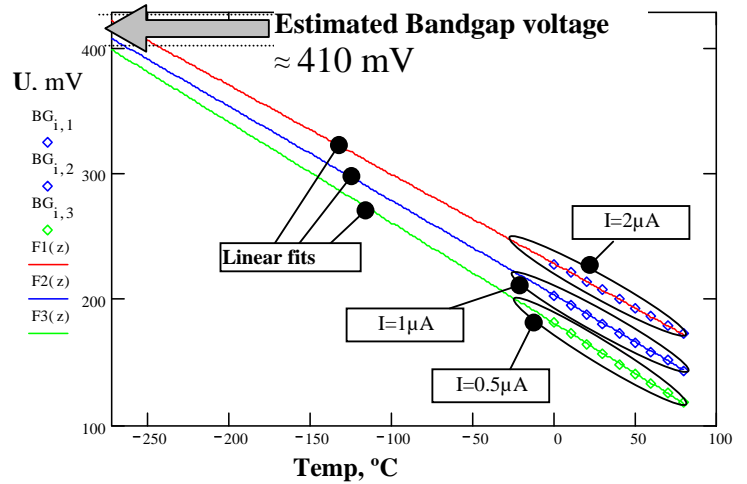


Fig.19. Voltage across the DTMOST at various currents as a function of temperature (gate areas is 10µm/0.6µm).

**Evaluation of the Performance of the Voltage Summing Bandgap Reference circuit.**

Having characterized current-to-voltage dependences at various temperatures we are able to evaluate the performance of some basic BGR circuits. The most common of them is a voltage summing BGR circuit (see Fig.20). Every component of the circuit except for the DTMOST's themselves, have been considered ideal when estimating the temperature stability of the output voltage ( $V_{ref}$ ). In a real design a full temperature dependent SPICE simulation will, of course be needed, including non-ideal components.

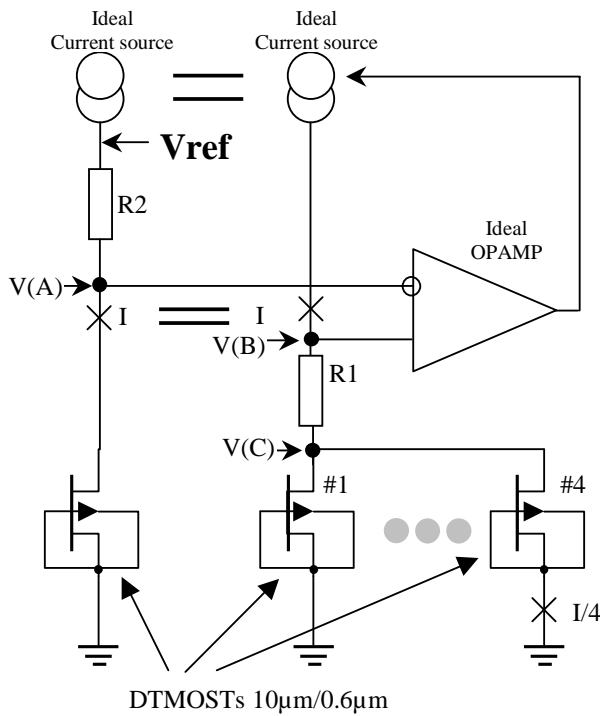


Fig.20. Schematic of a semi-ideal voltage summing BGR circuit with the DTMOST's (gate dimensions  $10\mu\text{m}/0.6\mu\text{m}$ ).

The quiescent current in the stable operation point of the circuit is given as

$$I_o(T) = [kT/e] \ln(A) [1/R1], \text{ where}$$

$T$  is the absolute temperature,

$k$  is Boltzmann's constant,

$e$  is the electron charge,

$A$  is the ratio of DTMOST's areas in both branches of the circuit.

To keep the operating point of the DTMOST's within the region of exponential behaviour ( $0.1\mu\text{A} < I_o < 2\mu\text{A}$ ) the parameter  $A$  is chosen equal to 4 and  $R1$  is  $30\text{k}\Omega$ .

A simple linear interpolation was used to form a continuous function out of the measured data values (see

Fig.21). The quiescent operation point occurs at  $V(A)=V(B)$  (see Fig.21)

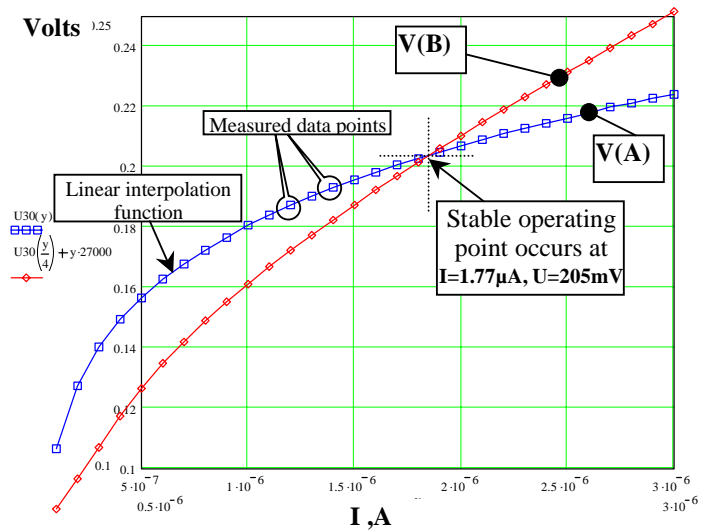


Fig.21. Voltage at the inputs of the OPAMP as a function of current at  $30^\circ\text{C}$ .

The temperature drift of the voltages in the stable operation point is conversely proportional to the absolute temperature (CTAT) (see Fig.22). The voltage drop across the resistor  $R1$  is on the contrary directly proportional to the absolute temperature (PTAT) (see Fig22).

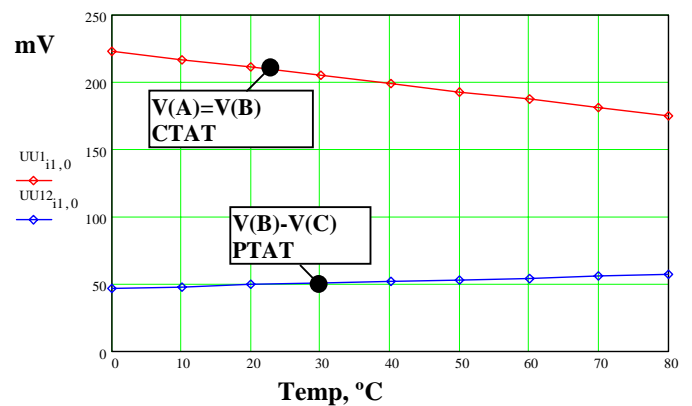


Fig. 22. Temperature drift of the voltages in the voltage summing BGR circuit.

Figure 22 shows the different slopes of the curves. For the precise compensation of the temperature drifts the following condition must be met:

$$R2 = R1 [\text{Slope(CTAT)}/\text{Slope (PTAT)}]$$

Under this condition the output voltage (see Fig.23)  $V_{ref}=464\text{mV}$  remains temperature insensitive within a margin of  $\pm 1.25\text{mV}$  (see Fig 21).

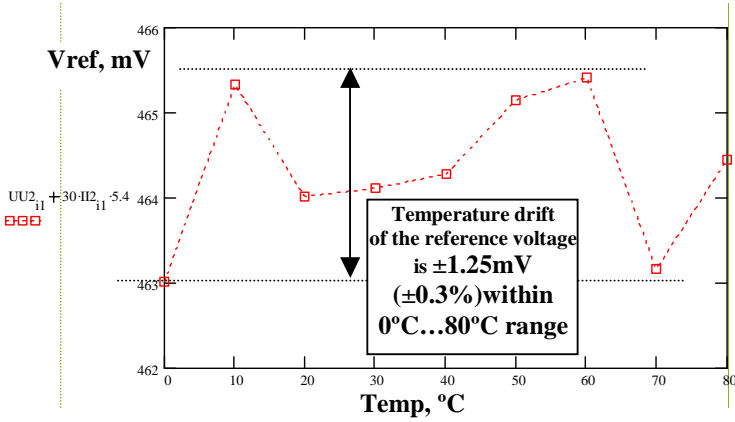


Fig. 23. Temperature drift of the reference voltage ( $V_{ref}$ ) ( $R1=30\text{k}\Omega$ ,  $R2=162\text{k}\Omega$ ).

**Evaluation of the Performance of the Current Summing Bandgap Reference circuit.**

The current summing BGR circuit employs the same mechanism of temperature compensation as the voltage summing BGR (see Fig.24). This circuit delivers a stable reference current that can be converted into a stable voltage if necessary.

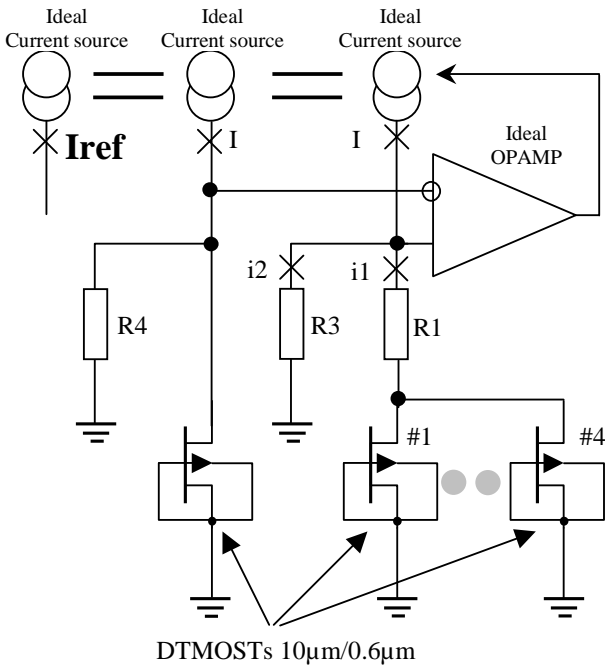


Fig.24. Schematic of a semi-ideal current summing BGR circuit with the DTMOST's (gate dimensions  $10\mu\text{m}/0.6\mu\text{m}$ ).

Each of the ideal current sources drives current  $I$  (see Fig.25) equal to

$$I=i1(\text{PTAT}) + i2(\text{PTAT})$$

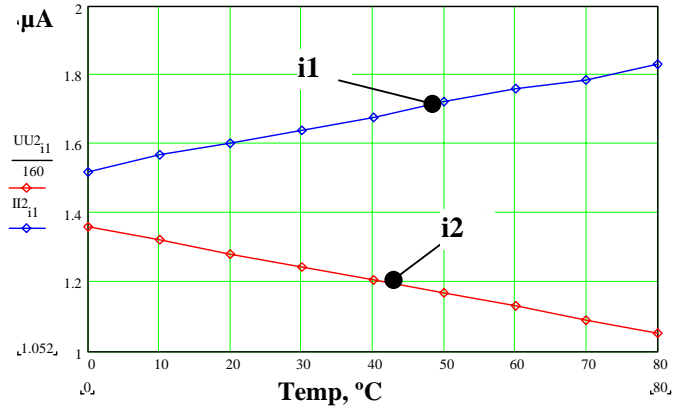


Fig.25. Temperature drift of the currents in the current summing BGR circuit ( $R3=R4=160\text{k}\Omega$ ,  $R1=30\text{k}\Omega$ ).

The sum of the partial currents ( $i1$ ,  $i2$ ) is  $I=2.882\mu\text{A}$  and remains constant within  $\pm 0.3\%$  in a temperature range from  $0^\circ\text{C}$  to  $80^\circ\text{C}$  (see Fig.26).

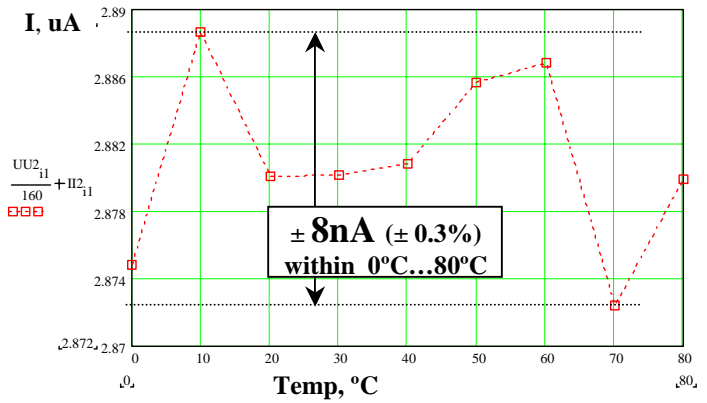


Fig. 26. Temperature drift of the reference current ( $I_{ref}$ ) ( $R3=R4=160\text{k}\Omega$ ,  $R1=30\text{k}\Omega$ ).

### Conclusions.

The current-to-voltage relationship  $I_d(V_{gs})$  of the DTMOST's have been measured at various temperatures. The DTMOST structures came from an experimental submission in 0.13 $\mu\text{m}$  CMOS technology. The measurements have been the basis to evaluate performances of two principal bandgap reference (BGR) circuits assuming ideal opamps and ideal current sources inside.

The measured DTMOST structures show a valid exponential behaviour, which can be used to construct a device with a PTAT characteristic.

Within a temperature range from 0°C to 80°C the voltage summing BGR circuit can provide a reference voltage of  $V_{ref}=464\text{mV}\pm 1.25\text{mV}$  and supposedly is capable to operate at a  $V_{dd}$  as low as 600mV. In the same temperature range, the current summing BGR circuit can generate a reference current  $I_{ref}=2.882\mu\text{A}\pm 8\text{nA}$  (or  $\pm 0.3\%$ ) and would supposedly be able to operate at a supply voltage down to 350mV.

The DTMOST structure seems to be an attractive candidate for very low-voltage bandgap reference circuits.

### Acknowledgements.

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I thank Ruud Kluit for giving me productive ideas on the test facilities and Fred Schimmel for his help in handling LabVIEW software.

### References.

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