

ETR 2001-01

**B-Timizer,
32 channel time digitizer
with L1 buffer for the
LHCb Outer Tracker
Chambers.**

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Abstract:

The B-Timizer boards hosts one 32-channel TDC (with integrated L0 buffer) and L1 buffer and logic. The B-Timizer receives and distributes L0 and L1 triggers and reset signals. Upon an L0 accept, the TDC is read out and its data is stored in the L1 buffer. Upon an L1 accept, the event data is read from the buffer and transmitted over a serial link.

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1. Introduction

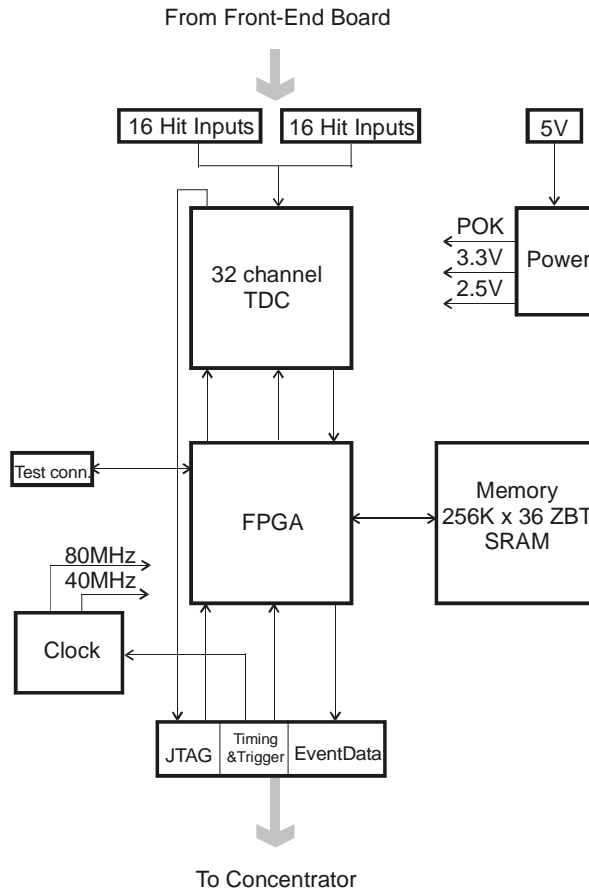


Figure 1: Block Diagram

The B-Timizer consists of a 32 channel TDC, a 256K x 36 bit memory (L1 Buffer) and an FPGA. The TDC is the HPTDC [1] with an integrated 256 deep L0 buffer. The FPGA contains the control logic to write the L0 data from the TDC into the L1 Buffer, to read the L1 data from the L1 Buffer and to serialize the L1 data using the physical layer of the DS Link protocol [2].

The B-Timizer has to function in a radiative environment and therefore a simple design has been chosen without the use of LookUp Tables. In this proto-type an Altera 1K30 FPGA is used, together with a serial PROM (EPC2) to program the FPGA. Later this should be changed into a rad-tolerant device like a laserprocessed or an antifuse FPGA. In the design, the maximum number of hits per event has been limited to 61 hits. The event data stored in the L1 Buffer consists of TDC hits, a B-Timizer header, a TDC header and a TDC trailer, all 32 bits wide, and this takes up to 64 addresses in the L1 Buffer. The L1 Buffer can store 4K L0 events at an average rate of 1MHz allowing the specified L1 latency of 2 milliseconds [3]. This is compatible with the LHCb specifications.

The system clock of the B-Timizer is 40 MHz and is derived from the TTC system [4]. The system clock is doubled to get an 80 MHz clock to be used as clock for the L1 Buffer read/write access and as clock for the output serializer to achieve the required output data rate of 80 Mb/sec.

The differential hit signals (LVDS type) are connected to the board via two 64 pins High-Density connectors. They are converted to LVTTTL and fed to the TDC.

The output connector is a 25p D-type connector connected to the Concentrator [5]. It carries the serial event data, the trigger information extracted from the TTC system, and the JTAG signals to control the B-Timizer. All signals to and from the B-Timizer are differential LVDS type signals.

An additional test connector is connected to the FPGA and is used for debugging purposes.

2. Mechanical considerations

The board outline corresponds to the Common Mezzanine Card (CMC) specifications. The power can be derived from the 64p High-Density connectors or from the 25 pin D-type connector depending of the power jumpers.

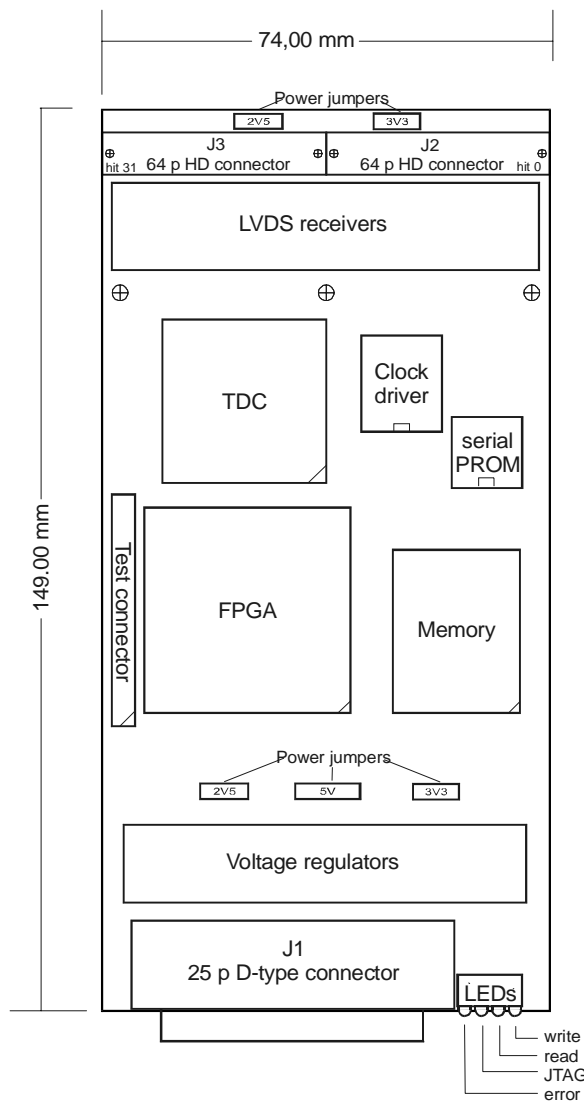


Figure 2: Board Outline

The board can be directly connected to a front-end board with 4 ADSBLRs. This will probably be the case for 2112 of the B-Timizers at T7, T8, T9 and T10 (depending of the radiation level). The adapter board is needed to interface the front-end board to the B-Timizer.

The ‘in magnet’ detectors (T2, T3, T4, T5, T6) do not allow on-detector B-Timizers. Here 1368 of

the B-Timizers are connected via cables to the front-end board. Three B-Timizers can be mounted on a 6U host board. A 6U Euro crate can contain up to $20 \times 3 = 60$ B-Timizers (3 B-Timizers in one slot). So 23 crates will be needed for these stations. An example of both setups is given in Figure 3a and 3b.

In Figure 3c and 3d a possibility is given to accommodate high occupancy detector channels. On the adapter boards only 16 channels are routed to the TDC on the B-Timizer, in such a way that 4 channels out of a group of 8 channels, sharing the same L0 buffer, are used. This doubles the L0 buffer space per channel and avoids ‘overrun errors’ in the TDC.

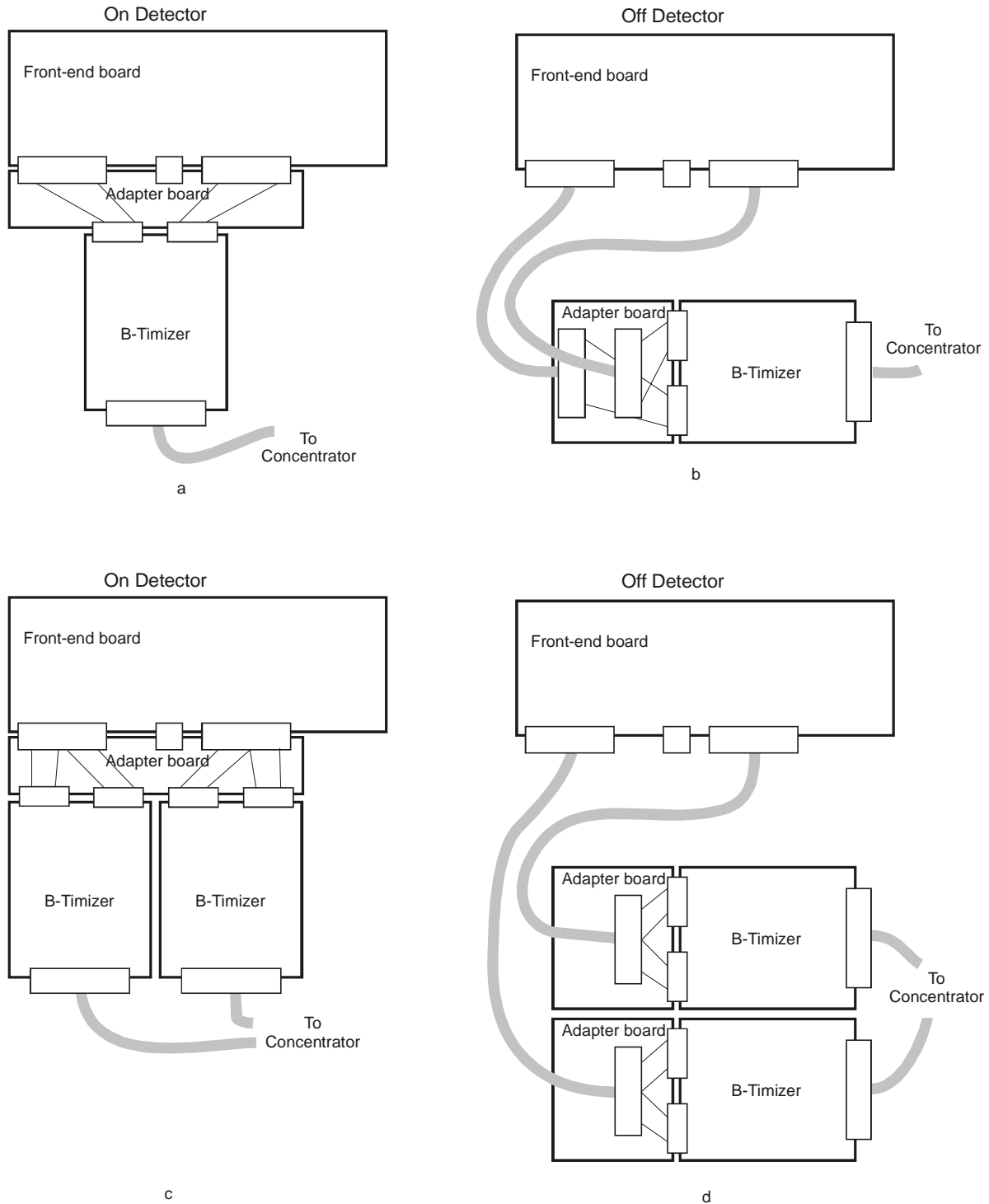


Figure 3: B-Timizer connections

3. Functional Description

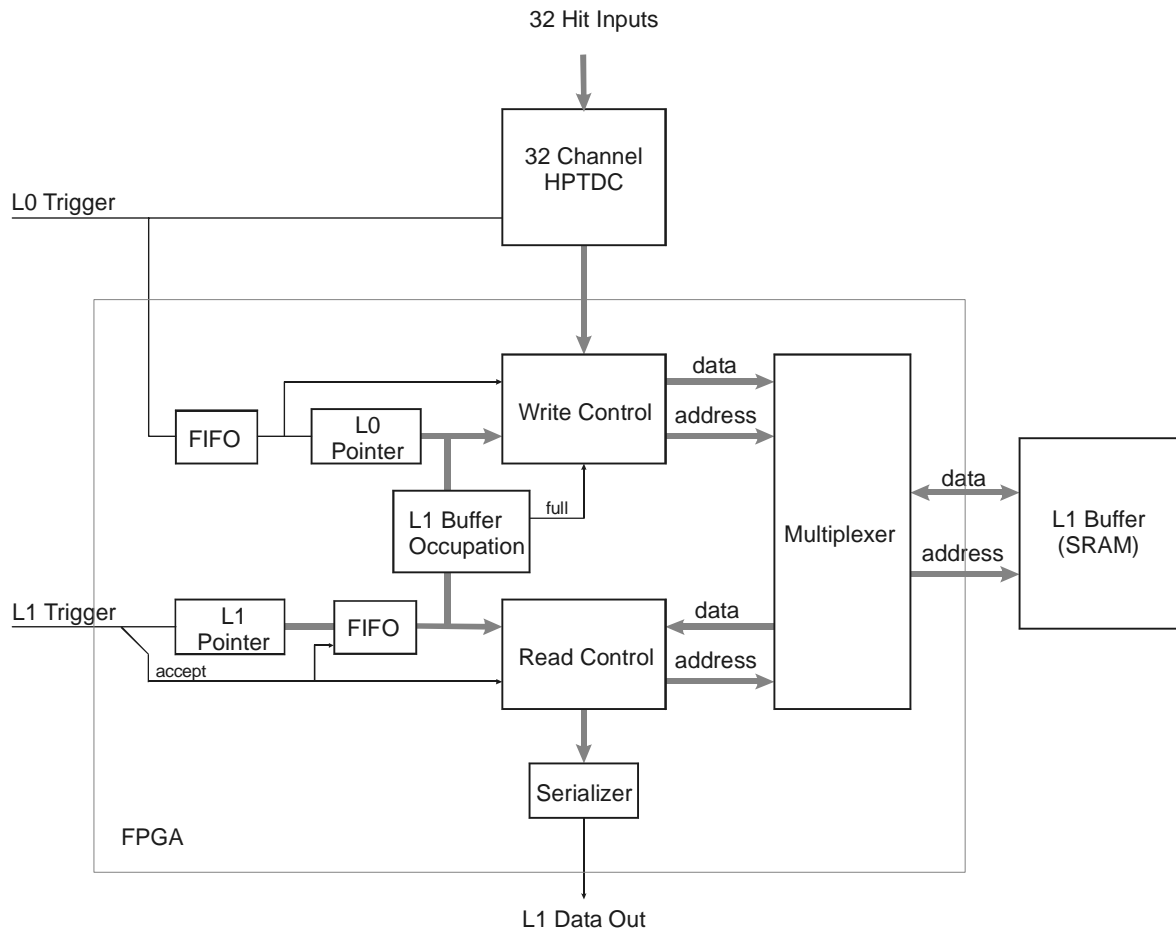


Figure 4: Functional diagram

3.1 Write Control

The L0 trigger is derandomized in a counter that acts as a 1 bit FIFO and counted both in the L0 Pointer counter and the L0 Event ID counter: the L0 Event ID is reset by the Event Count Reset (EC Reset) while the L0 pointer is not. As long as the FIFO is not empty, the Write Control reads an event from the TDC and stores the event data in the L0 Buffer starting with the TDC header at address $((L0\ Pointer * 64) + 1)$ and then the TDC hit data all the way through the TDC trailer. After the TDC trailer, a random amount of test data can be inserted. The maximum number of test data is specified in the JTAG-controlled Command register (TestId[2:0]). Finally, a B-Timizer header containing the 12 bit L0 Event ID and an 8 bit word count and error flags is inserted at address $(L0\ Pointer * 64)$. This completes the writing of an event in the L1 Buffer. All data formats are given in section 6.

If the L1 Buffer gets full (L0 Pointer wraps around and reaches the L1 Pointer), the data from the TDC is flushed and a 6-bit memory-full counter is incremented. These events will later appear in the L1 buffer as 'empty' events with the Empty Event flag on in the B-Timizer header and Error Flags, the L1 Buffer full flag in the Error Flags will be set (see section 3.3). When the memory-full counter is 63, the L1 Buffer overflow in the Error Flags will be generated and events will be lost. An L1 Reset or JTAG Reset will be needed to recover from this situation.

If an event from the TDC is longer than the event length specified in the Command register (MaxEvt[1:0]), the exceeded TDC data is skipped until the TDC trailer is received. In the B-Timizer header the Event overflow bit is set. The difference between the word count in the TDC trailer (+2) and the word count in the B-Timizer header gives the amount of data that was skipped. Care must be taken that the number of hits (MaxEvt), plus the amount of testdata (TestID), plus the two headers and one trailer does not exceed 64.

The TDC generates one 32-bit word for each hit. To reduce the amount of data in an event the MergEn option is added. When the MergEn bit in the Command register is set two words from the TDC are merged into one 32-bit word by omitting the most significant bits of the coarse time and diminishing the fine time from 8 bits to 5 bits (800 ps resolution). A coarse error bit (bit 26) is set in the merged TDC data when the coarse time of a hit is out of range. The data format is described in section 6.

3.2 L1 FIFO

The L1 Accept and Reject increment the L1 Pointer, which is reset (as well as the L0 Pointer) by L1 Reset. At an L1 accept, the L1 pointer and the 2 bits ID from the TTC system and the L1 FIFO Overflow flag are written into the 16 deep L1 FIFO. The FIFO Full flag is set both in the B-Timizer header and Error Flags if a watermark, set to 12, is reached in the L1 FIFO. The L1 FIFO Overflow flag in the Error Flags is asserted when 15 L1 accepts are stored in the L1 FIFO and will remain asserted until a L1 Reset or JTAG Reset is given.

3.3 Read Control

As long as the L1 FIFO is not empty, the Read Control reads its content (L1 Pointer, the 2 bits ID and the L1 Overflow flag). Then the B-Timizer header (with the 12 bit Event ID) is read from the L1 Buffer using the L1 Pointer as address. The two least significant bits of the Event ID in the B-Timizer header are compared with 2 bits ID from the L1 FIFO and the L0 Event ID error flag in the B-Timizer trailer is set if the bits do not match. Then the event data is read from the L1 Buffer, the parity is checked and the data is transferred to the Serializer. The word count in the B-Timizer header is used to determine the last address to read; after this last word is transferred to the Serializer, a B-Timizer trailer is generated by the Read Control and is sent to the Serializer.

When the L1 FIFO Full flag is detected in the B-Timizer header, only the B-Timizer header followed by a B-Timizer trailer is sent to the Serializer. In this way the L1 FIFO is emptied faster to cancel the full condition. The trailer contains the B-Timizer ID, the 12 bits Event ID and the following flags: L0 Event ID error or Broadcast Parity error (from the TTC Chan B decoder), L1 FIFO Full, Parity Error and Error Detected. The Error Detected bit is the 'OR' of all error flags and if it is set, an Error Flag word is appended after the event trailer. This Error Flag word is not counted in the Event Header word count.

3.4 Multiplexer and L1 Buffer

The L1 Buffer is a synchronous, single-port ZBT SRAM of 256K x 36 bits. The Multiplexer and L1 buffer are clocked at 80MHz; this enables a write and a read during one system-clock (40 MHz) cycle

The Multiplexer takes care of the multiplexing between the write and read addresses, the pipelining of the write data and it generates the (even) parity bits for the write data (4 bits for each 32-bit word in the L1 Buffer).

3.5 Serializer

The Serializer generates the serial data using the physical layer of the DS Link protocol [2], where the data and clock are encoded in Data and Strobe in such a way that on the serial clock there is a transition on Strobe when there is no transition on Data (figure 5).

The Serializer adds a start bit, a parity bit and a stop bit. The serial clock can be 40 MHz or 80 MHz controlled by ScIkSel in the Command register.

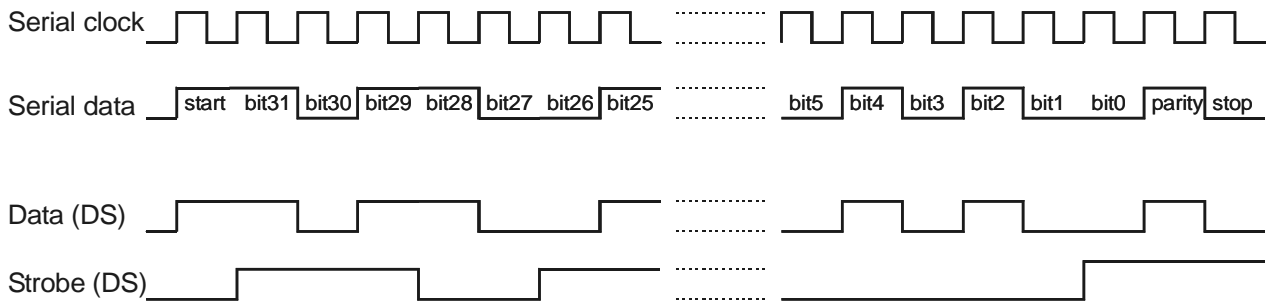


Figure 5: Serial frame format

4. L1 Trigger and Resets

The L1 Trigger and various resets are derived from the serial Broadcast channel (Channel B) of the TTC system [1]. The broadcast frame is given in figure 6.

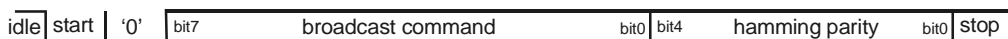


Figure 6: Broadcast frame

Parity bits 0 to 3 are used to correct single bit errors according to the Hamming code:

- Parity bit 0 checks bit 7, 6, 4, 3 and 1 of the broadcast command,
- Parity bit 1 checks bit 7, 5, 4, 2 and 1 of the broadcast command,
- Parity bit 2 checks bit 6, 5, 4 and 0 of the broadcast command,
- Parity bit 3 checks bit 3, 2, 1 and 0 of the broadcast command.

Parity bit 4 is the even parity of the 8 bit broadcast command and is used to detect double bit errors. In case of a double bit error the broadcast parity error bit is set.

5. JTAG

The B-Timizer is controlled by means of a 4-wire JTAG bus (TAP). The instructions, data and control signals are all passed along this serial bus. The TAP controller monitors two signals from the serial bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the bus and generates the appropriate control signals to access the control and data registers in the B-Timizer. The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one half of the TCK cycle.

The B-Timizer contains one JTAG port accessible from the 25-p D-type connector. The JTAG chain (figure 7) consists of four devices: the emulated JTAG port in the FPGA together with the JTAG port of the TDC is used to control the B-Timizer; The EPC2 port and the standard JTAG port of the FPGA (byteblast) are used to program the FPGA. The JTAG port of the TDC is described in the TDC specification [2] and the emulated JTAG port in the FPGA is described in the next section.

The JTAG jumper should be in the 1 – 2 position to program the EPC2, or the FPGA via the byteblast port, for the first time.

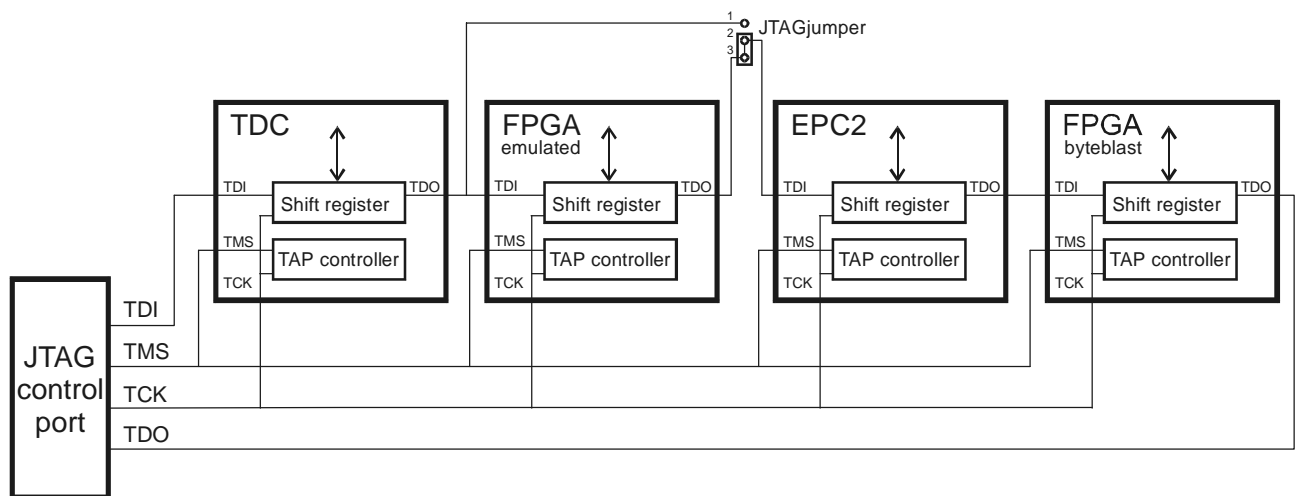


Figure 7: JTAG chain

5.1 FPGA JTAG port

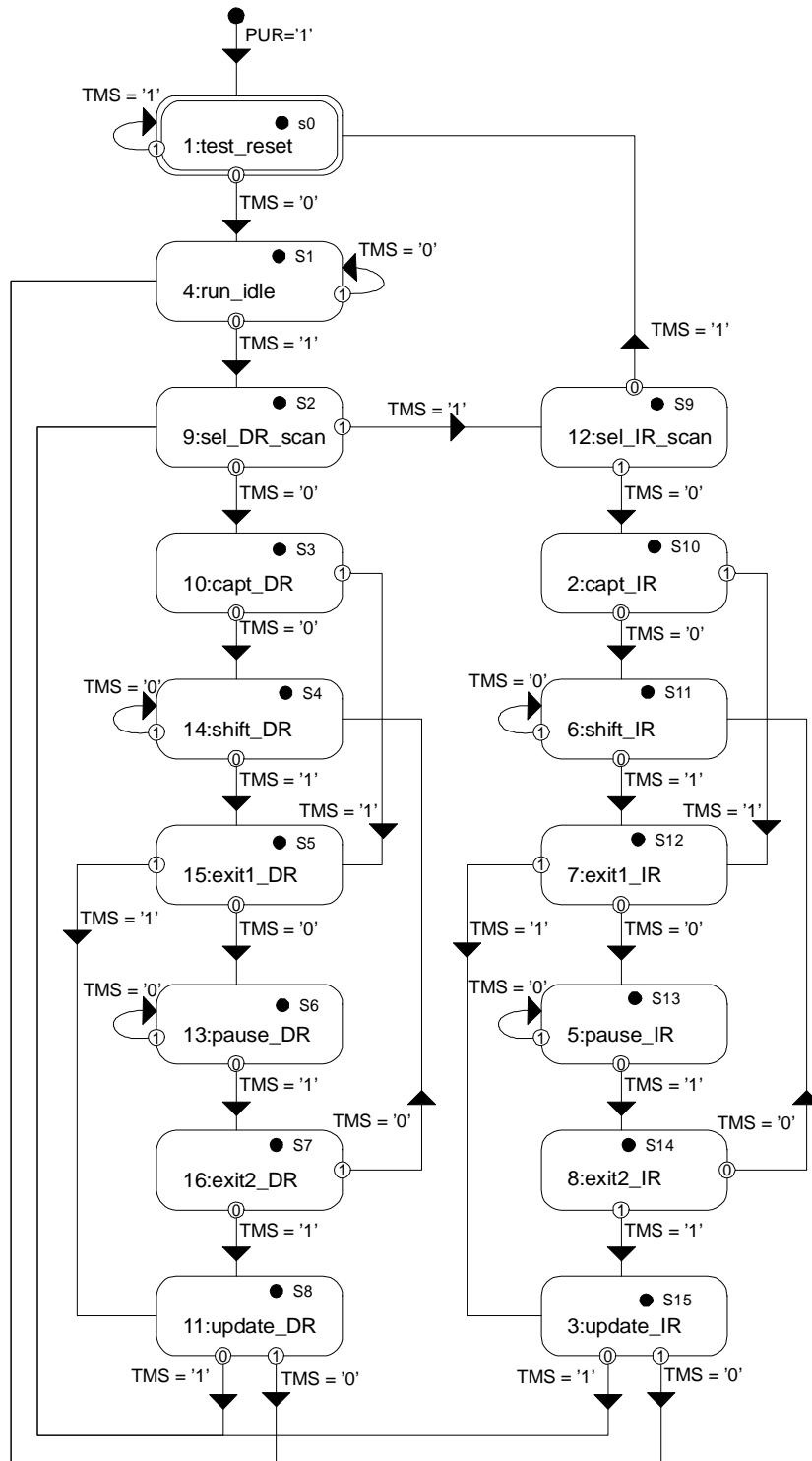


Figure 8: TAPcontroller state diagram

The state diagram of the emulated TAP controller in the FPGA is given in figure 8. To control the B-Timizer the FPGA contains a 4-bit instruction register, five 12 bit data registers (Command

register, Identification Code, Event ID offset, Error flags, Version code) and a 32 bit Event data register.

Instruction Register	Register	Read/Write
0000	Command register reset	Read/Bit reset
0001	Command register set	Read/Bit set
0010	Identification Code	Read/Write
0011	Event ID offset	Read/Write
0100	Error flags	Read only
0101	Version Code	Read only
0110	Event data	Read only
0111-1111	Bypass	Read/Write

5.2 Command register (IR=0000 IR=0001)

The Command register cannot be directly written into but is bit-selective set (IR = 0001) or reset (IR = 0000). On ‘capture DR’ with IR = 0000 or IR = 0001 the contents of the Command register is copied in the JTAG shift register for reading.

Command register							
Bit 11:10	Bit 9	Bit 8	Bit 7,6,5	Bit 4,3	Bit 2	Bit 1	Bit 0
unused	MergEn	JtagRo	TestId[2:0]	MaxEvt[1:0]	SclkSel	Ena	Rst

Rst (bit 0) generates a global reset for the TDC and clears all counters and state machines to their initial state and resets all error flags.

Ena (bit 1) enables the module to read the TDC, store the data in the memory and on a L1 read the data from L1 Buffer and send the serialized data to the concentrator. If the enable bit is off no data is read from the TDC and a dedicated header and trailer is sent to the concentrator on every received L1 trigger.

SclkSel (bit 2) specifies the clock frequency of the serializer. If SclkSel is set, the clock frequency is 80 MHz otherwise it is 40 MHz.

MaxEvt[1:0] (bit 4,3) determines the maximum event length of an event stored in the L1 Buffer. If an event from the TDC is longer than the specified event length, the exceeded TDC data is skipped until the TDC trailer is received and in the B-Timizer header the Event overflow bit is set

MaxEvt	Number of hits
0	7
1	15
2	31
3	61

TestID[2:0] (bit 7,6,5) enables to insert a random number of test-data words into an event. The maximum number is given in the table below. When the module is disabled (Ena = 0) and the TestId = 4 the number of test words is fixed on 63 in this way a simple memory and readout test is possible.

TestID	Number of test- words
0	0
1	16
2	32
3	63
4	Fixed 63
5-7	TBD

JtagRo (bit 8) enables event read out by JTAG and disables the output via the serializer.

MergEn (bit 9) enables two TDC data words to merge into one 32-bit word.

If MergEn is set the Channel ID, 5 MSBits of the fine time and the 3 LSBits of the coarse time are put in the event description. The coarse time of the merged data words are checked and if it is out of range the CoarseErr bit is set.

5.3 Identification Code (*IR=0010*)

The Identification Code (B-T ID) is a programmable 12 bits number that uniquely identifies the B-Timizer board. It appears in the event data.

5.4 Event ID offset (*IR=0011*)

The Event ID offset (12 bits) is the start value of the event counters and is loaded in the event counters upon a reset.

5.5 Error Flags (*IR=0100*)

The Error flags are latched and reset after read by JTAG.

Bit 0	Event overflow flag
Bit 1	L0 FIFO full flag
Bit 2	L1 Buffer full flag
Bit 3	L0 FIFO overflow, L1 Reset or JTAG Reset needed
Bit 4	L1 Buffer overflow, L1 Reset or JTAG Reset needed
Bit 5	L0 Event ID error flag
Bit 6	'0' L1 FIFO full flag
Bit 7	'0' L1 FIFO overflow, L1 Reset or JTAG Reset needed
Bit 8	Broadcast parity error
Bit 9	Header parity error
Bit 10	TDC parity error
Bit 11	Uncorrectable error, L1 Reset or JTAG Reset needed

5.6 Version Code (*IR=0101*)

The 12 bits Version Code is read-only and is used to identify the version of the B-Timizer.

Version Code 01	jan. 2001	first prototype.
Version Code 02	jan. 2002	

5.7 Event Data (*IR=0110*)

When the JtagRo bit in the Command register is on, the event and test data will appear in this 32-bit register, the data is valid if it is unequal to zero. In this way the B-Timizer can be tested

without the need of a Concentrator. When the JtagRo bit is off uncorrelated samples of the event data can be read from this register.

6. Data format

The description below gives a summary of the data format used by the B-Timizer. The TDC data format is given in the TDC specification [2]. The programmed TDC ID is reduced to 3 bit to enable a 'merged data bit' (bit 27) in the event description. Bit 31 is set in data generated by the B-Timizer.

B-Timizer Header

- Bit 31 – 28 Word type identifier = 1010
- Bit 27 – 24 Four least significant bits of the programmed B-Timizer ID
- Bit 23 – 12 12 bits Event ID from the event counter
- Bit 11 – 8 Error flags:
 - Bit 11 Empty Event (event does not contain valid TDC data)
 - Bit 10 L1 FIFO full
 - Bit 9 L0 FIFO full
 - Bit 8 Event overflow
- Bit 7 – 0 Number of words in event, inclusive headers and trailers but exclusive Errors word

TDC Header

- Bit 31 – 28 Word type identifier = 0010
- Bit 27 – 24 the programmed TDC ID
- Bit 23 – 12 12 bits Event ID from the TDC
- Bit 11 – 0 12 bits Bunch ID from the TDC

TDC Data

- Bit 31 – 28 Word type identifier = 0100
- Bit 27 '0'
- Bit 26 – 24 three least significant bits of the programmed TDC ID
- Bit 23 – 19 5 bits TDC channel number
- Bit 18 – 8 11 bits Coarse time
- Bit 0 – 7 8 bits Fine time (100ps-resolution mode)

Merged TDC Data

- Bit 31 – 28 Word type identifier = 0100
- Bit 27 '1' = merged data bit
- Bit 26 Coarse time error, coarse time in one of the channels is out of range
- Bit 25 – 21 5 bits TDC channel number
- Bit 20 – 18 3 least significant bits of the Coarse time
- Bit 17 – 13 5 bits fine time (800ps resolution)
- Bit 12 – 8 5 bits TDC channel number
- Bit 7 – 5 3 least significant bits of the Coarse time
- Bit 4 – 0 5 bits fine time (800ps resolution)

TDC Trailer

- Bit 31 – 28 Word type identifier = 0011
- Bit 27 – 24 the programmed TDC ID
- Bit 23 – 12 12 bits Event ID from the TDC
- Bit 11 – 0 12 bits Word count from the TDC, (a merged data word counts double).

B-Timizer Trailer

- Bit 31 – 28 Word type identifier = 1101
- Bit 27 – 24 Four least significant bits of the programmed B-Timizer ID
- Bit 23 – 12 12 bits Event ID from the event counter
- Bit 11 – 8 Error flags:
 - Bit 11 Error Detected. ‘OR’ of all error sources. If this bit is set an error flag word is appended after the trailer. This flag word is not counted in the header word count!
 - Bit 10 Parity Error
 - Bit 9 L1 FIFO full
 - Bit 8 L0 Event ID error or Broadcast parity error
- Bit 7 – 0 bit 4 – 11 of the programmed B-Timizer ID

Errors

- Bit 31 – 28 Word type identifier = 1001
- Bit 27 – 24 Four least significant bits of the programmed B-Timizer ID
- Bit 23 - 20 "0000"
- Bit 19 - 16 TDC Parity. 4 bit even parity of all TDC or test data in the event (one bit for each byte).
- Bit 15 - 12 Header Parity. 4 bit even parity of event header (one bit for each byte).
- Bit 11 - 10 "00"
- Bit 9 Broadcast parity error, reset needed.
- Bit 8 L1 FIFO overflow, reset needed.
- Bit 7 L1 FIFO full flag.
- Bit 6 Event ID error flag.
- Bit 5 L1 Buffer overflow, reset needed.
- Bit 4 L0 FIFO overflow, reset needed.
- Bit 3 Empty Event (event does not contain valid TDC data)
- Bit 2 L1 Buffer full
- Bit 1 L0 FIFO full
- Bit 0 Event overflow

6.1 Event Record example

Below an event description is given of an event with five hits

Description	Bit 31 - 28	Bit 27 - 24	Bit 23 - 20	Bit 19 - 16	Bit 15 - 12	Bit 11 - 8	Bit 7 - 4	Bit 3 - 0
B-Timizer header	1010	B-T ID (3-0)		Event ID (12bits)			Error flags	Word count
TDC header	0010	TDC		Event ID			Bunch ID	
TDC data	0100	0	TDC	Channel	Coarse time		Fine time	
More TDC data	0100	0	TDC	Channel	Coarse time		Fine time	
More TDC data	0100	0	TDC	Channel	Coarse time		Fine time	
More TDC data	0100	0	TDC	Channel	Coarse time		Fine time	
More TDC data	0100	0	TDC	Channel	Coarse time		Fine time	
TDC trailer	0011	TDC		Event ID			TDC Word count	
Test data *	1100	Shifted 1's						
B-Timizer trailer	1101	B-T ID (3-0)		Event ID (12bits)			Error flags	B-T ID(11-4)
Errors	1001	B-T ID (3-0)		Error Flags				

The same event but now with merged data

Description	Bit 31 - 28	Bit 27 - 24	Bit 23 - 20	Bit 19 - 16	Bit 15 - 12	Bit 11 - 8	Bit 7 - 4	Bit 3 - 0	
B-Timizer header	1010	B-T ID (3-0)		Event ID (12bits)			Error flags	Word count	
TDC header	0010	TDC		Event ID			Bunch ID		
Merged TDC data	0100	1	C E	Channel	Crse time	Fine time	Channel	Crse time	Fine time
More Merged TDC data	0100	1	C E	Channel	Crse time	Fine time	Channel	Crse time	Fine time
More Merged TDC data	0100	1	C E	00000	000	00000	Channel	Crse time	Fine time
TDC trailer	0011	TDC		Event ID			TDC Word count		
Test data *	1100	Shifted 1's							
B-Timizer trailer	1101	B-T ID (3-0)		Event ID (12bits)			Error flags	B-T ID(11-4)	
Errors	1001	B-T ID (3-0)		Error Flags					

* If enabled in JTAG command register (TestID /= 0)

6.2 Test Record example

Below an example of a test data record is given. The TestID in the Command register determines the amount of test data. The word count in the B-Timizer Header does not count the Errors word.

Description	Bit 31 - 28	Bit 27 - 24	Bit 23 - 20	Bit 19 - 16	Bit 15 - 12	Bit 11 - 8	Bit 7 - 4	Bit 3 - 0
B-Timizer header	1010	B-T ID[3-0]	Event ID (12bits)			Error flags	Word count	
Test data	1100	Shifted 1's						
More Test data	1100	Shifted 1's						
B-Timizer trailer	1101	B-T ID[3-0]	Event ID			Error flags	B-T ID[11-4]	
Errors	1001	B-T ID[3-0]	Error Flags					

7. Connector pinout

Output connector J1 (25p D-type male)

Pin	Signal	In/Out	Pin	Signal	In/Out
1	Clock(+)	In	14	Clock(-)	In
2	L0(+)	In	15	L0(-)	In
3	L1/Reset(+)	In	16	L1/Reset(-)	In
4	Data(+)	Out	17	Data(-)	Out
5	Strobe(+)	Out	18	Strobe(-)	Out
6	TCK(+)	In	19	TCK(-)	In
7	TMS(+)	In	20	TMS(-)	In
8	TDI(+)	In	21	TDI(-)	In
9	TDO(+)	Out	22	TDO(-)	Out
10	GND	In	23	+ 5 V	In
11	GND	In	24	+ 5 V	In
12	GND	In	25	+ 5 V	In
13	GND	In			

Input connector J2 (64p CMC connector male)

Pin	Signal	Pin	Signal
1	NC	2	Hit0(+)
3	NC	4	Hit0(-)
5	GND	6	Hit1(+)
7	GND	8	Hit1(-)
9	GND	10	Hit2(+)
11	GND	12	Hit2(-)
13	GND	14	Hit3(+)
15	GND	16	Hit3(-)
17	2V5	18	Hit4(+)
19	2V5	20	Hit4(-)
21	2V5	22	Hit5(+)
23	2V5	24	Hit5(-)

25	2V5	26	Hit6(+)
27	2V5	28	Hit6(-)
29	2V5	30	Hit7(+)
31	2V5	32	Hit7(-)
33	GND	34	Hit8(+)
35	GND	36	Hit8(-)
37	3V3	38	Hit9(+)
39	3V3	40	Hit9(-)
41	3V3	42	Hit10(+)
43	3V3	44	Hit10(-)
45	3V3	46	Hit11(+)
47	3V3	48	Hit11(-)
49	3V3	50	Hit12(+)
51	GND	52	Hit12(-)
53	GND	54	Hit13(+)
55	5V	56	Hit13(-)
57	5V	58	Hit14(+)
59	5V	60	Hit14(-)
61	5V	62	Hit15(+)
63	5V	64	Hit15(-)

Input connector J3 (64p CMC connector male)

Pin	Signal	Pin	Signal
1	5V	2	Hit16(+)
3	5V	4	Hit16(-)
5	5V	6	Hit17(+)
7	5V	8	Hit17(-)
9	5V	10	Hit18(+)
11	GND	12	Hit18(-)
13	GND	14	Hit19(+)
15	3V3	16	Hit19(-)
17	3V3	18	Hit20(+)
19	3V3	20	Hit20(-)
21	3V3	22	Hit21(+)
23	3V3	24	Hit21(-)
25	3V3	26	Hit22(+)
27	3V3	28	Hit22(-)
29	GND	30	Hit23(+)
31	GND	32	Hit23(-)
33	2V5	34	Hit24(+)
35	2V5	36	Hit24(-)
37	2V5	38	Hit25(+)
39	2V5	40	Hit25(-)
41	2V5	42	Hit26(+)
43	2V5	44	Hit26(-)
45	2V5	46	Hit27(+)
47	2V5	48	Hit27(-)
49	GND	50	Hit28(+)
51	GND	52	Hit28(-)

53	GND	54	Hit29(+)
55	GND	56	Hit29(-)
57	GND	58	Hit30(+)
59	GND	60	Hit30(-)
61	NC	62	Hit31(+)
63	NC	64	Hit31(-)

Test connector

Pin	Signal
1	GND
2	JTAG
3	Memory write
4	GND
5	Memory read
6	Error
7	GND
8	Test 4
9	Test 5
10	GND
11	Test 6
12	Test 7

8. Abbreviations

Abbreviations and other less well known definitions used in this document.

FPGA	Field Programmable Gate Array.
ASDBLR	Amplifier, Shaper, Discriminator, Base Line Restorer.
ZBT SRAM	Zero Bus Turnaround Synchronous Random Access Memory.
JTAG	Joint Test Action Group IEEE 1149.1. Functional test and programming facility.
LVDS	Low Voltage Differential Signaling. ± 400 mV. Compatible with 3V and 5V supply voltages.
B-Timizer	LHCb Time digitizer

9. References

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