

MROD-0 : MROD design study and demonstrator

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NIKHEF, November 10, 1999

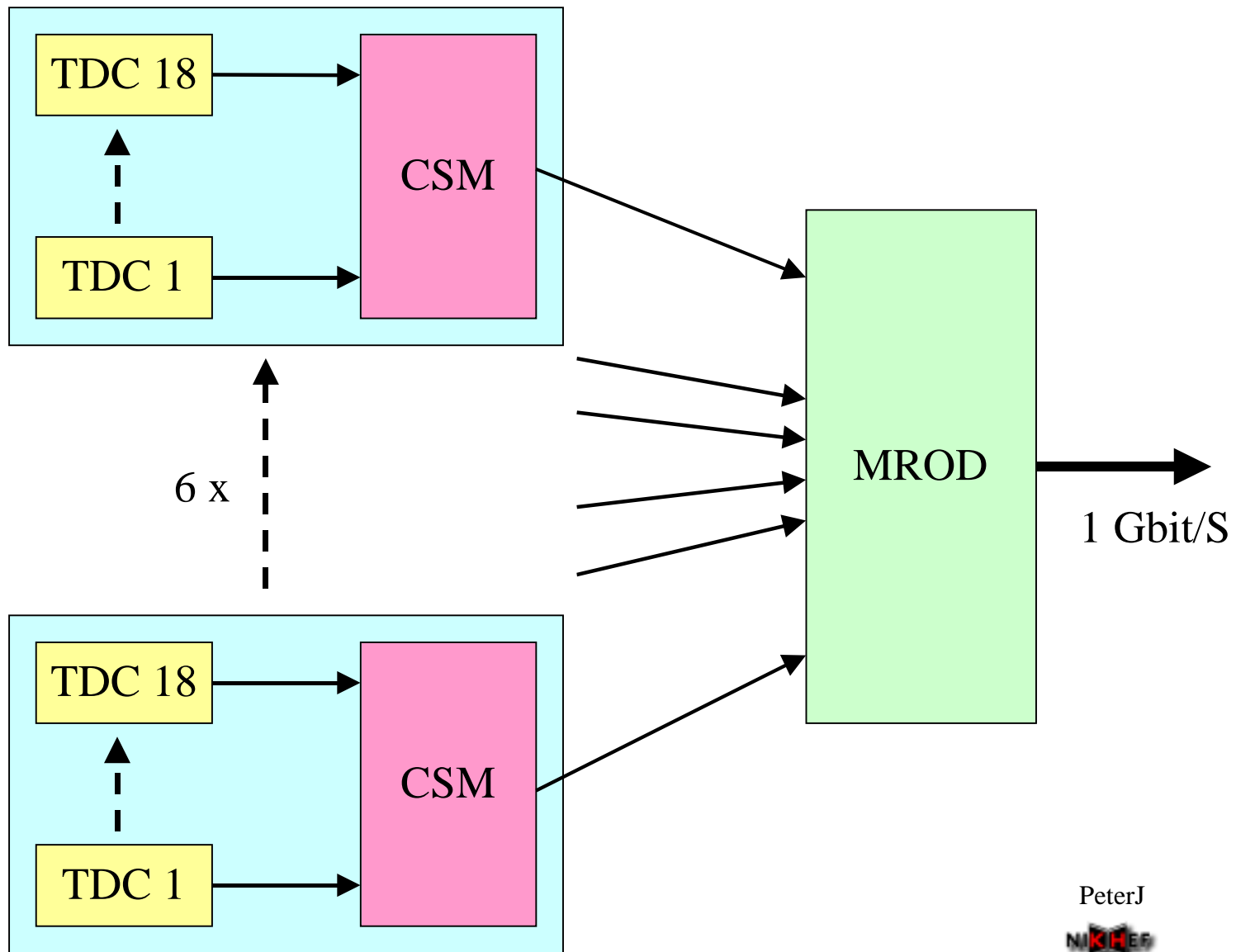
Reminder :

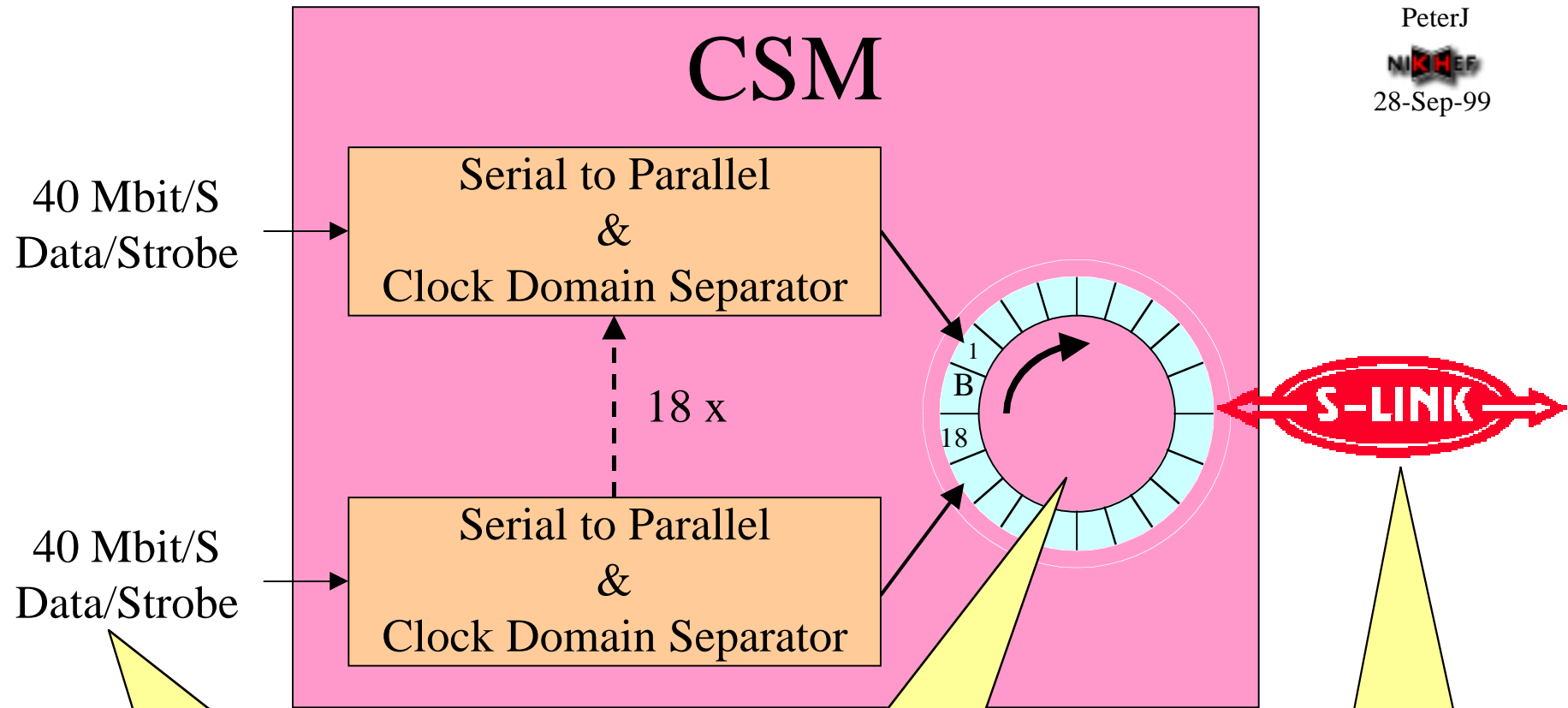
M-CRUSH : **existing** CRUSH (ROBIn) hardware, but with reprogrammed FPGA.

Goal : learn about unforeseen difficulties and achieve knowledge required for finding a good compromise between minimization of cost and functionality / flexibility.

Use ShaSLINK for output to S-link AND as programmable data generator for S-link input of M-CRUSH

System organization





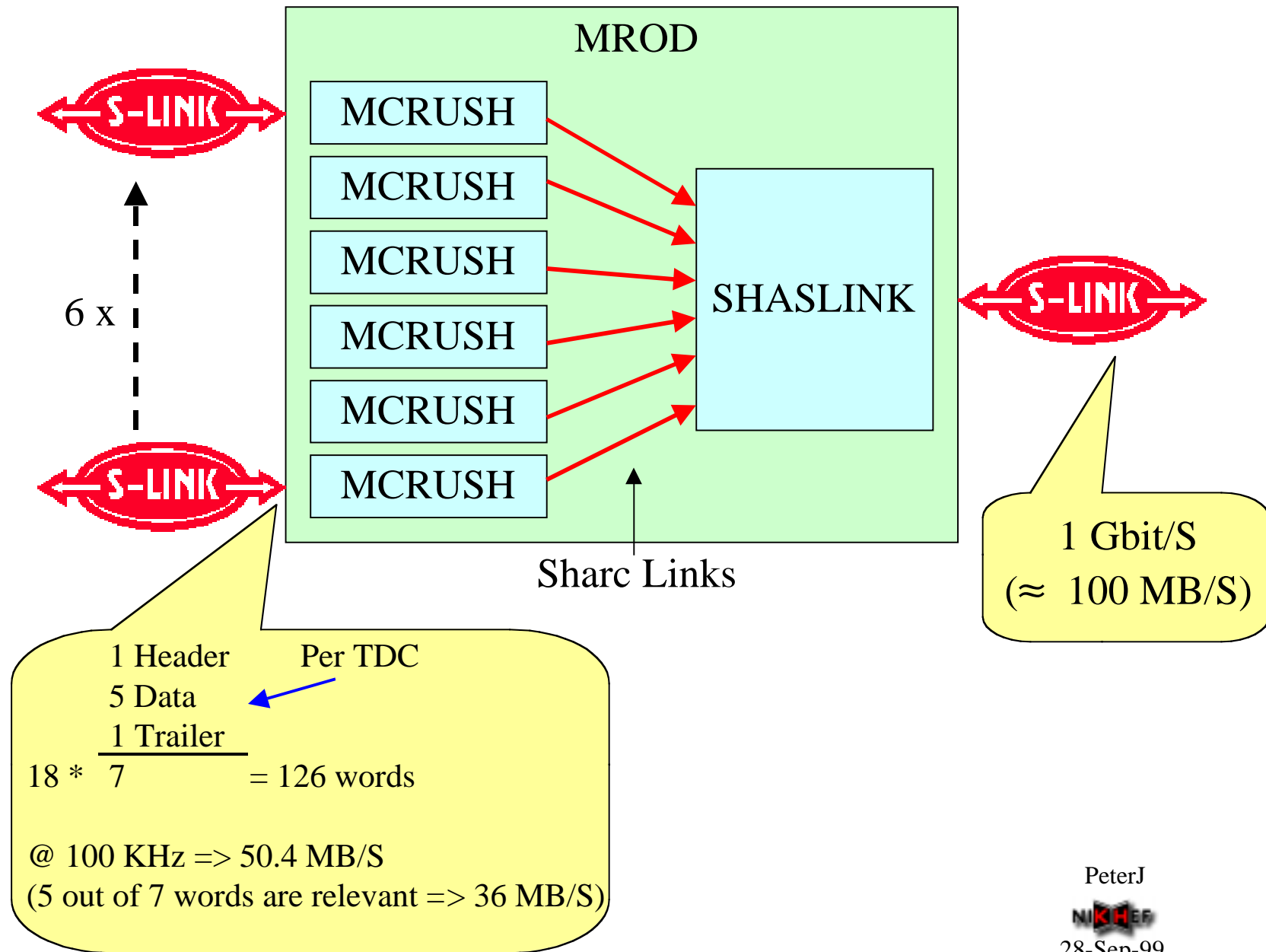
1 Start
 32 Data
 1 Parity
 1 Stop

 35 bits @ 25 ns = 875 ns

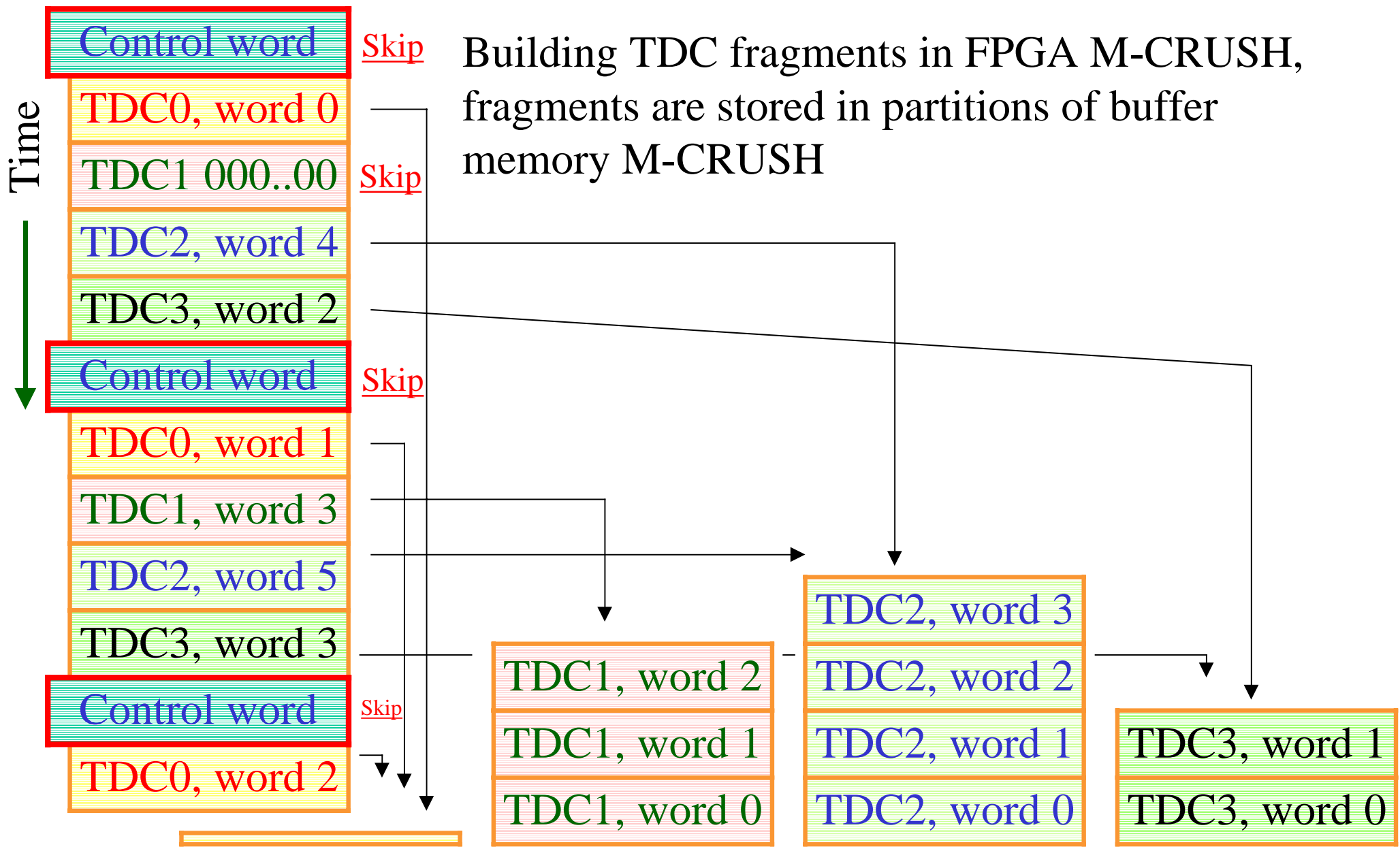
1 Separator (B)
 18 TDC data

 19 words @ 25 ns = 475 ns

19 words in 875 ns is sufficient
 (= 86.8 MB/S)



Building TDC fragments in FPGA M-CRUSH, fragments are stored in partitions of buffer memory M-CRUSH



Position in sequence determines TDC id, can check against TDC id in data

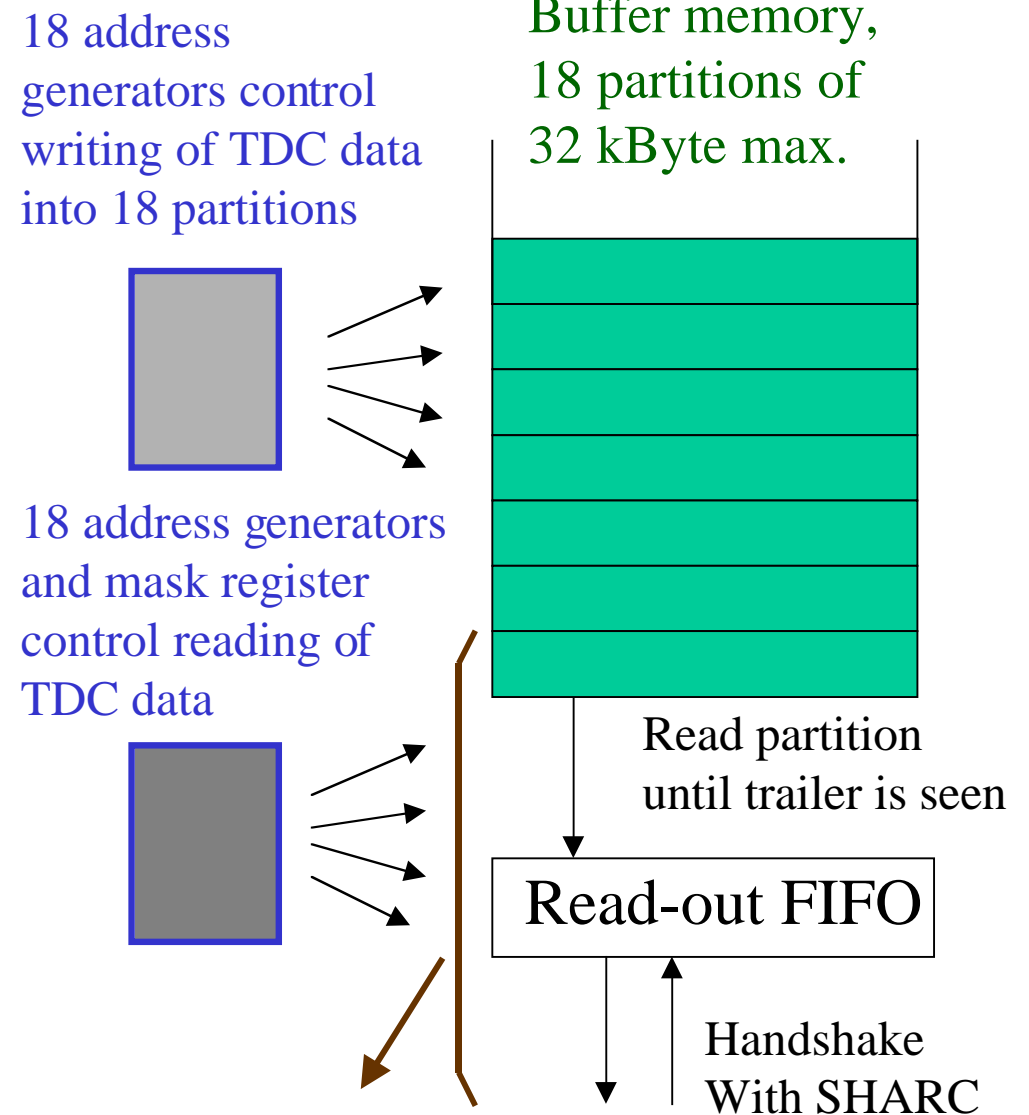
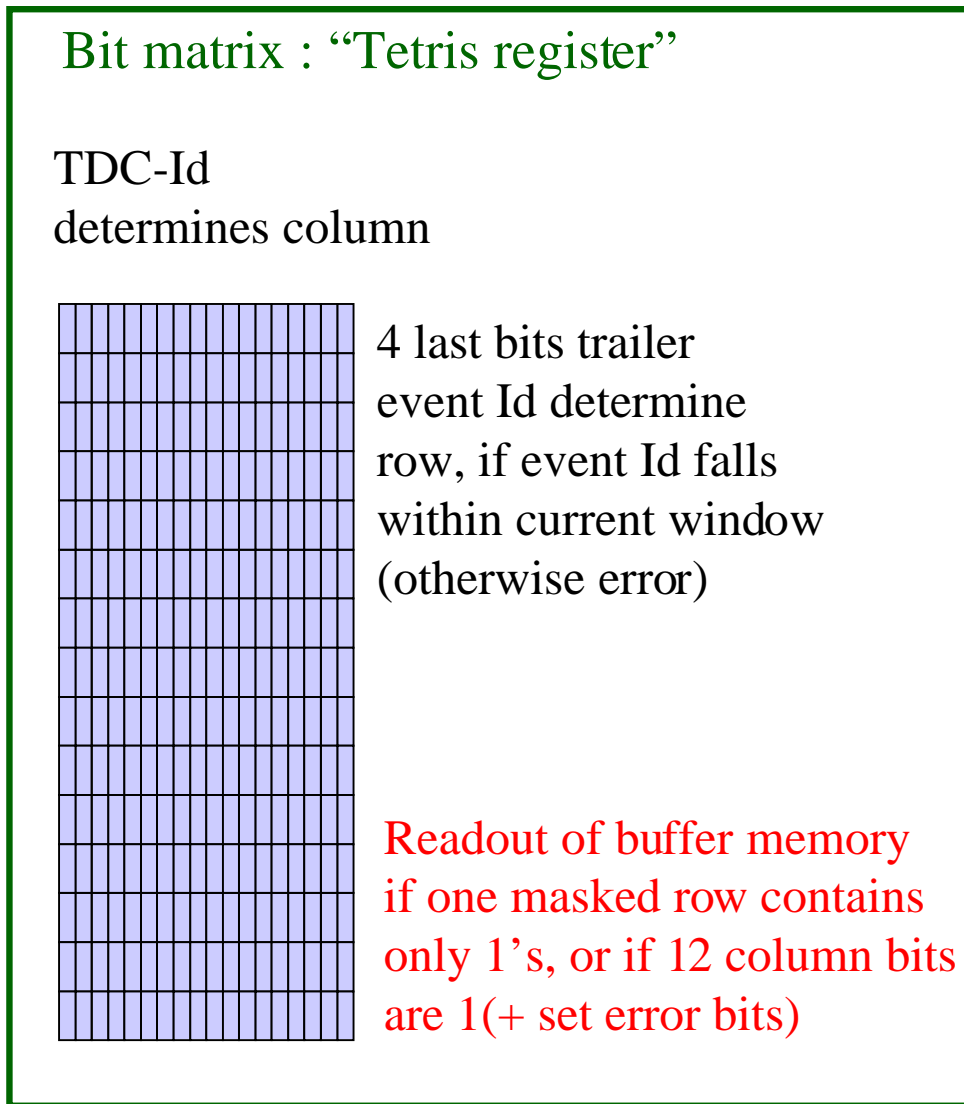
NB : Control words could be used to send TDC parity bits

M-CRUSH readout organisation (1)

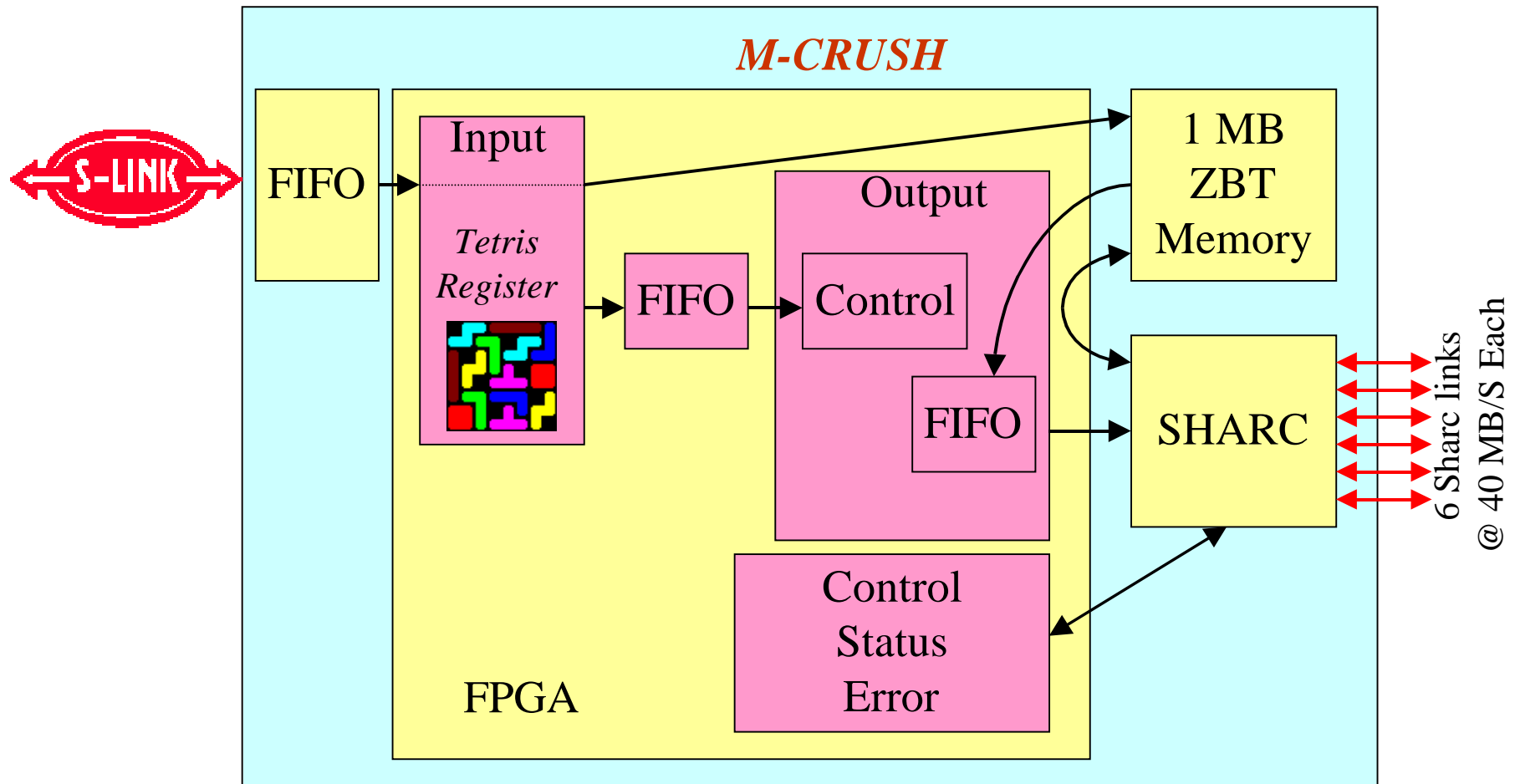
- All incoming data are stored in the buffer memory, trailer id's control setting of bits in "Tetris register"
- Normal operation : readout of data out of buffer memory only when all trailers have been seen, in that case all data is available in the buffer memory
- Errors that can disturb operation :
 1. corruption of trailer words,
 2. > 12 difference in event Id's : unlikely (simulation study)

Both cases are handled by incomplete readout. Data not readout for a certain TDC may be read out later together with data from later event fragments (signalled with error bits), when read-out for a later event id is signalled by Tetris register. Reading out of data of each individual TDC can be shut off under control of the SHARC. *The SHARC can also stop the complete read-out and then has random-access to the buffer memory for error checking.*

M-CRUSH readout organisation (2)



Max. transfer speed : 80 MByte/s

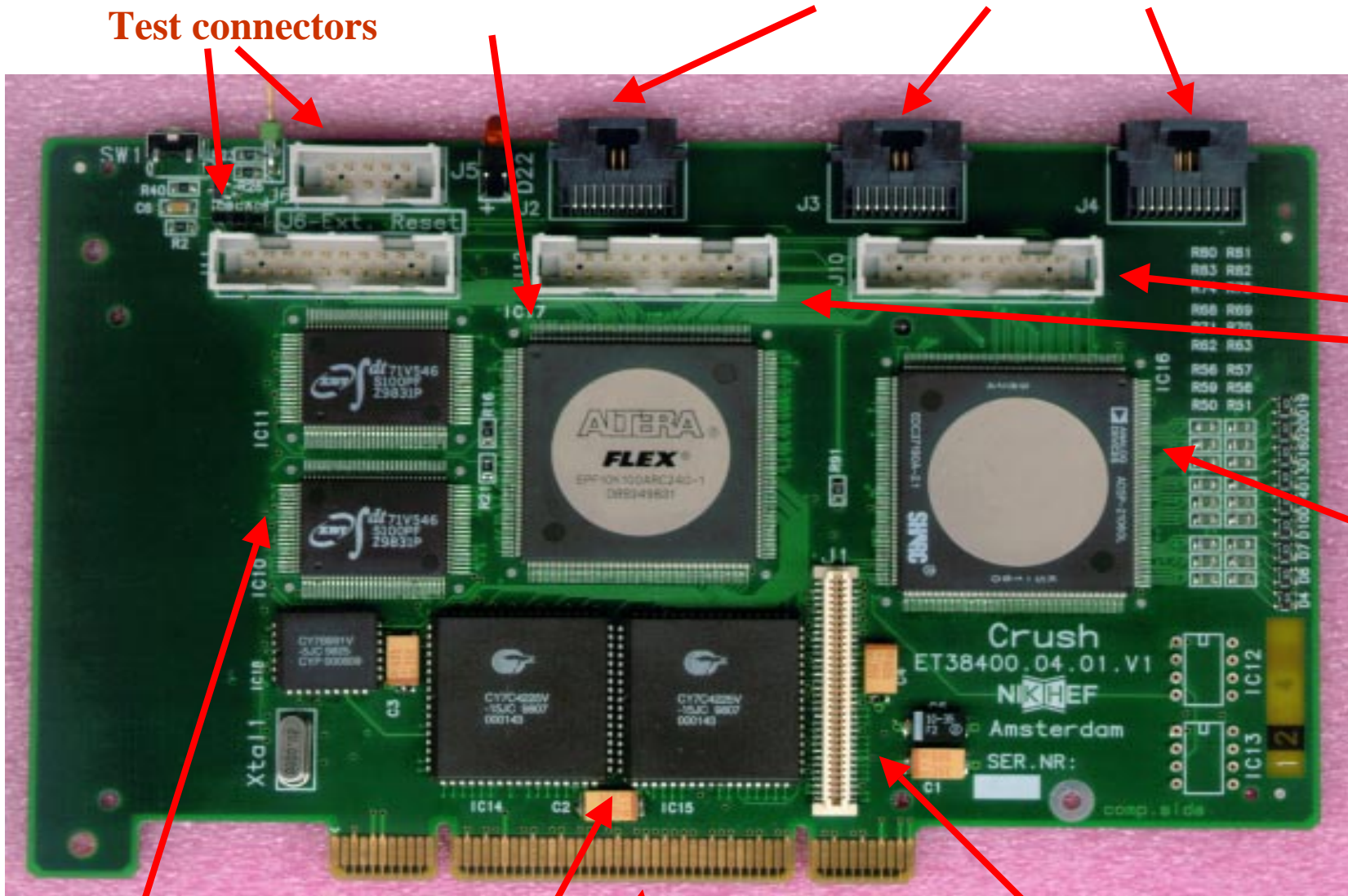


First tests with reprogrammed FPGA @ 37 MHz with full functionality (Tetris register 8 deep) successful. "Program" FPGA has to be modified somewhat, so that event headers (with bits of Tetris register) are inserted in the outputdata stream.

PeterJ

 28-Sep-99

CRUSH / M-CRUSH FPGA



Test connectors

Connectors for 6 SHARC links

Test connectors

SHARC

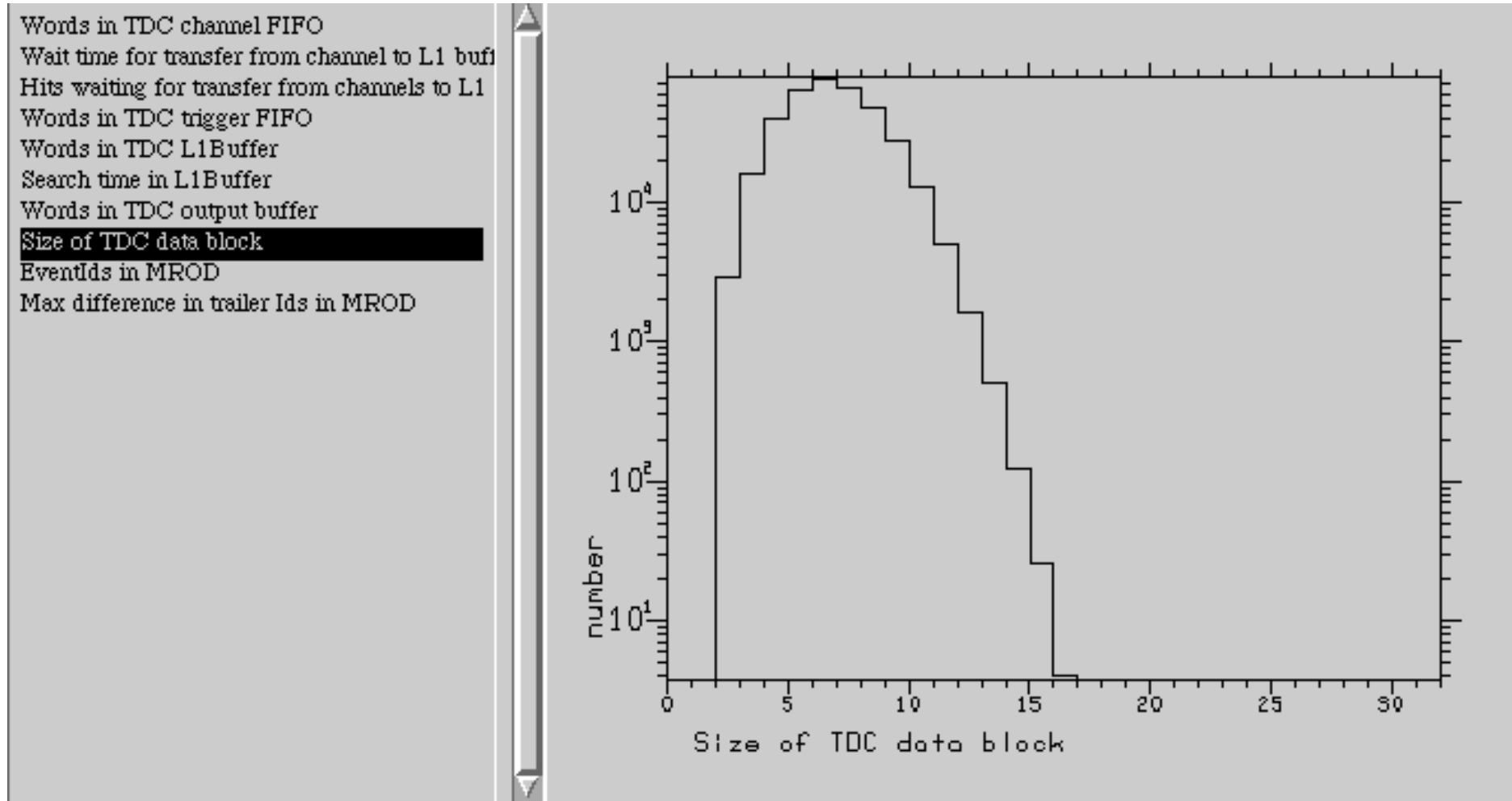
1 Mbyte ZBT RAM

FIFO

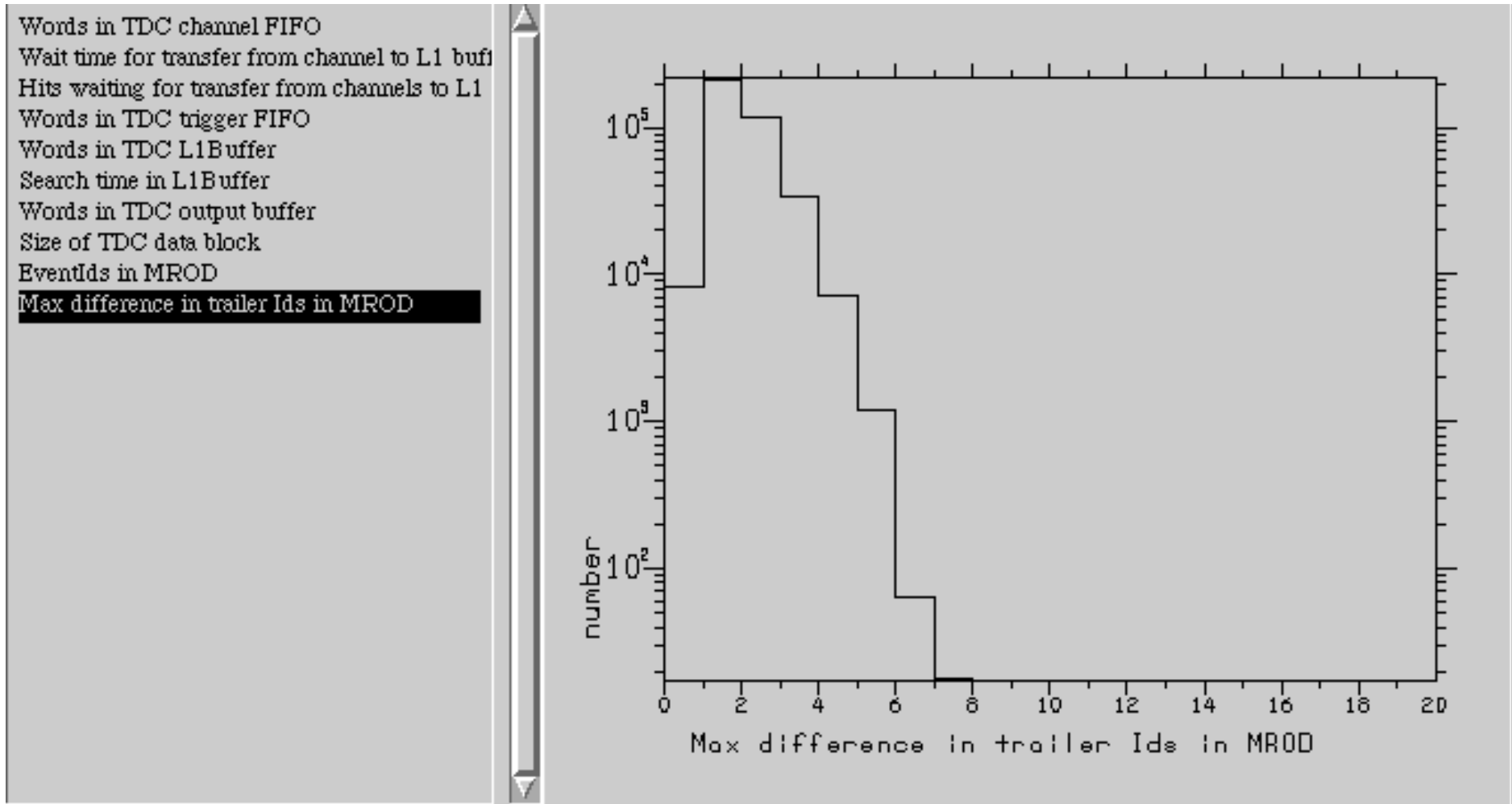
Connector for S-link daughterboard

PCI connector (only used for power)

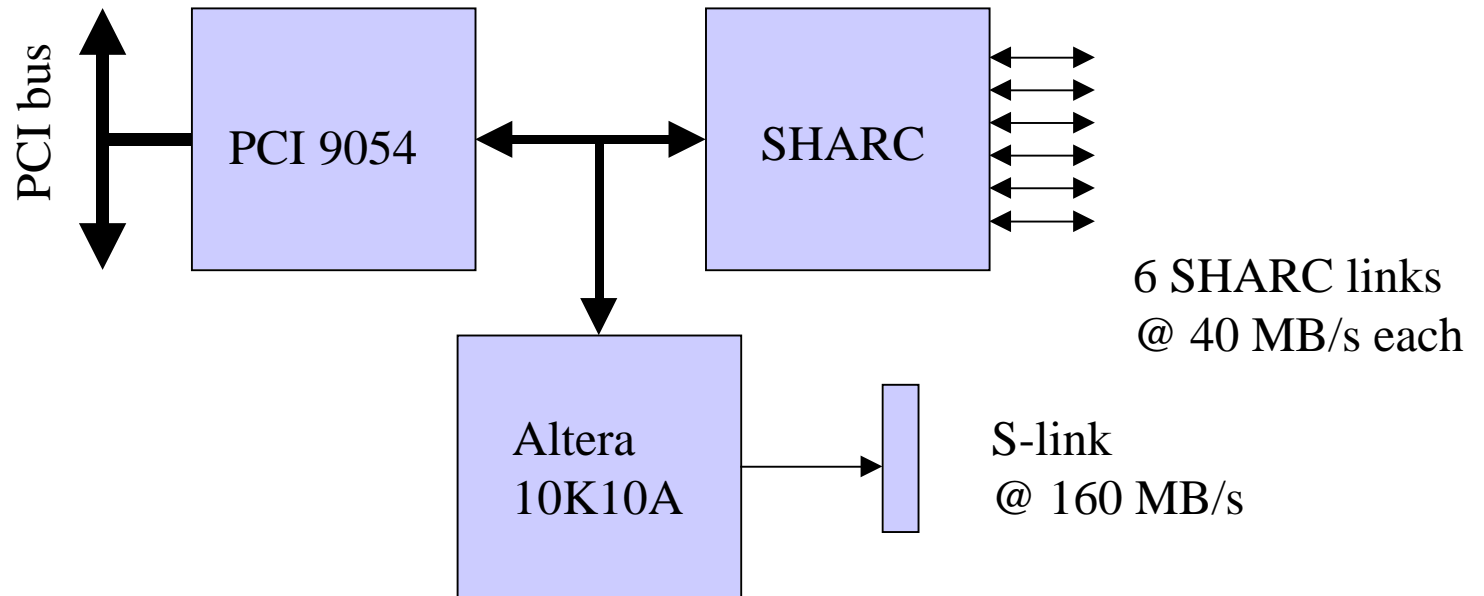
First simulation results : size of TDC data block



First simulation results : maximum difference in trailer Ids
(determines the required depth of the "Tetris register")



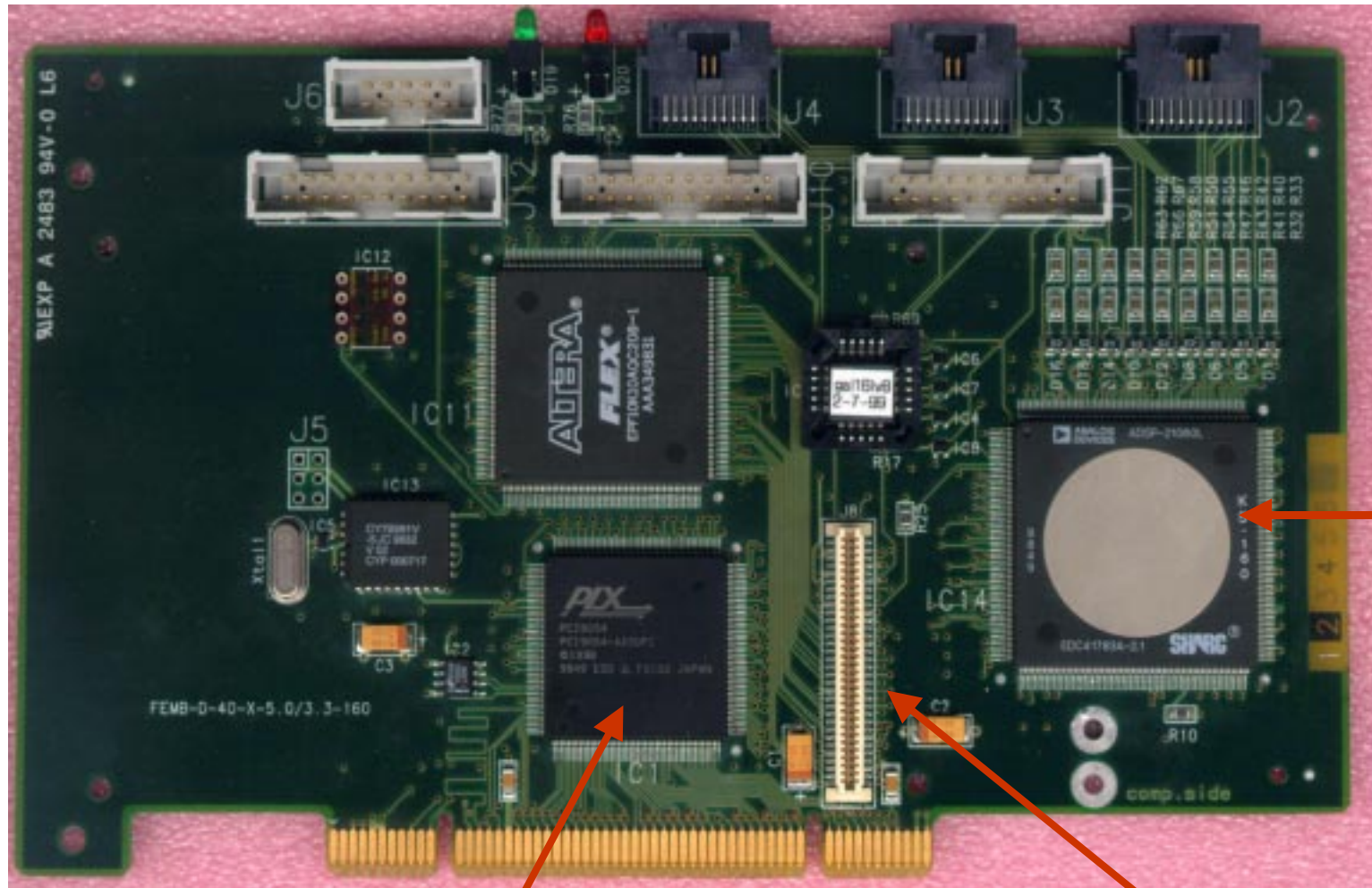
SHaSLINK



5 boards produced and tested, all fully functional, support software (library for SHARC + server program + driver for PC) also OK

ShaSlink

Connectors for 6 SHARC links



SHARC

Measured!

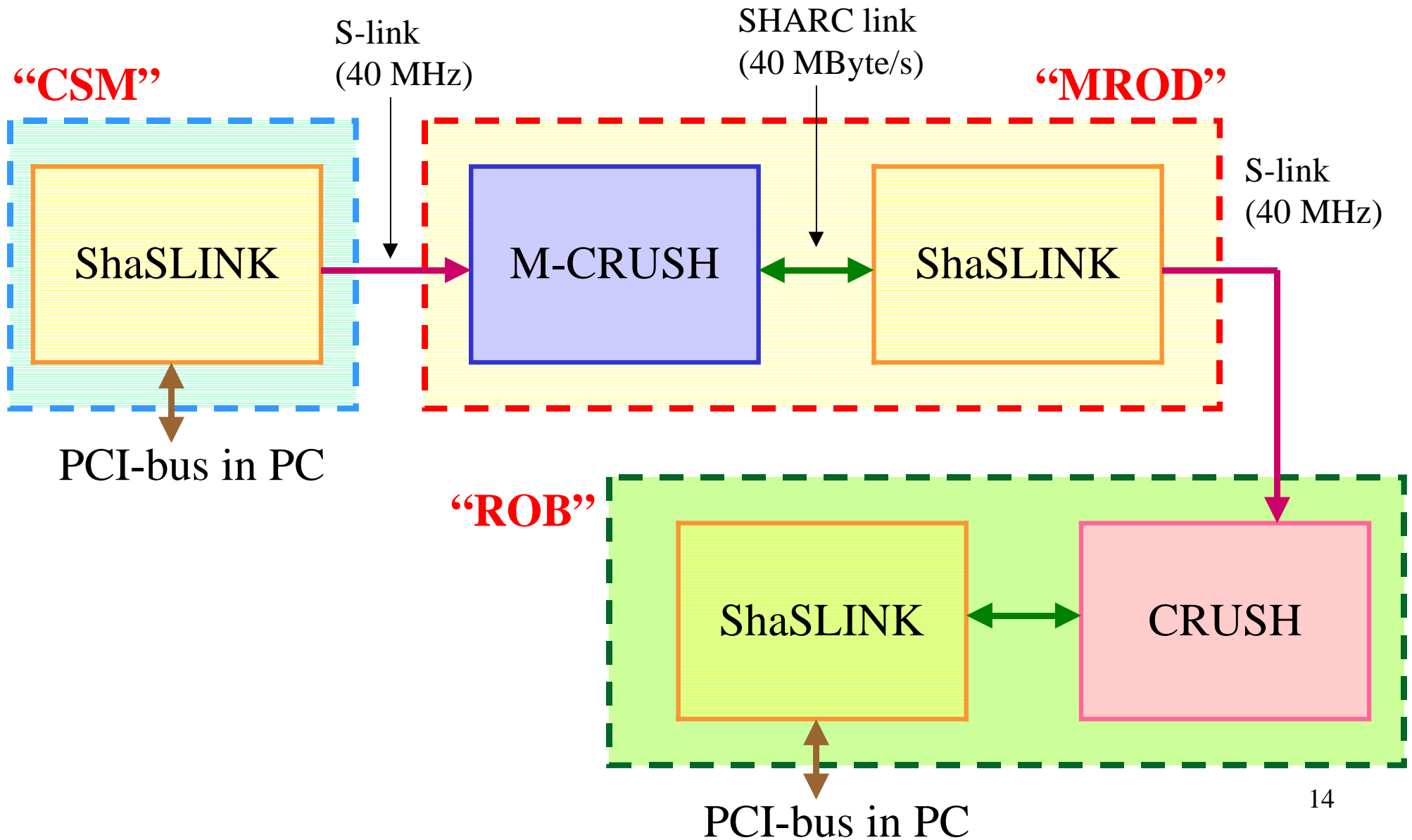
PCI interface (PLX 9054), supports full PCI bus speed transfers from SHARC memory

S-link connector for 160 MByte/s output S-link

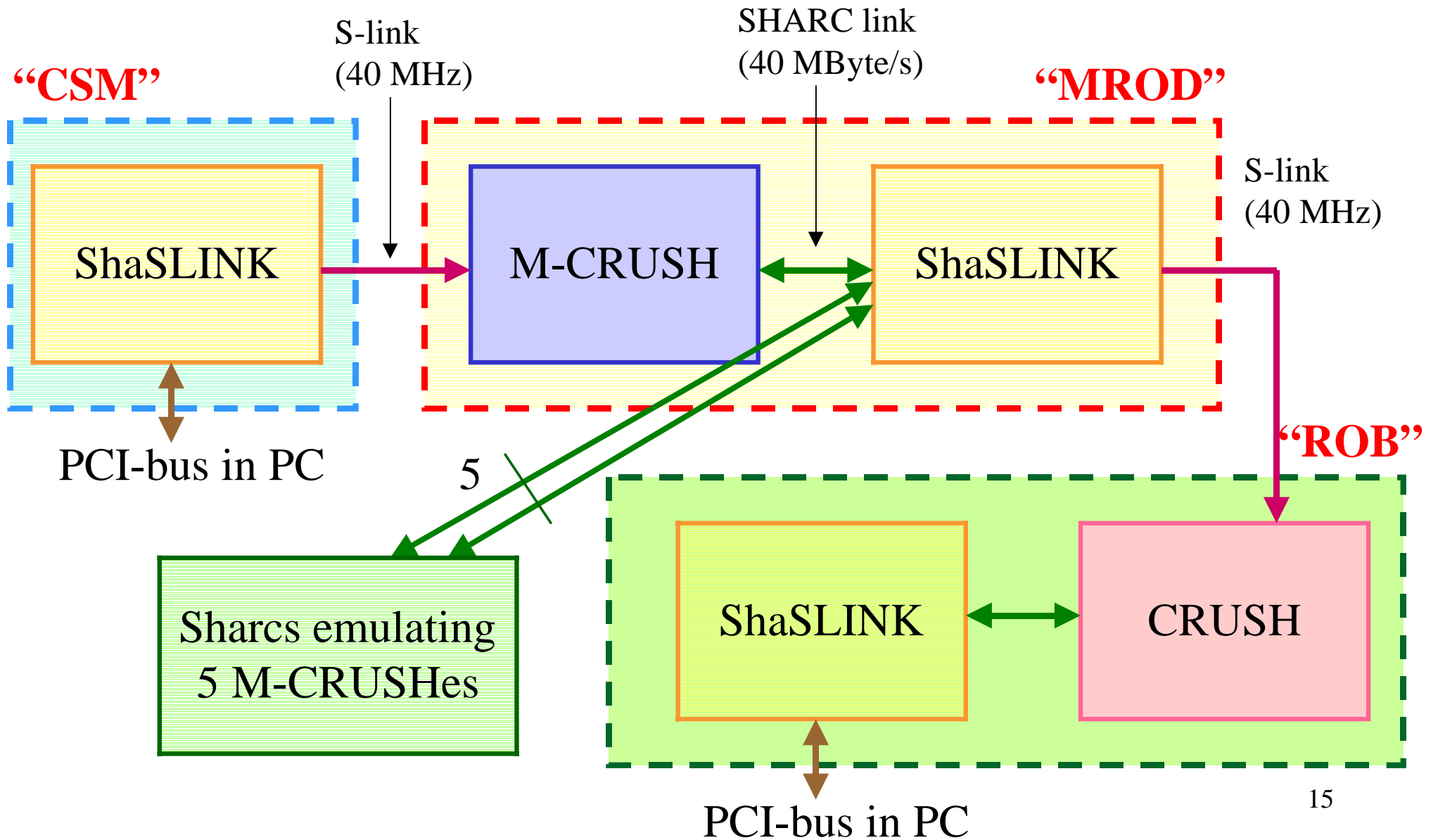
Measured!

NB : for data flowing through the SHARC (input via the SHARC links and output via S-link) the maximum throughput is 80 MByte/s due to an internal bandwidth limitation of the SHARC

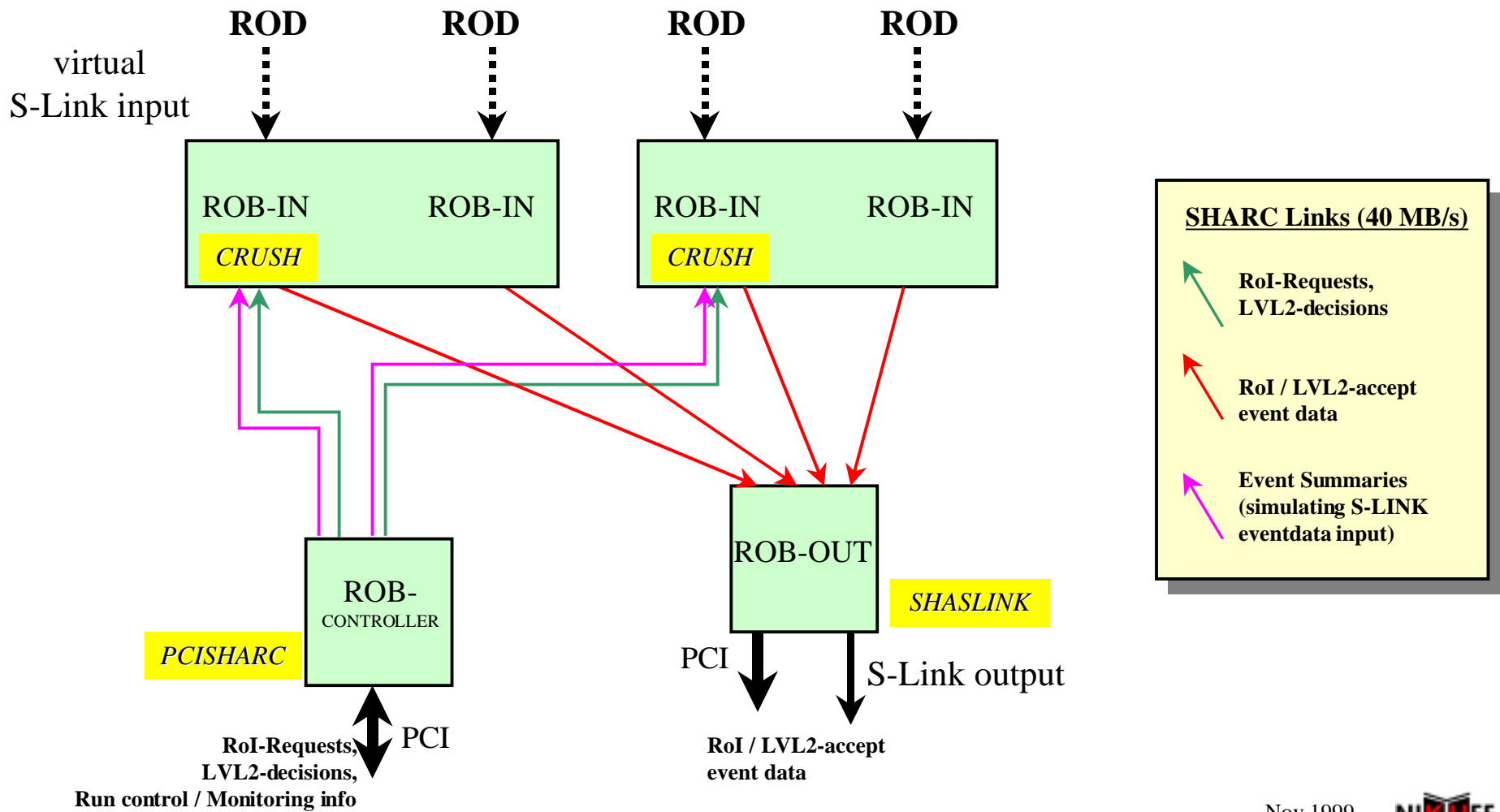
Test set-up MROD-0



Test set-up MROD-0, 6 input link test



ROB-Complex test : two CRUSHes simulating 4 ROBINSs, *similar to MROD test, fully functional*



Status MROD-0, 10 November 1999

M-CRUSH : first tests with reprogrammed FPGA @ 37 MHz*) with full functionality (Tetris register 8 deep) successful. "Program" FPGA has to be modified somewhat, so that event separators are inserted in the output data stream.

*) max. frequency 39 MHz, test at 37 MHz as there was no 39 MHz crystal immediately available)

SHASLINK operational, including Windows NT support. Internal bandwidth limitation of current SHARC limits throughput to 80 Mbyte/s.

Software for MROD-0 : simplification of ROBComplex software which is used for measurements now.

Error-tolerant scheme for fragment building in M-CRUSH found, simulations look fine.

High-level simulation in C++ of TDCs - CSM - MROD system : first version available, checking against available results of VHDL simulation of TDCs