SCI Concentrator & Distributor Systems

Idea to use B-Link standard of Dolphin as a direct connection to nodes (ROBs, Processors etc.)

Objectives

- MultiROB - possibly based on existing RHUL rob with PCI adaptors, but much better to make a new BLink ROB daughtercard
- Some ROB functions to be centralised ?
- Build in LVDS S-Link onto daughterboard, connect via carrier ??
- Farm/SFI studies
- Cross bar switch studies
- Second generation DataSource for SCI studies
- Option for a very simple ROB module with commercial processor control via BLink
- TBD...

BLink

- 64 bit multiplexed bus (TTL, GTL, etc)
- Fully synchronous
- Large bandwidth, currently up to 800MB/sec
- Split Response (write only, no read hangup)
- Supports full SCI protocol + user extensions
- User friendly - easy to interface to

Advantages of using BLink to connect nodes

- Cost - several nodes can share a link controller (but the price of link controllers is likely to be low)
- Avoids extra complexity/bottleneck/cost of PCI (but PCI bandwidth is sufficient in most cases, and costs of PCI bridge will go down)
- Broadcast
- Achieves Atlas densities
- Ring failure tolerant (multiple links per BLink)

Need full discussion in SCI group to produce exact specification.
Expect Manchester to produce the Carrier board.
Expect Manchester and RHUL to produce the ROB/Processor module
Spec complete end 97. Carrier to be ready mid 98. Modules for Q4 98.
The "obvious" solution to incorporating ROBs into an otherwise commercial SCI system is to use the Royal Holloway ROBin module and a PCI-SCI adaptor. These could be PMCs (eg on a RIO) or PCI cards, in a workstation or PC.

The PSB chip is an asic bridge between PCI and BLink, which is the back end bus of the Link Controller chips (The interface chips to the SCI network).

Since both the local bus and the BLink have a large bandwidth, we can consider removing the PCI, and interfacing the buffer memory directly to SCI. The additional "crate" traffic from outside (through the host PCI) can now be carried on SCI.

Because of the large bandwidth (BLink runs at up to 800MBytes/sec in current implementations) we can handle several ROB modules on a single bus. We can also remove some of management functions from the ROB module, as there is sufficient bandwidth to allow centralised management of the ROBs, via SCI and BLink. In this way the ROB processor could be a commercial processor board.
Example of Implementation of Carrier

- 4 BLink busses

- Each bus has two "ROB like" sites, and two "Link like" sites

- Two 16 bit LVDS links to each site (plus associated lines)
  LVDS busses could carry PECL.

- Large sites could be "double headed" so that we can accommodate two full ROBin modules, or up to five minimal ROBs on each BLLink bus

- Control processor off board (linked by SCI) - Commercial soln ??
Minimal ROB Module

- No local processing - slave module
- Data input via LVDS SLINK through Motherboard
- SLINK header for other connections (but => PMC size)
- Logic implemented in Xilinx(s?) with FIFO / SRAM built in
- Broadcast control ??