ROBIN

Functional demonstrator of the ATLAS Trigger / DAQ

Read-Out Buffer

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Basic principles

Data flow: output < input including L2 and L3 according to strategy from few % to ~20 %

optimisation between Input buffering and Output data request (e.g. Calorimeter vs muons)

sequential processing: increase requests decrease data

C architecture: mix control, requests and data try to reduce number of links to switch

Group several Inputs on one Output
Conceptual Architecture

One buffer per input link
Input rate = 1 Gbit/s
large and fast memory with intermediate Fifo

Local fast data collector
PCI bus

Local intelligence
decode requests
prepare data transmission
preprocessing if necessary

Bi-directionnal downstream link
receive requests
send RoI data fragment (L2)
Event data (Filter)

1 Gbit/s
PCI

132 MByte/s
Local Intelligence
Downstream Link
Today Implementation

ROB backbone

PCI on VME board

Local Intelligence

CPU on board

Inputs & buffers

PMC boards

Output

ATM Port on PMC

Some limitations Port number Power

Possibility to extend PCI port number with extension boards

CES - RIO2

DRAM

VME Bridge

PPC 604

PCIBridge

DRAM

Network Port

PCI Bridge

Ethernet

PMC#1

PMC#2

ROBin

Data generator

FIFO

Main Buffer

PCI bridge

CPU Memory

TTC & L1 Interface

Logic

Input data port

serial ROL

serial to parallel

serial ROL

Possibility to extend PCI port number with extension boards
Implementation -> Next step
CompactPCI based

ROB backbone
  Crate
Local Intelligence
  CPU board  (Ex : RIOC)

Inputs & buffers
  ROBin boards

Output
  ATM Port
  possibility to adapt PMCs in Compact PCI
  up to 8 slots without additionnal bridge

To be purchased for end of 97
Short history of the project

1995  C80 implementation investigated
      on commercial board  dual port VRAM memory
      2 CPU
      possibility to connect input ports on links
      drawback  very long delay  ~ 1.5 year
      more additional electronics than foreseen

1996  PCI available  ->  new approach
      Cracow (April)  concept presented
      Balaton (September)  pre design  (Balatonfüred September 23-27, 1996; p 204)

1997  Design
      Difficulties:
      PMC design  few board space
      CPU knowledge  low power
      VHDL description
      components supplying  very flat package
      small quantities
ROBin present design

PMC format

- Input Port: 32 bits //
- Event Buffer Fifo: 64 kB
- Event Memory & Event Buffer Control
- Event Memory: 4 MB
- Local Bus: 33Mhz
- J960JF: CPU
- PLX9080: Bridge
- Local Memory Control: 512KB
- FPGAs
- Local Memory: 512KB
- Bus Arbitration
- jtag
- not used: RP -> BGA, JD -> Power increase
- i960JF
- PLX9080
- eeprom
- PCI
- FPGA: type MACH on site programming with JTAG port (through PLX9080)
- bridge: circular message queue eeprom: on site programming

ATLAS T/DAQ Marseille October 1997
Two steps

Version 1

Local Memory
512KB

Local Memory Control

FPGAs

Event Memory & Event Buffer Control

Bus Arbitration

jtag

Version 2

Input Port

32 bits //

Event Buffer
Fifo
64 kB

Event Memory
4 MB

Local Bus
33Mhz

PMC format

PCI

CPU

i960JF

Bridge

PLX9080

eeprom

eeprom

Local Bus
33Mhz

1960JF

Control

Event Memory & Control

FPGAs

Version 1
Planning

Step 1

- **Schematics**: end of October
- **CAO**: components description started
  placement
- **board cabling**: foreseen during december

Step 2

foreseen 4/98

Present cost ~ 7000 FF few pieces
Estimated future cost ~ 5000 FF large series
Software tools

No OS and No communication port in ROBin

Local Monitor downloaded in SRAM delivered by intel for i960 family
Remote Monitor for Host connected to local monitor through PCI

Ctools compiler
linker

Board debugging on PMC carrier located in a PCI slot on PC

Remote Monitor to be translated on RIO-CES/LynxOS
In parallel, 2 boards have been purchased and are in use.

* PCI board with i960RP

* PMC board equipped with SHARC
i960 evaluation

PCI evaluation board with intel960

familiarize with:

intel tools
pci protocol

ROBin circular message queue for request transmission
ROBin DMA for data sending to Host

in PC environment

Cyclone IQ-SDK

i960RP
2 M DRAM
monitor in rom
DMA on both PCIs
ROBin emulation

PMC Transtech ASP-C2

emulate ROBin in Demonstrator
real data flow on PCI

Driver to be converted for LynxOS