The Rob-in Development Project

Who is involved?

– **RHUL**: Barry GREEN, Gary BOORMAN, John STRONG
– **UCL**: Gordon CRONE, Bob CRANFIELD
– **Edinburgh**: Owen BOYLE
– **CERN**: Robert McLAREN
– **consultants**: David Francis, Eric van der Bij
rationale

• idea from Robert McLaren - split ROB development for prototyping:

11/07/97 Rob-in Project (R.Cranfield/UCL)
history

• Project start ... ~Jun’96
• ROB-IN URD, Draft Spec ... Jun - Sep’96
• Paper researches ... Sep - Dec’96
• Processor choice ... Jan’97
• Design issues ... Nov’96 - Mar’97
• Hardware design ... Feb - Aug’97
• Hardware layout/review ... Sep’97
• Software design, test-environment ... Feb - Jun’97
basic strategy for ROB-IN

• Start with URD (from ROB URD)
• base on existing T2B
• modify to fit current prototype “standards”:
  – add S-LINK to front-end
  – use PCI-bus comms
  – use PMC format (to integrate with e.g. RIO2)
new components

• opportunity to reconsider component choice:
  – use bigger Mach chip
  – use different processor (i960RP) - eventual criteria:
    • size limit
    • power limit
    • shorter development time (speed less important)
Hardware block diagram
ROB-IN block diagram using i960

- SLINK Connection
- Input fifo
- Double Buffer
- Data/Control
- Data
- HF
- XOFF
- LDERR#
- Control Logic
- Buffer Memory
- MUX
- Counter
- PAE Free Pages fifo
- PAE
- Status fifo
- Used Pages fifo
- Data Registers
- Status
- Control
- i960RP
- PCI bus
- Flash RAM
- Program RAM
- L1 Inhibit
- Address bus
- Data bus
software

- buffer manager in on-board processor
- polling-loop (no interrupts)
message-passing

- uses circular buffers (software FIFOs)
- polling (pointers checked)
- message passing library (Crone/Francis)
- event handling library (Crone/DAQ team):
  - get-event (id, location)
  - remove-event (id list)
  - monitor-event (id, location), ...
data transfer

• uses i960 DMA
• continuously operating DMA with dynamic extension of DMA chain
• header written last so receiver can check completion
• minimal use of PCI bus
• headers added by buffer-manager
development status

• 3 stages:
  – PCI (5V version)
  – PMC (5V version)
  – faster PCI (3.3V version)

• design review Sep-1997

• PCI in PCB manufacture/BGA mounting

• aim: PCI board end ‘97, PMC early ‘98
PCI board layout
software tests

- uses Intel i960RP evaluation kit + PC
- Intel code ported to Linux
applications

• DAQ Prototype “-1”
• Multi-ROB studies
• SCI studies
• Pilot project test-beds
• ???