RobIn design study - Mannheim

Status:
Use of commercial hardware only
- Intel PC
- microEnable
- S-Link

5 microEnables available at Mannheim, more on stock at Silicon Software corp. (aprox. 2500DM/pc.)

Tasks on microEnable:
- S-Link input, design available from Oct ’97 tests
- Buffer manager, ringbuffer version ready
- Preprocessing, TRT ready for implementation
  - PreProc at ROB output
  - PreProc at RobIn output

Performance:

<table>
<thead>
<tr>
<th>Event-size</th>
<th>Per ROB/RobIn: 15kHz, 10MB/s (Amsterdam)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 kB</td>
<td>Measurements: 14kHz, 14MB/s</td>
</tr>
<tr>
<td></td>
<td>Expected: 22kHz, 22MB/s</td>
</tr>
</tbody>
</table>

Current overhead 60µs per transfer => will drop to 30µs

Next steps:
- Integrate S-Link, Buffer manager, Preprocessing (-hook)
- API, conform with DAQ/EF and UCL
- Measure 4 RobIns/PCI-bus
  - coordinate with HPCN activity
  - try direct DMA from RobIns to PreProc or RobOut
- Add some monitoring

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ROB-IN
Inhalt

• Atlas DAQ
• ROB-IN Hardware
• FPGA Design
• Prozesse
• Buffermanagement
• Messungen und Erwartungen
Figure 1: The ATLAS three-level trigger architecture.

**EVENT RATES**
(@ 10^4 cm^2 s^-1)

40 Mhz
(20 events/b-c)

Level 1:
hardwired processors

10-100 kHz

Level 2:
local analysis

100-1000 Hz

**DATA RATES**
(@ 10^4 cm^2 s^-1)

event
~ 1.5 MB

1-10 GB/s

Readout Event building

MUX

Derandomizer

Multiplex, compress data

Digital buffer memories

Switch farm interface

Full-event buffers, processor farm

Data Storage

10-100 MB/s
μEnable
μEnable

RAM → FPGA

32

FPGA → S-LINK

32

Clock & Support

Local bus, 40 Mhz, 32 Bit

PCI - Interface

PCI, 33 Mhz, 32 Bit
FPGA design

PCI  ->  S-LINK  <-  out-bound

buffermanagement

in-bound

DP RAM
Out-bound process

PCI

EVENT

PAGE

lookup

address

request

DP RAM

Fragments

LUT
In-bound process

DP RAM

Empty Page

PAGE

EVENT

LUT

store

address

extract

S-LINK
Current implementation
Ringbuffer

- counter for next page
- simple
- nothing to do for ROB Controller
- no forgotten fragments
- all fragments have same lifetime
Outbound process
Inbound process
measured ROB-IN Output Rates

ROB-IN Output
ROB-IN Output Rates

- measured @ 20 MHz + 60 us overhead
- expected @ 20 MHz + 60 us
- expected @ 20 MHz + 30 us
- expected @ 33 MHz + 30 us
Current implementation

- 512 kB RAM, Xilinx 4028 @ 20 MHz
- 127 Pages a 4kB
- 4kB LUT
- 1,2 ms fragment-lifetime @ 100kHz
- max. fragmentsize 4kB
- Output Rate 33MB/s = 8,3 kHz