Compact ROB Using a SHARC (CRUSH)

No paging, cyclic memory

6 (40 MByte/s) SHARC links

S-link

SHARC receives for each event summary info:
start address in buffer memory + contents of 5 words,
addresses of these words relative to BOB and EOB can
be programmed, data pattern to be recognized as BOB and EOB
can also be programmed. Transfer of (FIFO buffered) summary
info to SHARC under DMA control with handshaking between
FPGA and SHARC (with DMA request and DMA grant lines)

Self test: SHARC can write data patterns to FPGA that follow
same route through system as data coming from the FIFO.
SHARC has also read-write access to buffer memory
CRUSH : Software study

Normal operation:
- via SHARC bus under DMA control

First result > 200 kHz for interrupt based handling of data, including (simple) "indexing"

CRUSH tester
(PCI SHARC card)

SummaryInfo

EventDataRequest

EventDataInput

AcceptReject

EventDataOutput

Simulated CRUSH
(PCI SHARC card)

Normal operation:
DMA controller initialisation

SendDataRequest