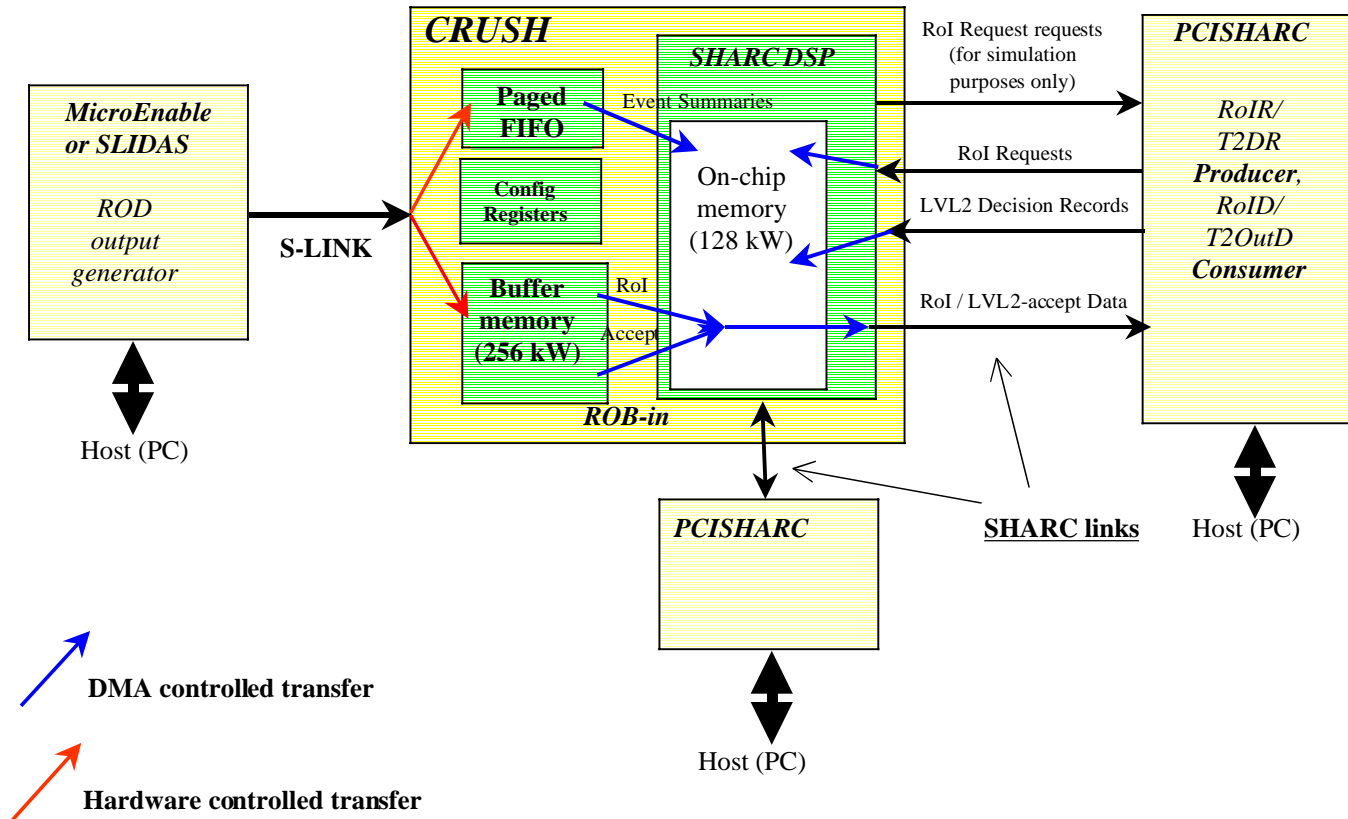
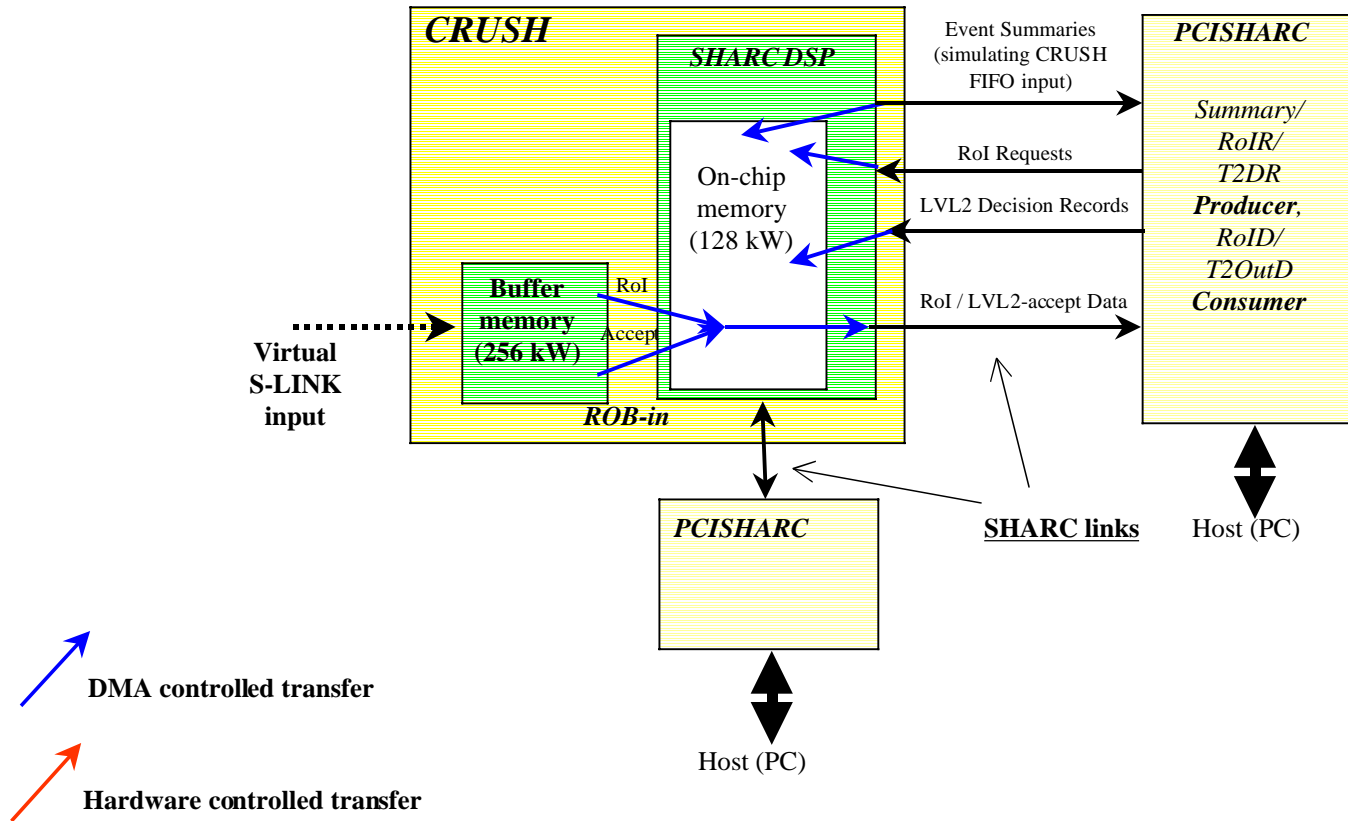


CRUSH ROB-IN performance test set-up (with real S-link input)



Event Summary: LVL1-ID, buffer address location,

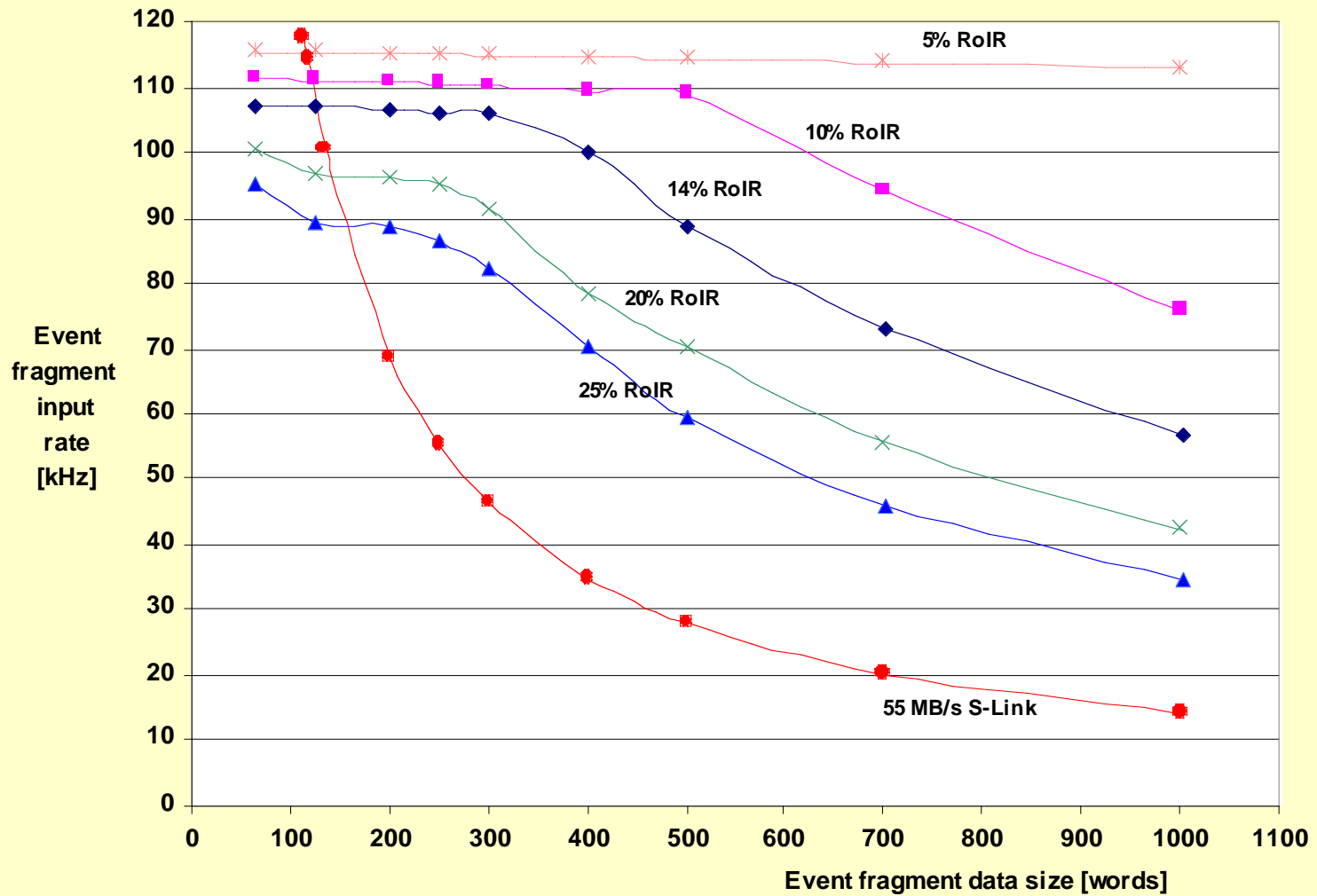
CRUSH ROB-IN performance test set-up (with simulated S-link input)



CRUSH ROB-IN software features

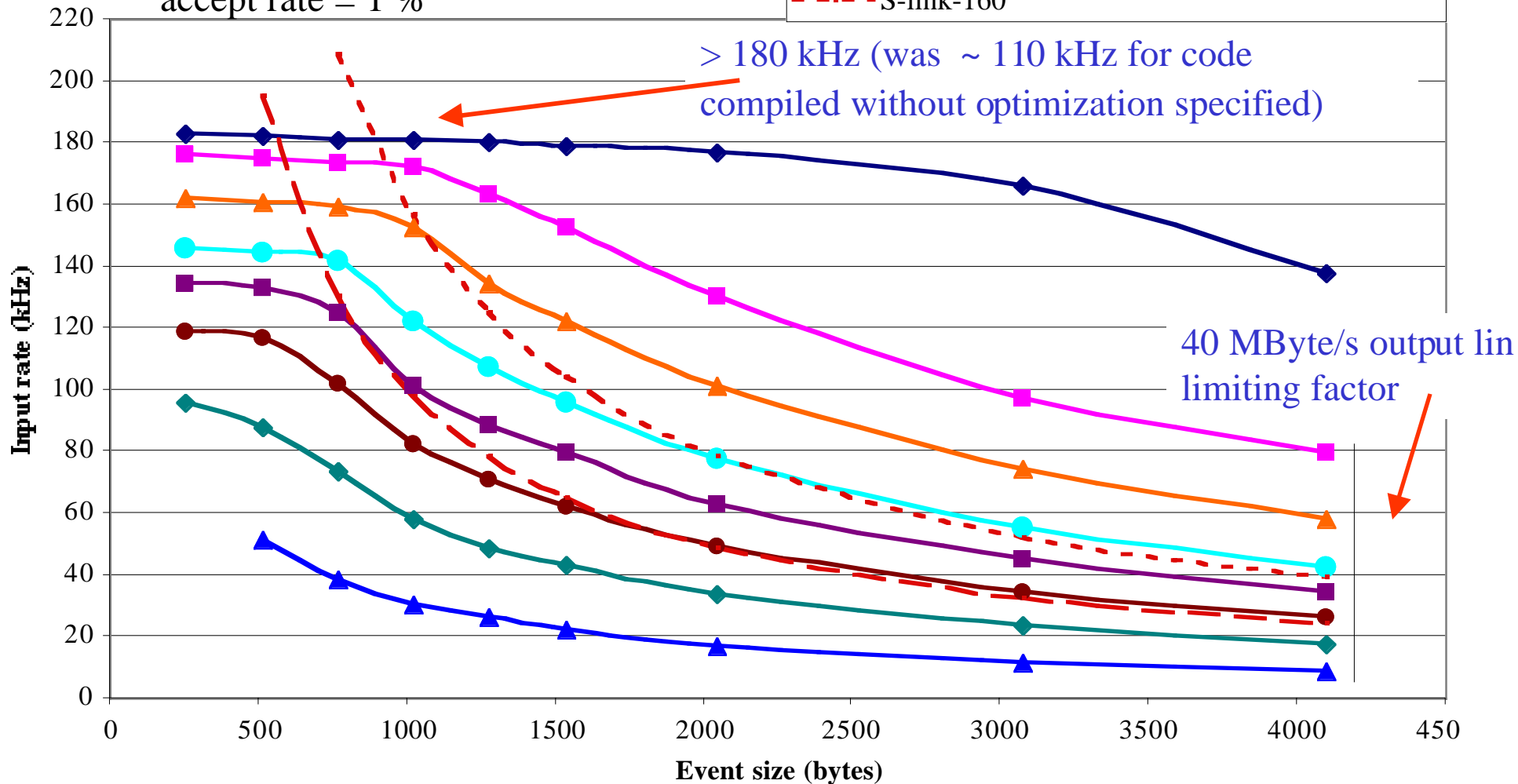
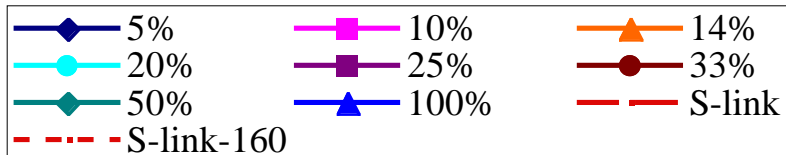
- ← SHARC I/O by **DMA** operations, concurrently with processing
- ← **I/O buffering** in SHARC on-chip memory
- ← **Event fragment** (summary) processing: ordered event fragment list
- ← **RoI-Request** processing: finding, formatting, sending event
- ← **LVL2 Decision Record** processing
 - § **RELEASE**: finding, releasing memory space
 - § **ACCEPT**: finding, formatting, sending event fragment
- ← Written in **C** using the Development Toolset for the SHARC processor

CRUSH ROB-IN performance results

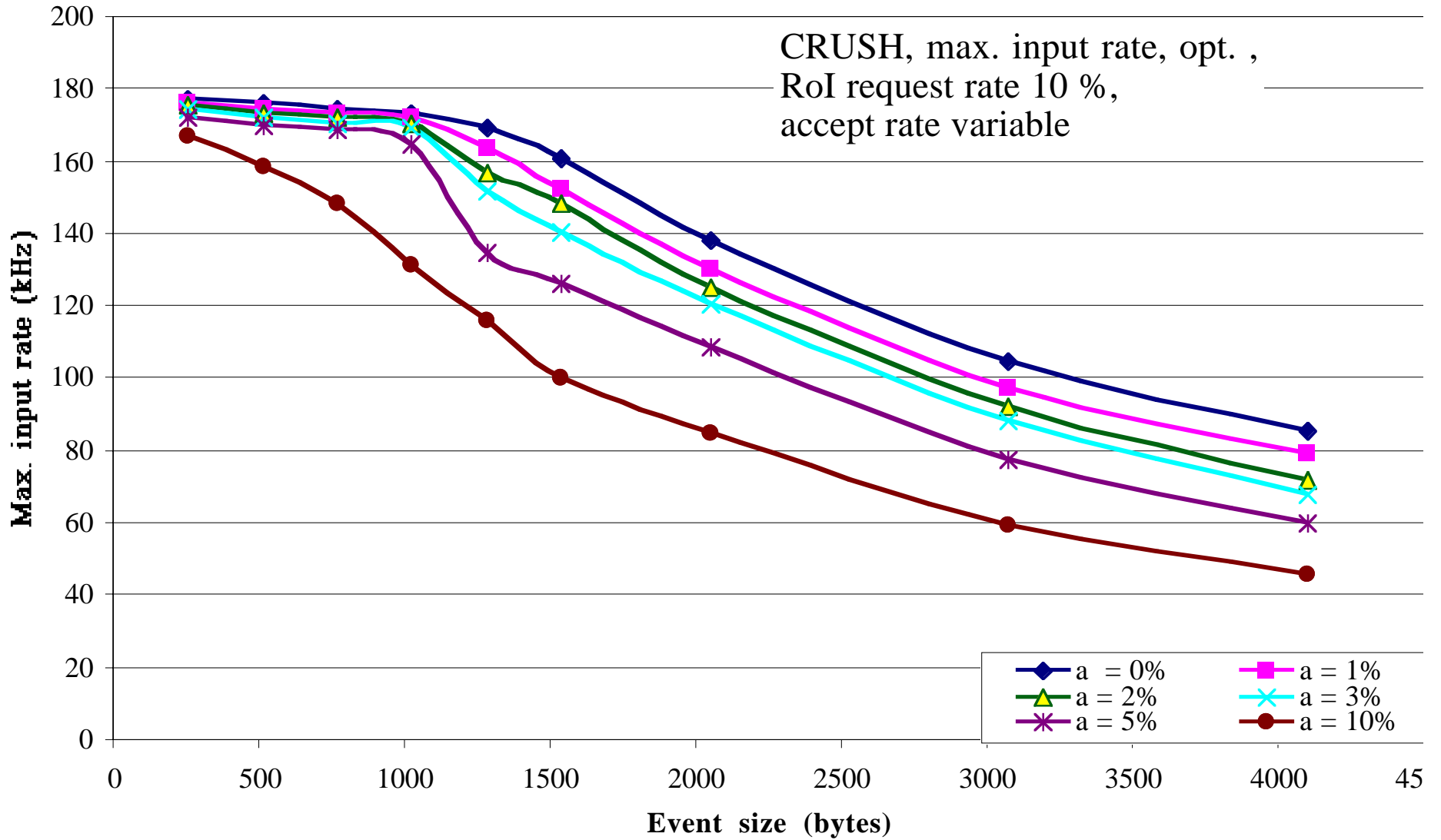


Processor load:
Event fragment processing: ca. 8 μ s/fragment
RoI-Request processing: ca. 9 μ s/RoIR

CRUSH max. input rate, opt. ,
variable RoI request rate,
accept rate = 1 %

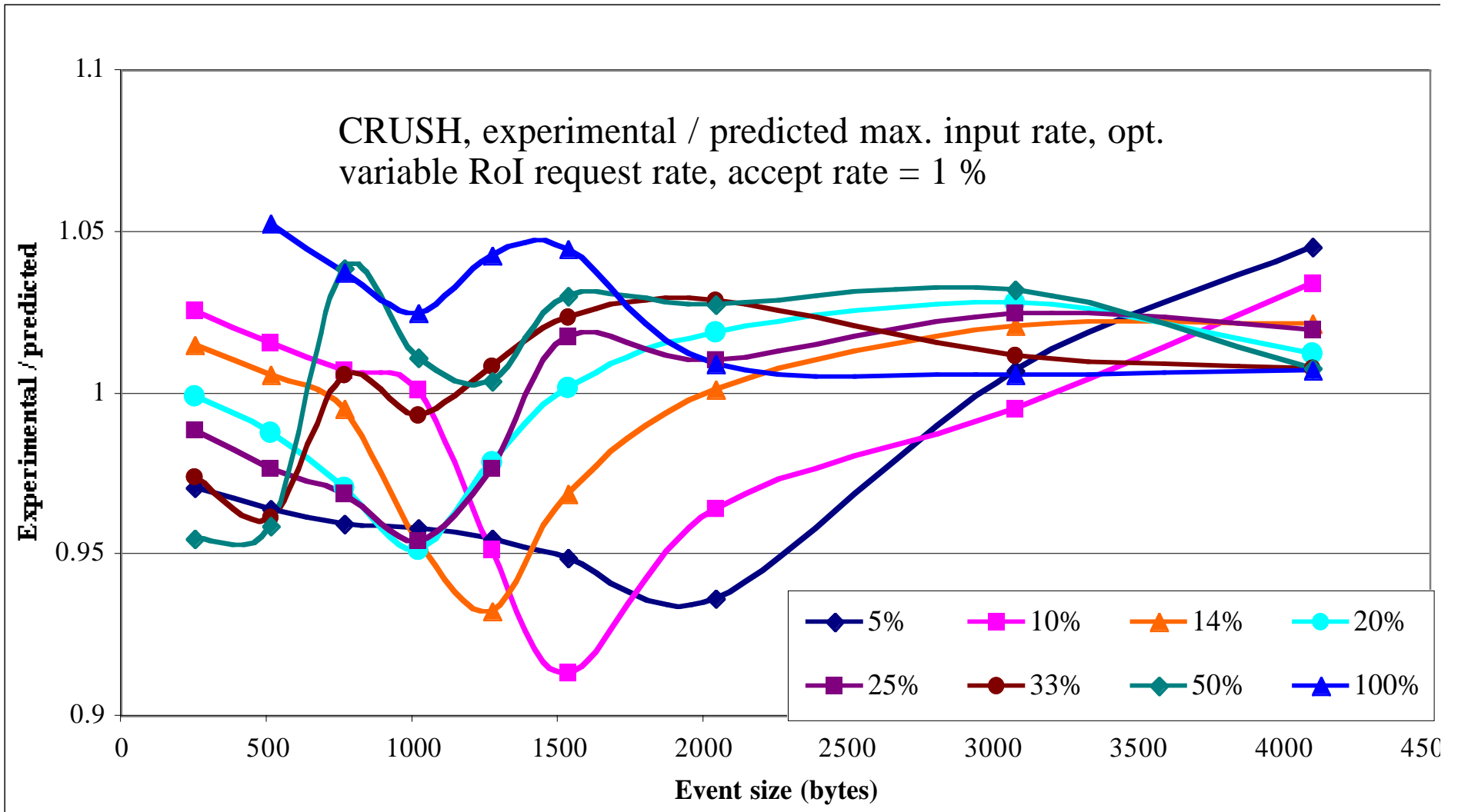


CRUSH, max. input rate, opt. ,
RoI request rate 10 %,
accept rate variable



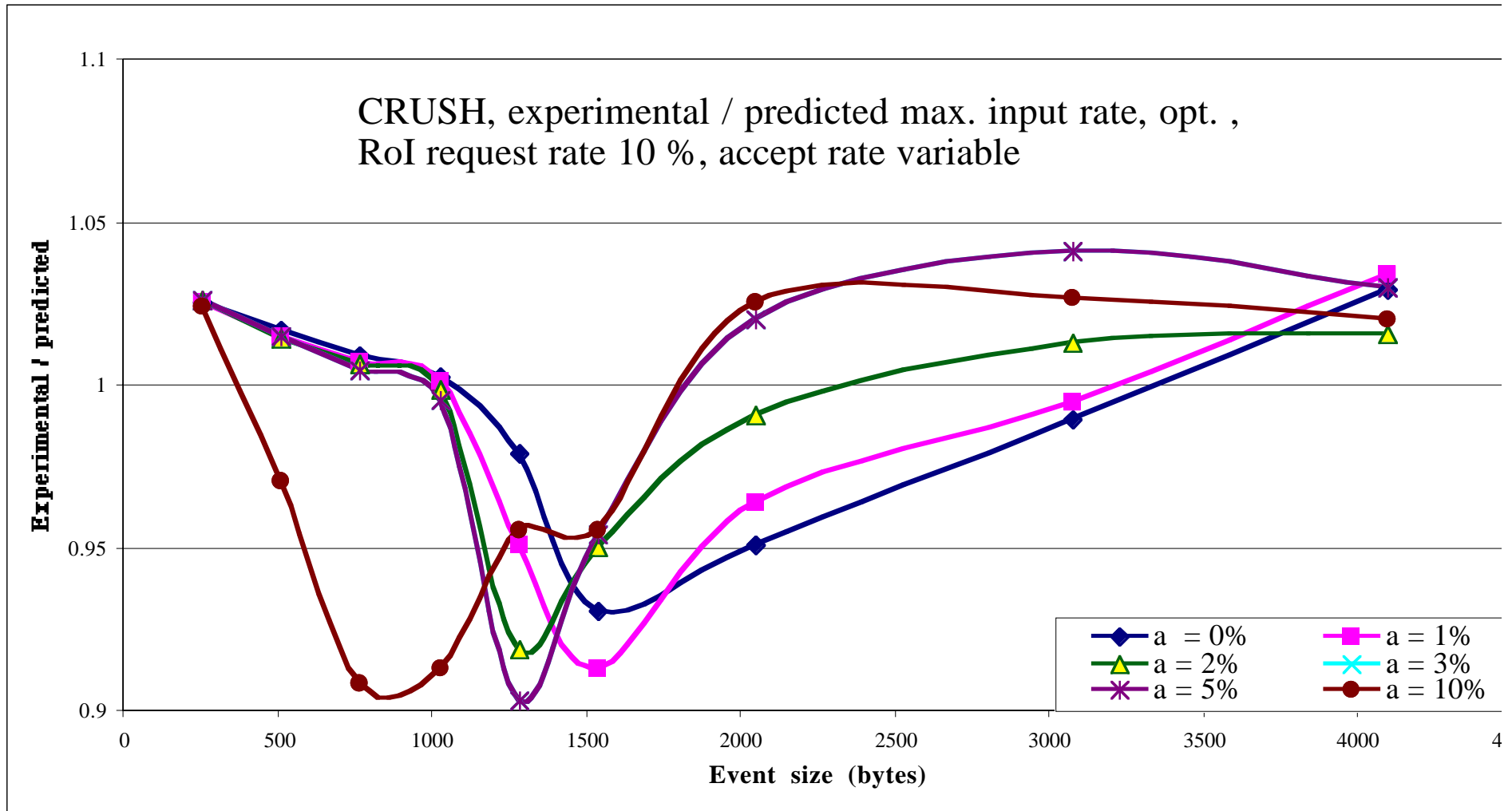
Prediction : f_{\max} (kHz) = $\min (1 / (4.75+10.3 r +3.44 a) , 1/(1.12+5.8 r +0.025 (r + a) n_{\text{bytes}})$
 r = RoI request rate, a = accept rate, n_{bytes} = size event fragment

From 40 MByte/s link



Prediction : f_{\max} (kHz) = $\min (1 / (4.75+10.3 r +3.44 a) , 1/(1.12+5.8 r +0.025 (r + a) n_{\text{bytes}})$
 r = RoI request rate, a = accept rate, n_{bytes} = size event fragment

From 40 MByte/s link



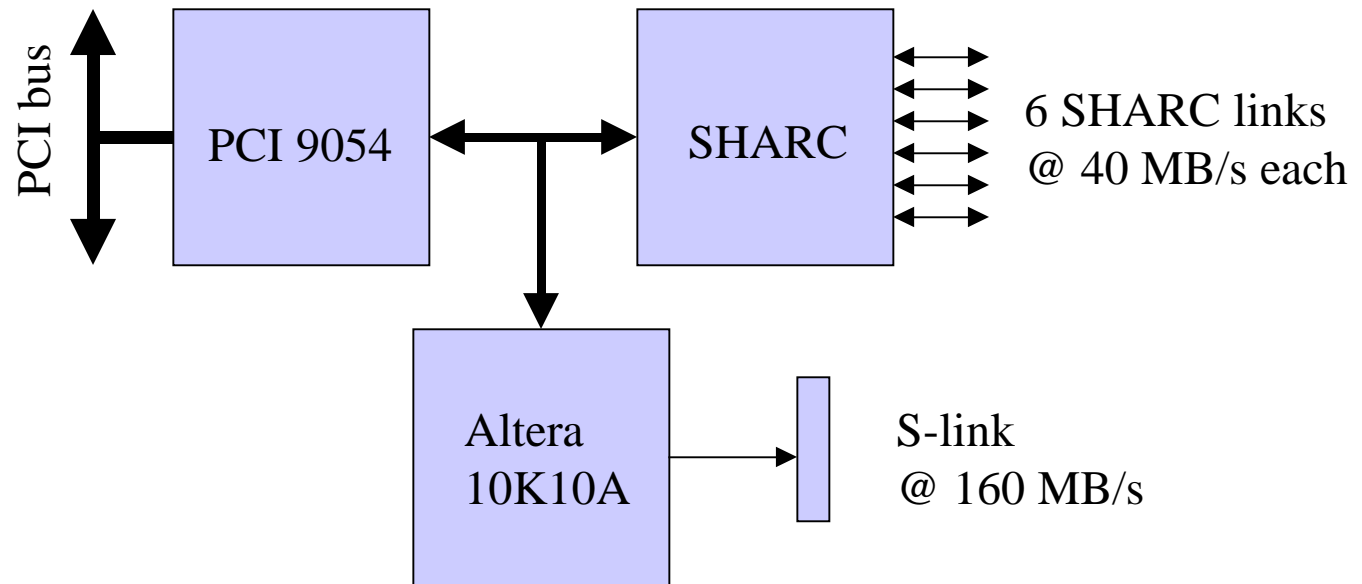
ShaSLINK : *SHARC + output S-Link (+ PCI interface)*

Developed for MROD study : S-link output

PCI interface, supporting PCI transfers without wait cycles also makes the device of interest for ROBOut study

Can be used as programmable (40 MHz) S-link data source

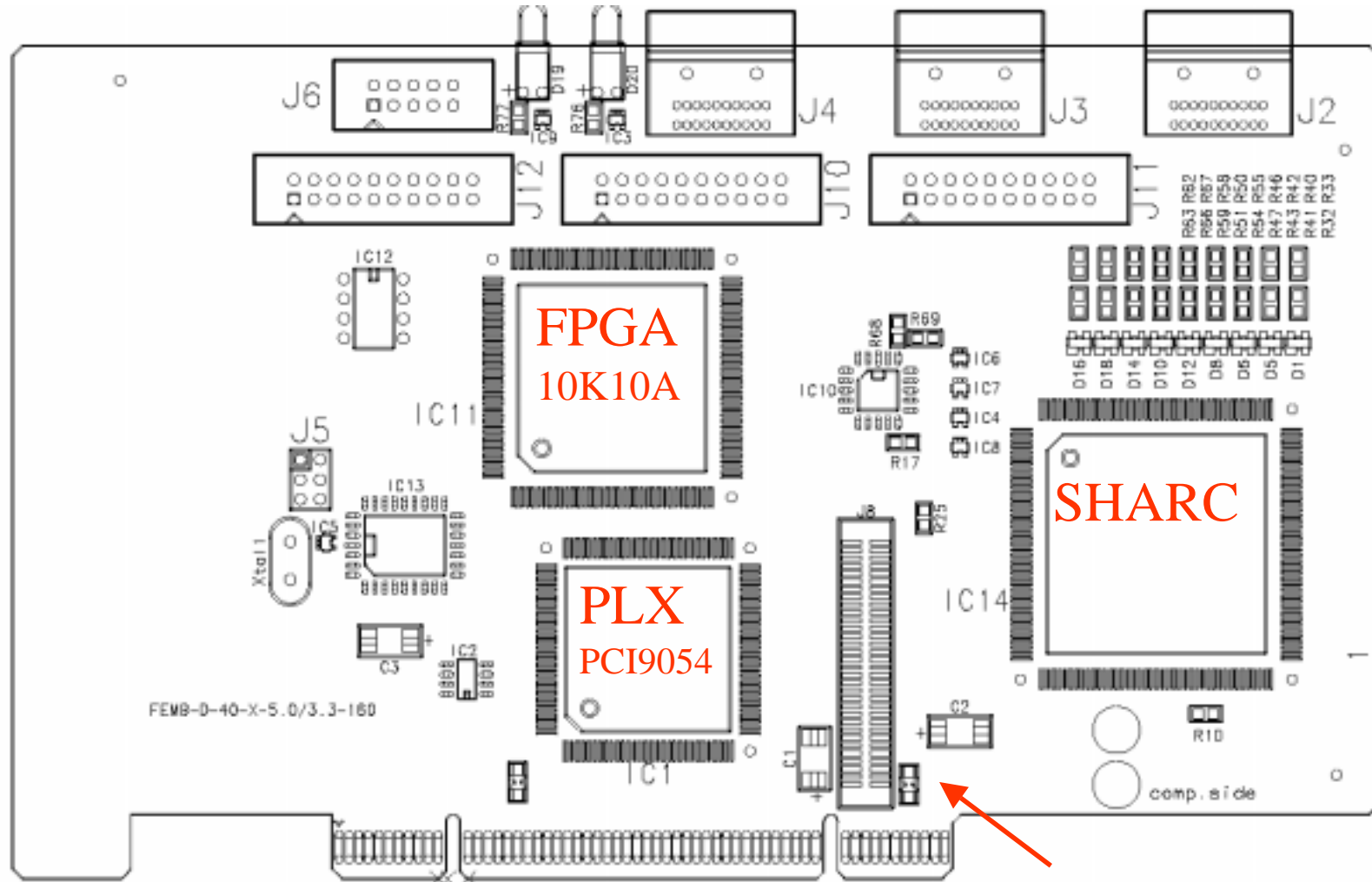
SHaSLINK



PCB in production, start testing in July

ShaSLINK PCB

Connectors for SHARC links



S-link connector

