**CRUSH** ROB-IN performance test set-up
(with real S-link input)

Event Summary: LVL1-ID, buffer address location, …..
CRUSH ROB-IN performance test set-up
(with simulated S-link input)

Event Summaries
(simulating CRUSH FIFO input)

SHARC links

On-chip memory
(128 kW)

PCISHARC

Summary/
RoIR/
T2DR
Producer,
RoID/
T2OutD
Consumer

Host (PC)

DMA controlled transfer

Hardware controlled transfer

Henk B&B, Mar 26 1999
CRUSH ROB-IN software features

← SHARC I/O by DMA operations, concurrently with processing
← I/O buffering in SHARC on-chip memory
← Event fragment (summary) processing: ordered event fragment list
← RoI-Request processing: finding, formatting, sending event
← LVL2 Decision Record processing
  § RELEASE: finding, releasing memory space
  § ACCEPT: finding, formatting, sending event fragment
← Written in C using the Development Toolset for the SHARC processor

Henk B&B, Mar 26 1999
Processor load:
Event fragment processing: ca. 8 μs/fragment
RoI-Request processing: ca. 9 μs/RoIR
CRUSH max. input rate, opt., variable RoI request rate, accept rate = 1 %

> 180 kHz (was ~ 110 kHz for code compiled without optimization specified)

40 MByte/s output limit, limiting factor
CRUSH, max. input rate, opt., RoI request rate 10%, accept rate variable.
Prediction: $f_{\text{max}}$ (kHz) = $\min\left(\frac{1}{4.75 + 10.3\ r + 3.44\ a}, \frac{1}{1.12 + 5.8\ r + 0.025\ (r + a)}\right)$, $n_{\text{bytes}}$ = size event fragment

$r$ = RoI request rate, $a$ = accept rate, $n_{\text{bytes}}$ = size event fragment

From 40 MByte/s link
Prediction: $f_{\text{max}} \text{ (kHz)} = \min \left( \frac{1}{4.75 + 10.3 \ r + 3.44 \ a}, \frac{1}{1.12 + 5.8 \ r + 0.025 \ (r + a) \ \text{nbytes}} \right)$

$r =$ RoI request rate, $a =$ accept rate, $n_{\text{bytes}} =$ size event fragment

From 40 MByte/s link
ShaSLINK: SHARC + output S-Link (+ PCI interface)

Developed for MROD study: S-link output

PCI interface, supporting PCI transfers without wait cycles also makes the device of interest for ROBOOut study

Can be used as programmable (40 MHz) S-link data source
SHaSLINK

PCB in production, start testing in July
ShaSLINK PCB

Connectors for SHARC links

FPGA 10K10A

PLX PCI9054

SHARC

S-link connector
Initial ROBOOut test set-up

Event fragments

CRUSH

ROBIN

RoIR

Decisions

RoI ROBIn mask

Host server

PCI-SHARC

Boot + server

PCI-SHARC

Host server

PCI-SHARC

“summary data” (if no S-link input present)

PCI-SHARC

Host server

PCI-SHARC

Host server