Saclay Robin Status

Last ROBIn design

Input Port

32 bits
4 bits Markers

Input Control
FPGA 100 MHz

Glue Logic
FPGA 66 MHz

33 MHz

Bi-Reg 2

Bi-Reg 1

Full pages

Empty pages

SDRAM
8 Mbytes
Event Buffer

@ 64 MHz

Local Bus

CPU

PCI Bridge

32 bits

D Bi-Reg

Data

DRAM Bus

64 MHz

FPGA 100 MHz

FPGA 66 MHz

PCI Bus
Input Port

Compatible with some S-Link features (to be discussed)

- 32 bits parallel port
- 1 control bit for start and end of event
- Generate “Link Full Flag” from “Robin Input Fifo Almost Full”
- Generate Link Down

Speed

- 33 MHz upgradable to 40 MHz (optimize input control logic) for Larg Calo request

Event Buffer

Organised in pages

- choice between 256, 512, 1024 bytes at configuration time

Input event

- completely hardwired (FPGA)
- transfer from input fifo to event buffer at 64 MHz

Read and modification of event

- by software: local processor
- DMA access for transfer

Page management

list of empty pages in fifo

- filled by local processor
- used by input logic

list of full pages in fifo

- filled by input logic
- used by local processor

- time to switch between two pages at input ~ 200ns

Test

Input Fifo filled by local processor

- can run in loop for test at full speed
Status

completely described in VHDL
simulation is almost finished

main issue was SDRAM access to share input output refresh
avoiding wait states
managing readdressing when swaping
final fit in FPGA for last simulation to be done
Performance evaluation by simulation while building

Start building summer
Delivery 10 pieces by december
Use for Larg ROD - ROB connection in testbeam