PCI Performance Measurements
Introduction

- Test system
- First results & explanation
- Second results & explanation
Measurement Hardware

- PC with Linux operating system.
- 2 or 4 RHUL rob-in card.
- PCI bus breakout card & Logic analyser.
PC Architecture

- Pentium
- Memory
- VIA Bridge
- IDE/ISA Bridge
- PCI Bus 0
- Bridge DEC21132
- Internal PCI Bus
  - VGA
  - SCSI
  - LAN

- Bridge DEC 21132 - 1 slot PCI bus
- Bridge DEC 21132 - 1 slot PCI bus
Measurement Method

- ROB-In cards programmed to DMA out data from local memory to memory on other ROB-in card via PCI bus. This is kicked off by the controlling PC.

- By software: Control program measures time from start until acknowledge.

- By hardware: Logic analyser set to trigger on address phase of transfer.
Hardware Configurations

- Source & Destination on same bus.
- Source & Destination on different busses
- Two sources & Two destinations on one bus
- Two sources on one bus Two destinations on the other bus
## First Results Summary

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Bandwidth (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>One source &amp; One destination</td>
<td>40 MB/s</td>
</tr>
<tr>
<td>Two sources &amp; Two destination</td>
<td>80 MB/s</td>
</tr>
<tr>
<td>One source &amp; One destination across bridge</td>
<td>15 MB/s</td>
</tr>
</tbody>
</table>
Explanation Of First Results

- The destination write had a wait state. This caused the destination FIFO to fill causing a retry.

- Once the destination FIFO is full the FIFO must be emptied before a new burst can be accepted.

- The data from two sources to two destinations interleaves on the bus using it more efficiently.
## Latest Results Summary

<table>
<thead>
<tr>
<th>Setup Description</th>
<th>Bandwidth (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>One source &amp; One destination</td>
<td>127 MB/s</td>
</tr>
<tr>
<td>Two sources &amp; Two destination</td>
<td>130 MB/s</td>
</tr>
<tr>
<td>One source &amp; one destination across bridge</td>
<td>21 MB/s</td>
</tr>
</tbody>
</table>
Explanation Of Latest Results

- The removal of the destination bottle neck has allowed almost the full PCI bandwidth to be achieved, only small loss due to overheads
- Multiple sources can be made to interleave so that losses due to overheads can be minimised
Data rate versus latency setting

![Graph showing data rate versus latency setting](image)
For more detail

- Http://www.hep.ph.rhbnc.ac.uk/~lide