

An Overview of the Mannheim ROB Complex Hardware

1. Abstract

This document describes the hardware of the FPGA coprocessor microEnable and its next generation system Atlantis. It shows the use of these two systems as ROB hardware for the Atlas Detector trigger.

2. Introduction

In conventional computers an algorithm is executed by a CPU that processes a sequence of standard instructions. Contrary an FPGA processor allows the implementation of an algorithm directly in hardware. An FPGA chip contains a high number of simple logical elements which can be “wired” by software by downloading a configuration file. Thus the hardware of the FPGA processor – the chips on the board – is the same for all applications. If configuration is done appropriately input data can be shifted through the processor and are processed on the fly. Since parallel and pipelined processing can be implemented, even a single FPGA can provide a speedup of a factor 10 to 30, depending on the algorithm.

To use FPGA technology in standard PCs the microEnable card was developed. With an SLink adapter as input and and PCI interface as connection to the PC it is a good choice to show the use of FPGA technology as RobIn for the Atlas trigger. The hardware of the microEnable card is described in chapter 3.

From the experiences with microEnable, the Atlantis system was developed. As microEnable, the Atlantis boards are also PCI plug-in cards, but with CompactPCI formfactor. It provides the latest FPGA technology as well as more flexibility. Its hardware is described in detail in chapter 4.

3. microEnable RobIn

The microEnable is a FPGA processor on a PCI plug in card for every standard PC.

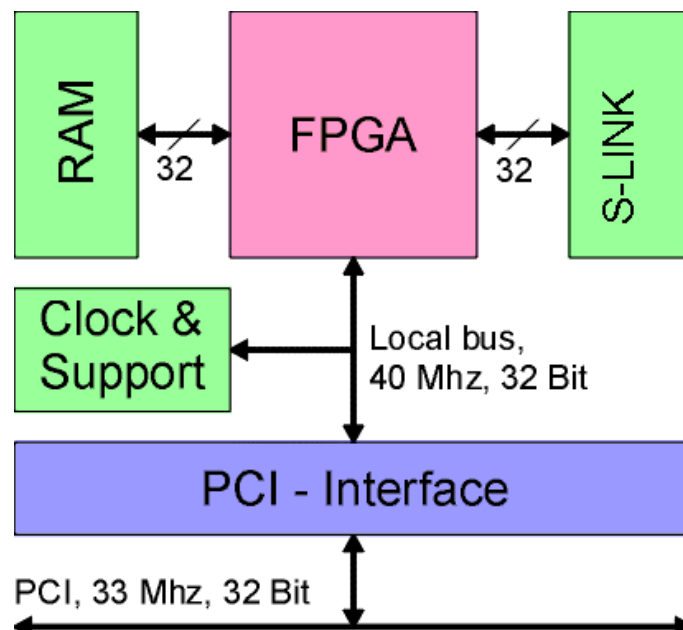


Figure 1
The structure of microEnable

Its structure can be seen in figure 1. The main component is a Xilinx XC4000 series FPGA with up to 120 MHz clock speed. As the clock speed of an application depends on the design inside the FPGA, it runs usually with less than 120 MHz.

The card is equipped with 512kB or 2 MB SRAM which can be clocked depending on the RAM type and design with up to 80 MHz. To link to the PCI bus a PLX 9080 is used. This chip provides two master DMA channels for DMA on demand transfers to host CPU memory.

External input devices, e. g. SLink adapters, can be plugged on the microEnable card as a daughterboard. Both the electrical and the optical SLink are available for microEnable.

For the basic ROB measurements the implemented FPGA design consists of three main parts:

- Input process
Stores the incoming data into the buffer memory (onboard SRAM).
- Output process
Answers incoming requests and transfers the requested event fragment to host CPU.
- Pre-processing
Currently pre-processing for the LVL2 TRT trigger is implemented. It reduces the data, and it simplifies the work of the LVL2 TRT Feature Extraction Algorithm (FEX).

These three parts and it's relations are shown in figure 2 .

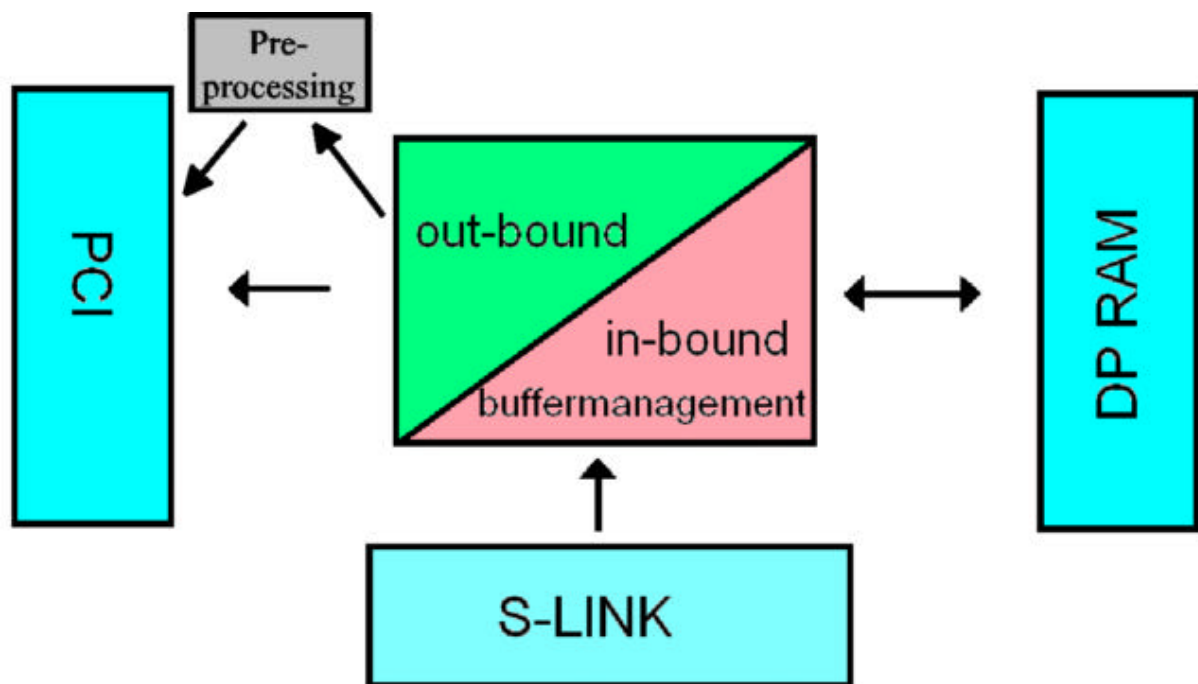


Figure 2
The microEnable RobIn algorithm parts

As both the input and the output process access the event buffer in the RAM a dual port RAM is useful. To get this with the microEnable SRAM, the dual port functionality has to be emulated inside the FPGA. This leads to half the bandwidth for the RAM access in the RobIn application. For storing events inside the SRAM a ringbuffer management is used.

The lifetime of an event fragment in 2 MB SRAM is 5 ms when using an 80MB/s input link.

4. Atlantis based ROB Complex

From the experience with microEnable, the Atlantis System was designed to provide the functionality of a full ROB Complex. It's hardware fulfils the three components of a ROB Complex:

- RobIn
- ROB Controller
- ROB to Switch Interface (RSI)

As main advantage the Atlantis system makes four input links per RobIn card available as well as up to seven RobIns per PCI bus with the use of CompactPCI. Depending on the crate several PCI busses can be present. The current crate provides up to 14 slots for I/O boards. Currently a backplane with one PCI bus (7 slots) is used.

To communicate to each other without loading the PCI bus, the Atlantis boards can make use of a private bus. This is a high speed point to point connection with the neighbouring Atlantis boards and allows a raw bandwidth of ca. 1 GB/s. Figure 3 shows the general setup of the Atlantis based ROB Complex. In the following sections the Atlantis hardware is described in more detail.

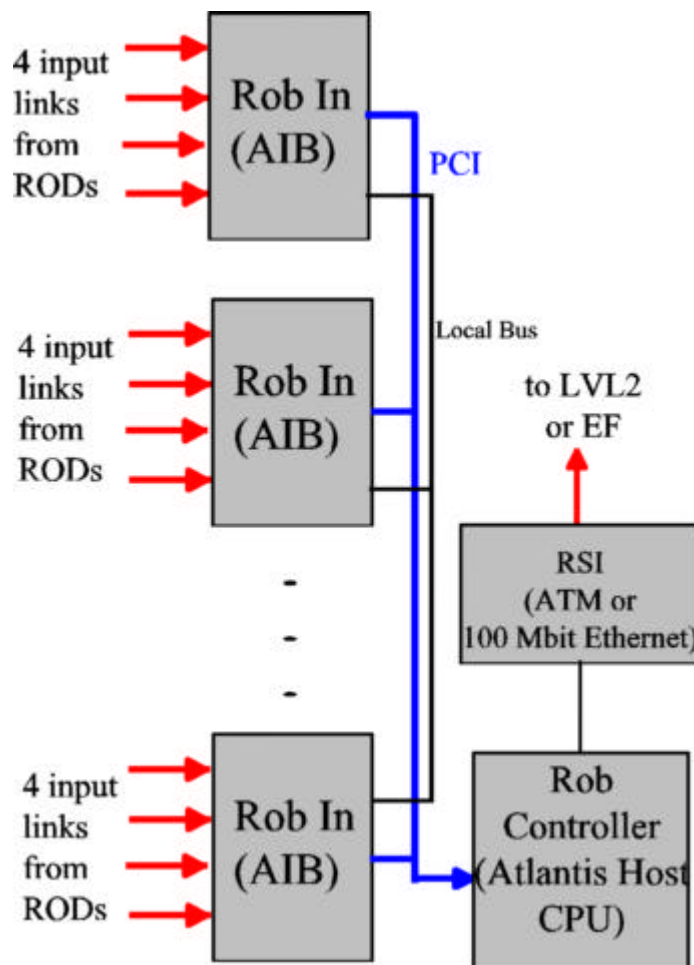


Figure 3
The Atlantis based ROB Complex

a) RobIn

The RobIn is implemented by the Atlantis I/O (AIB) board. This board is shown in figure 4. It is a 6HU CompactPCI board with 2 Xilinx Virtex 600 FPGA's. The board has four input channels which are controlled by the two FPGA's. Per input channel 4 MB SRAM and 128kB true dual port RAM are available.

The data received by each input channel can be buffered in 128 kB true dual-port RAM before they are stored in the event buffer inside the SRAM. This allows a very fast buffering of incoming data, without disturbance of the output facilities. Output to PCI bus is done by an PLX9080 which is the same as in the microEnable board. Each FPGA is also connected to a private bus system, which makes it possible to communicate with other Atlantis boards without loading the PCI bus. This facility makes pre-processing as well as ROI collection over several RobIn boards possible.

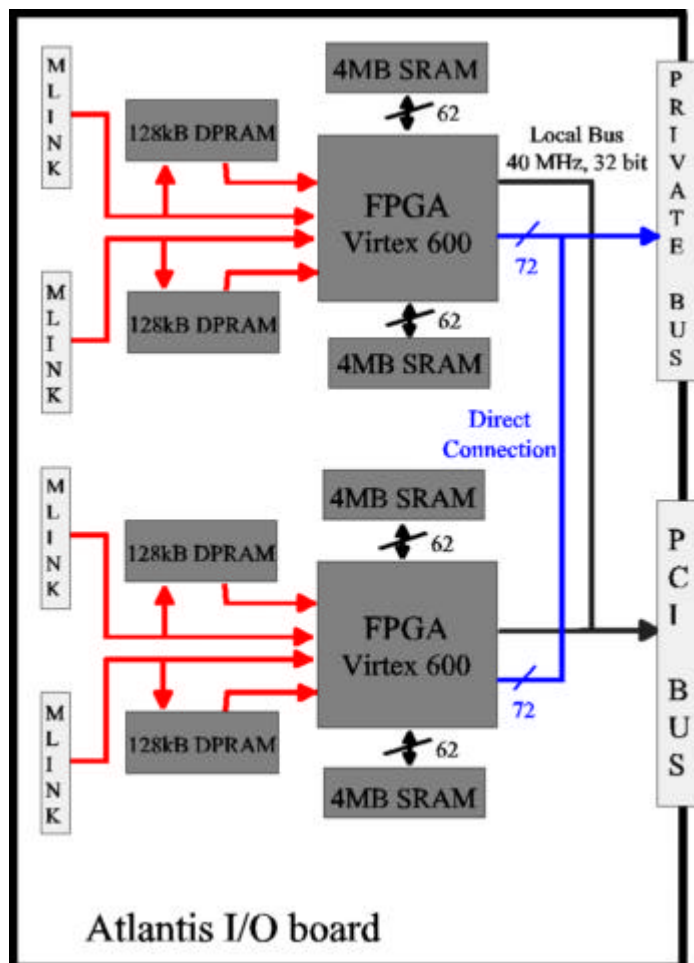


Figure 4

b) ROB Controller

The Rob Controller is implemented by a commercial embedded host CPU. This CPU is a full functional PC which works with WindowsNT and all other x86 operating systems as for example Linux. Also the reference software was tested on this CPU. Currently this CPU is equipped with a PentiumII 400MHz processor, 128 MB SDRAM, built in harddisk, video card, SCSI interface and a fast ethernet card. It controls the CompactPCI bus and with that all plugged-in Atlantis boards.

c) RSI

One possibility for the Atlantis ROB Complex is to use the build in 100MBit ethernet card inside the host CPU for RSI. Furthermore a 155 MBit ATM card is available and tested. It is an PMC card which is plugged with an PMC to CompactPCI adapter into the PCI bus. This card occupies one Compact PCI slot which is no longer available for a AIB.

Also other network cards can be used. If not available in CompactPCI formfactor, several adapters are available for example the above mentioned PMC to CompactPCI adapter or a PCI to CompactPCI adapter.

5. Conclusions

The microEnable hardware showed the possibility of an RobIn purly based on FPGA. The next generation system Atlantis gives more flexibility and new possibilities for the use of FPGAs in applications. With modern hardware it promises a speed up of the ROB Complex application as well as other applications compared with microEnable and standard processors.