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μEnable
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FPGA design

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Out-bound process

PCI → request → EVENT

lookup → PAGE

address → LUT

DP RAM → Fragments
Current implementation
Ringbuffer

- counter for next page
- simple
- nothing to do for ROB Controller
- no forgotten fragments
- all fragments have same lifetime
Outbound process
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ROB-IN Output

measured ROB-IN Output Rates

MB/s

Fragment size [kB]
Mannheim University

ROB-IN Output Rates

- Measured @ 20 MHz + 60 us overhead
- Expected @ 20 MHz + 60 us
- Expected @ 20 MHz + 30 us
- Expected @ 33 MHz + 30 us

Fragmetsize [kB]

Fragments /s [kHz]

MB/s
Preprocessing

• Implementet for TRT Barrel (old Data format)

• 1642 Straws with ca. 30 % occupancy
  average of 2 hits per Straw

• average Proccessing Time:
  \[2600 \text{ CLK @ 20 MHz} = 130 \mu\text{s}\]
Preprocessing measurements

- Output rate with preprocessing and 140\(\mu s\)
  Software overhead:
  9 MB/s = 4 kHz Eventrate

- New Driver with ca. 30\(\mu s\) overhead
  13 MB/s = 6 kHz Eventrate

- Processing of 2 unhit Straws in one CLK will give a factor of 1.3
  (without Software overhead)
Preprocessing Implementation

- Old dataformat
- unhit straws need 1 CLK
- Hit straws need 1 CLK + 1 CLK per BC
- New dataformat will give similar results
- processing of 2 unhit straws in one CLK possible
Current implementation

- 512 kB RAM, Xilinx 4028 @ 20 MHz
- 127 Pages a 4kB =>
- 1,2 ms fragment-lifetime @ 100kHz
- max. fragmentsize 4kB
- Output Rate 33MB/s = 8,3 kHz with old devicedriver
- Slink-Interface @ 20 MHz = 80 MB/s