Compact ROB:

* 8 ROBs / board
* 1..4 boards / PCI-bus  <70 MB/s
* 1..8 PCI-bus / subdetector  TRT: 22 PCI-bus
  Calo: 32 PCI-bus

* there are more PCI-bus per crate
* each crate has interface to supervisor, LVL 1.5, LVL 2, LVL3/DAQ
RoI-Collection (Components)

available!

S-Link
ROI fragments (from Concentrator)

104 MByte/s

2 MByte

1k events (or RoI-fragments) x 2kB size

10 ms latency

Memory

fragment controller

local memory controller

RoIC-Memory Modul (local modul)

RoIC-Control Modul (global modul)

FPGAs (programmable)

readout controller

global memory controller

data for monitoring

complete ROIs (to FEX)

320 MByte/s

LVL 1.5 37..52 MB/s
LVL 2 3..10 MB/s
LVL 3/DAQ 16..24 MB/s
Enable++

3 functional units

fully configurable

I/O submodules for physical links

Variable topology of computing core

Scalable I/O and computing power

I/O subsystem

7 I/O module ports

8 Interconnect slots

200MB/s per slot

Computing Core

16 FPGA blocks

8 Interconnect slots

Configurable Backplane, 5 ports

A. Kugel

Page - 5

Mannheim University
ROBs built completely from FGPAs

**Jena**: proposal presented in Marseille

**Observations:**

Maximum latency for *all* events determined by size of buffer memory

LVL1 Id determines location of storage in memory, page size is upper limit for event length

**Mannheim**: possible use of Enable ++ , which has 12 MByte of SRAM

**Observation:**

Enable++ probably has more resources than required

Future of further work in this field by Jena and Mannheim groups unclear