UK ROB-IN design issues

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Motivation

- modularise ROB for prototyping & development
- ROB-IN module = input link + buffer + buffer manager + data/message path
- current design to fit with current interface “standards” (S-LINK, PCI/PMC) + URD
PCI ROB-IN (with i960-RP)
Design parameters

- **SIZE**: PMC (+ S-LINK)
- **POWER**: aim for PMC spec: 7.5W (+ S-LINK?)
- **PROCESSOR**: i960-RP/D for convenience, (paper exercise => PowerPC, AMD)
- **LOGIC**: MACH 5 (convenience + predictability => CPLD rather than FPGA)
PMC dimensions

- PCB solder side: 9.80
- Front Panel: 32.00
- Dimensions: 4.70 x 31.00
Performance

- INPUT: 100 MB/s @ 100 kHz (URD)
- PAGE SIZE: 1 kB (optional multi-pages)
- BUFFER SIZE: 0.5 MB (requirement?)
- PCI BANDWIDTH: (estimated requirements)
  - messages: 3.17 MB/s @ 1 Hz - 10 kHz
  - data: 10 MB/s @ 10 kHz
- PROC SPEED: 30 MIPS => ~75 kHz, but RD runs with 2x clock
Status & applications

• Status:
  – RP-version PCI board being debugged
  – PMC & RD PCI to follow shortly

• Potential applications:
  – DAQ -1
  – Pilot project
  – SMP pilot
  – Multi-ROB