S-Link

Decoder

Inc
Address

Addr

Buffer Memory

D

ADR

>= 256K * 32 bits

A

MUX

Select

32*34

FIFO

Select

D

D

SHARC

Select

Internal
Memory

A

128K * 32 bits

SHA

Links

DMA
Control

Data for programming decoder

Inc

Clr

A

D

40 MHz

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>BOB Pattern</td>
<td>nnnnnnnnnH</td>
<td>nnnnnnnnnH</td>
</tr>
<tr>
<td>01H</td>
<td>BOB Control Bit Pattern</td>
<td>xxxxxxxxpH</td>
<td>00000000pH</td>
</tr>
<tr>
<td>02H</td>
<td>BOB Mask</td>
<td>nnnnnnnnnH</td>
<td>nnnnnnnnnH</td>
</tr>
<tr>
<td>03H</td>
<td>BOB Control Bit Mask</td>
<td>xxxxxxxxpH</td>
<td>00000000pH</td>
</tr>
<tr>
<td>04H</td>
<td>EOB Pattern</td>
<td>nnnnnnnnnH</td>
<td>nnnnnnnnnH</td>
</tr>
<tr>
<td>05H</td>
<td>EOB Control Bit Pattern</td>
<td>xxxxxxxxpH</td>
<td>00000000pH</td>
</tr>
<tr>
<td>06H</td>
<td>EOB Mask</td>
<td>nnnnnnnnnH</td>
<td>nnnnnnnnnH</td>
</tr>
<tr>
<td>07H</td>
<td>EOB Control Bit Mask</td>
<td>xxxxxxxxpH</td>
<td>00000000pH</td>
</tr>
<tr>
<td>08H</td>
<td>BOB Word Flag 0</td>
<td>xxxxxxxqH</td>
<td>000000qH</td>
</tr>
<tr>
<td>09H</td>
<td>BOB Word Flag 1</td>
<td>xxxxxxxqH</td>
<td>000000qH</td>
</tr>
<tr>
<td>0AH</td>
<td>BOB Word Flag 2</td>
<td>xxxxxxxqH</td>
<td>000000qH</td>
</tr>
<tr>
<td>0BH</td>
<td>BOB Word Flag 3</td>
<td>xxxxxxxqH</td>
<td>000000qH</td>
</tr>
<tr>
<td>0CH</td>
<td>EOB Word Flag 0</td>
<td>xxxxxxxpH</td>
<td>00000000pH</td>
</tr>
<tr>
<td>0DH</td>
<td>EOB Word Flag 1</td>
<td>xxxxxxxpH</td>
<td>00000000pH</td>
</tr>
</tbody>
</table>

Remarks:

‘n’ is any hexadecimal number  
‘q’ is 00H, 01H, 02H or 03H  
‘p’ is either 00H or 01H  
‘x’ is don’t care
Sharc based ROB-in with minimum amount of dedicated hardware

1. Data format not fixed

2. Per event always a block with data like start address in buffer, end address in buffer, event id, etc., of fixed size can be transported by one of the DMA controllers of the processor (also in case of a fault)

3. Processor has direct access (with minimal CPU load) to event fragment length and other important information, because of 2.

4. Small FPGA can probably do the job -> cheap + low power dissipation. Design for Altera chip under study.

5. Sharc is small and has relatively low power dissipation

6. Sharc links provide enough bandwidth for connecting to Sharc ROB controller and only need 6 signal lines

==> Want to find out more, two lines of study :

a. Hardware implications

b. Software implications