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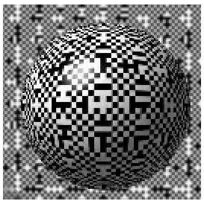

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MiniMasterMux

The MiniMasterMuX is a combination of the MasterMux and USA15Mux. It connects a maximum of 4 RasMuxes to the PCs' serial port and the framegrabber. It is a prototype multiplexing system for the alignment system within the barrel muon detector and the associated alignment systems in ATLAS. It will not be installed in ATLAS.

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Introduction

The basic idea is to create an image of a coded mask on an optical sensor by means of a lens. An infrared LED lights the mask. In this set up the relative position in X and Y direction is measured along the line mask, optical center of the lens and the sensor. Also the (relative) rotation of the mask or the sensor can be measured. By calculating the actual image spotsize and comparing this with the mask spot size, the position of the lens along the Z-axis is calculated. Also the relative rotation around the X and Y-axis of the mask in respect to the CCD sensor can be calculated.

The system can be split into three major components

1. The optical system:
   - a coded mask
   - a lens
   - an optical sensor
2. The sensor and framegrabber combination (video):
   The optical sensor is a commercially available B&W observation camera, without a lens. This can be a CCD type or CMOS.
   The framegrabber is a commercially available 8-bit grayvalue type E.G. Data Translation DT3152. Three levels of multiplexers connect one of the sensors (more than 6000 in total) to the framegrabber.
3. The reconstruction software ICARAS.

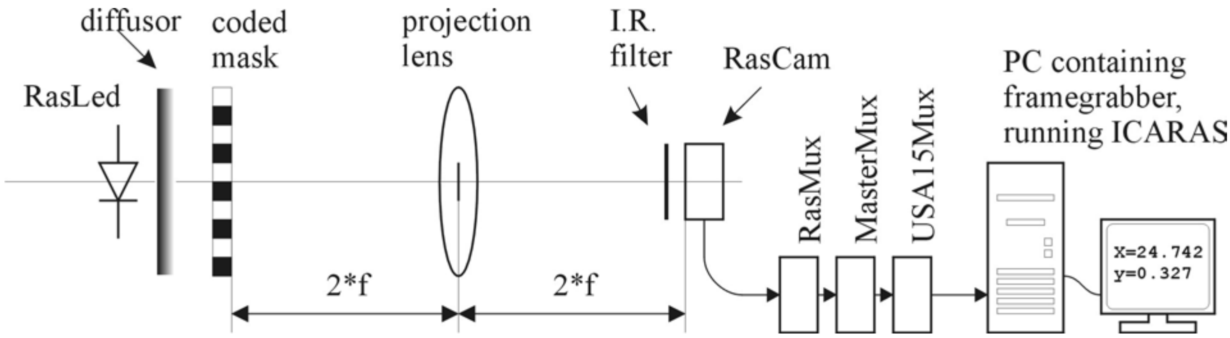

Figure 1: Alignment system

This paper describes the MiniMasterMux, which connects a maximum of four RasMuxes to the PCs' serial port and the framegrabber. It replaces the two stages of multiplexing, which are needed for the full system: the MasterMux and the USA15Mux. It cannot be used with RasMux V1. Instead of interfacing to the parallel port (as the MasterBrico did) it talks to the PCs' serial port. This prototype is used to test the new RasMuxes and to enable the different institutes to start using the new RasMuxes.

The framegrabber digitizes the picture and the IcaRas software cycles through the total system and hands over the picture-files to the analyses software.

The new RasMuxes are mounted on the longbeam of the barrel muon chamber and a few other convenient places for non-chamber alignment systems.

Specifications:

The video signal from the RasMuxes is differential. This is converted to standard CCIR for the framegrabber. The clock from the RasMuxes uses LVDS (Low Voltage Differential Signaling) levels. Communication between the MiniMasterMux and RasMuxes uses LVDS levels also.

RasMux connections (D25 male connector)		
Pin		**Function**
1		Shield
16		24 V
20, 21		12 V
11, 23		5 V
4, 8, 9, 13, 25		Ground
Pos.	**Neg.**	Note: All active signals are differential.
14	2	Video out, differential 1V.
15	3	TCK
17	5	TMS
18	6	TDI (serial data to the RasMux)
19	7	TDO (serial data from the RasMux)
22	10	Pixel clock, LVDS.
24	12	RasMux detection loop

Framegrabber connections (D15 male connector)	
Pin	**Function**
1	External clock
3	External trigger
8	Video
9…15	Ground (grabber only connects pin 15)

Serial connections DCE (D9 female connector)	
Pin	**Function**
1	RLSD (not used)
2	TXD (out)
3	RXD (in)
4	DTE ready (in)
5	Signal ground
6	DCE ready (out)
7	CTS (in)
8	RTS (out)
9	Ring (not used)

VSP

For the serial protocol to communicate with the RasMuxes a simple standard has been defined (Very Simple Protocol). The electrical implementation is fully differential (LVDS). All lines are terminated at the receiving end. The interface is used to control the settings of the RasMuxes and read back status bits. The RasMux translates the MasterMux commands to the I^2C protocol understood by the sensors and electrically translates the sensors' response to VSP.

The MiniMasterMux combines the functions of the (future) MasterMux and the (future) USA15Mux. It should be seen as two separate parts: A 4-channel MasterMux and a one channel USA15Mux. Between those parts the same 4 wire VSP protocol is used. The MasterMux listens to address 0010. The USA15Mux uses a small processor to talk to the PCs' serial port and to translate and retime the VSP protocol.

The MasterMux part is driven by an 8 bit command and returns a 10 bits status.

VSP input register		
Bits	**Name**	**Bits**
0	MxTs1	Talk select
1	MxTs0	
2	*MxSE	Slave enable
3	MxSs1	Slave select
4	MxSs0	
5	*MxVe	Video enable
6	MxVs1	Video select
7	MxVs0	
Enable: active low.		

VSP output register		
Bits	**Name**	**Bits**
-1	ACK	Address acknowledge
0	MxTs1	Talk select
1	MxTs0	
2	P24St	Status 24V switch
3	MxSs1	Slave select
4	MxSs0	
5	P12St	Status 12V switch
6	MxVs1	Video select
7	MxVs0	
8	PUR	Power up reset

Video select (plus enable) enables the power to a RasMux. The video-signal from this RasMux is routed to the framegrabber. *Slave select* enables power to an other RasMux to switch on a RasLed. *Talk select* routes the VSP to the RasMux selected. If a RasMux, cable or other component has a short circuit, the status bits indicate this. Address 0010 is acknowledged by the MasterMux part of the MiniMasterMux. The power off bit is set at power up and reset by a VSP cycle.

Protocol description

The VSP protocol uses four lines in a way similar to the JTAG protocol. The signals are named the same: TMS, TCK, TDI and TDO. TMS is used to switch between sending an address and shifting data. Here the difference with JTAG comes in: These are the only two possibilities. Both address and data are send with the least significant bit first. The length of address and data are not fixed. There is a minimum of one address bit in the VSP protocol. In the RasNik system 4 bits are used.

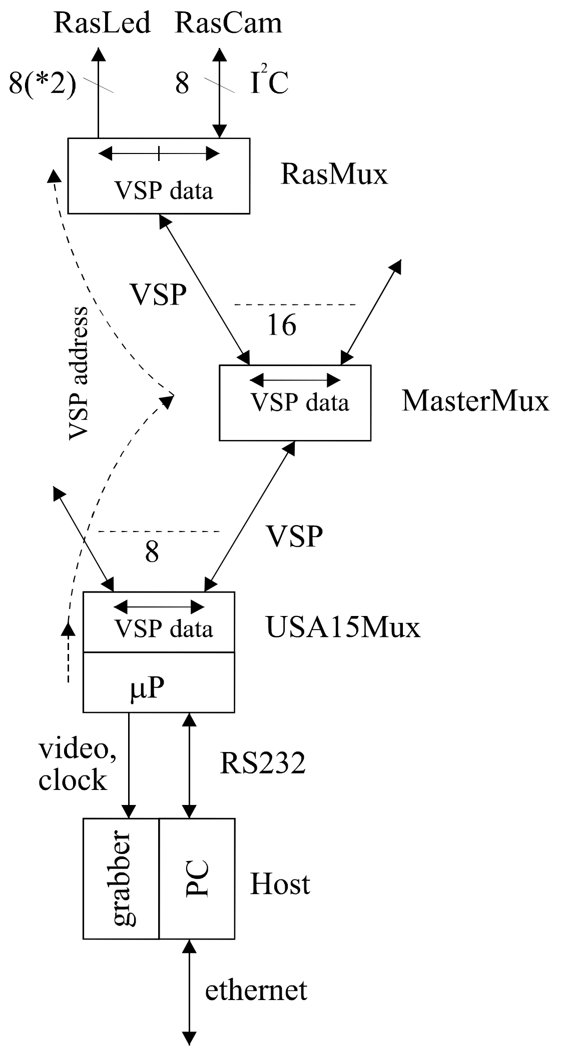

Figure 2: RasNik communication

The addressing part of the VSP protocol is used vertical in the tree of multiplexers. A module may respond to more than one address though.

Horizontal selection (which I/O) is taken care of by the data send to the multiplexer selected. One can go back and forth in the tree. After enabling a RasLed through the different levels of multiplexers, for example, one can check the status of the USA15Mux.

When the addressing is finished and TMS is kept low, the other lines can be used for other purposes than just loading a register. In the RasNik system they quite directly interface to the I^2C bus selected. In the different levels of the RasNik multiplexing scheme four address bits are used.

Address 0000 is used as a “deselect all”.

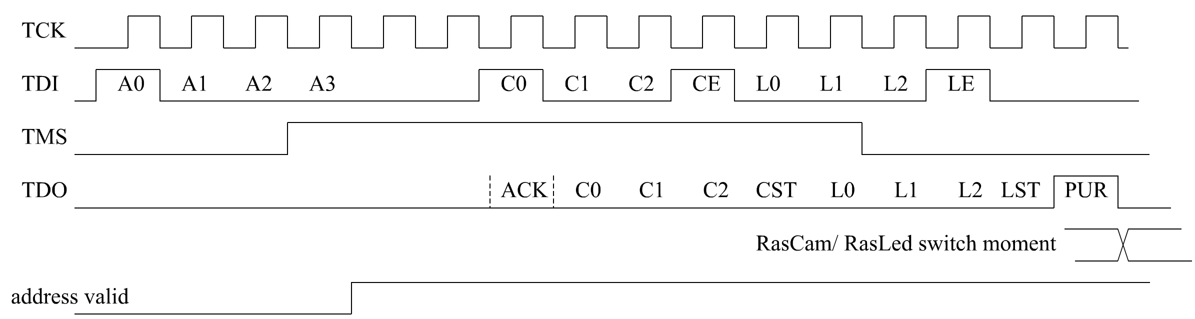

Figure 3: RasMux VSP example

A VSP cycle is shown, issued after a power-up condition. The *address valid* signal is an internal signal of the RasMux. The RasMux responds to the address 0001. The MSB of the address is indicated by TMS = 1. The address is then held to generate *valid address*, which enables shifting data in, copying of internal data and status to the output shift-register and generating an acknowledge. At the end of the output shift-register the power-up reset register bit is shifted in. This bit is reset by the end of the VSP cycle. After TMS goes low, two more bits are shifted in and four bits are shifted out. In the RasMux the VSP bus is connected to the appropriate I^2C bus, after this (selected RasCam)

.

The example shows:

- Loading of address 0001
- Selecting RasCam 001, including the enable bit.
- Selecting RasLed 000, including the enable bit.

At the same time the power-up situation is shifted out:

- The enables of the power outputs are reset.
- The power-up reset bit is set.

Selecting RasCam or RasLed 1000 will disable the power-switch.
After the VSP cycle the RasMux stays selected, which is indicated by the yellow LED. By keeping TMS low, the other lines (TDI and TCK in this case) can be used for the I^2C communication.

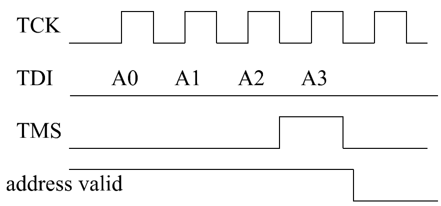

Figure 4: VSP deselect

Only one multiplexer in the total tree can be selected at the time. Address 0000 deselects all multiplexers, without changing the settings.

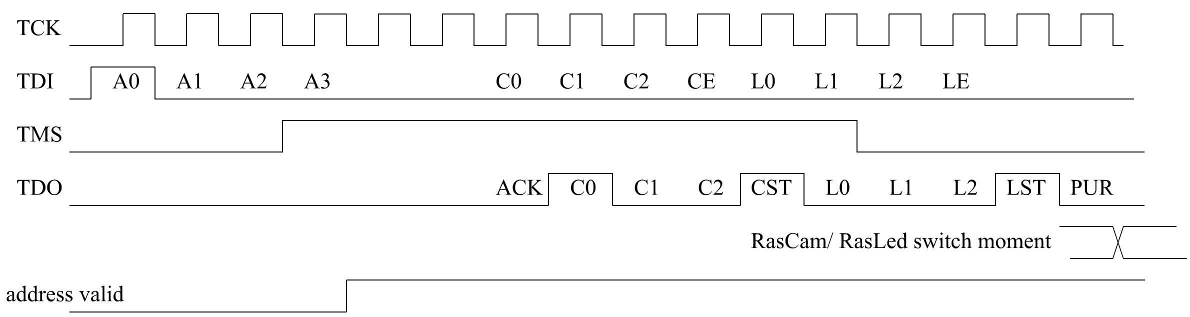

Figure 5: second VSP cyle

The deselect cycle has reset the *address valid* bit, while the first VSP cycle has reset the power-up reset bit. The new settings disable both RasCam and RasLed drivers and the old settings are read back: RasCam 001, with status Ok, and RasLed 000, with status Ok.

Power

The MiniMasterMux is powered by a single power supply: 24 V, 500 mA. This is converted to 12 and 5 V for the RasMuxes. All three supplies are switched off when a RasMux is not needed for the current measurement. A maximum of two RasMuxes can be powered at the time to be able to connect the components (RasCam and RasLed) of one RasNik system to different RasMuxes. The current drawn by the various components from the 24 V supply:

- MiniMasterMux: 75 mA (with LCD display: 85 mA),
- RasMux: 65 mA,
- RasCam: 55 mA,
- RasLed: 70 mA.

The USA15Mux and MasterMux are estimated to draw 100 mA each. The USA15Mux will power only one of the (maximum 8) connected MasterMuxes. This MasterMux can activate one or two RasMuxes.

Since power conversions are done in the USA15Mux, the total power dissipated in the experimental hall (USX15) must be calculated differently:

- MasterMux: 100 mA @ 5 V = 500 mW,
- RasMux: 80 mA @ 5 V = 325 mW (in some cases times two),
- RasCam: 100 mA @ 12 V = 1200 mW (960 in the RasCam, 240 in the RasMux),
- RasLed: 70 mA @ 24 V = 1680 mW.

There are eight USA15Muxes. Each can have one active channel.

The power to an output (to a RasMux) is only switched on when a RasMux is detected by means of a simple loop though the cable and RasMux.

Serial interface

The MiniMasterMux is controlled via the PC's serial port. Settings: 155.2 kb, 8bN1S, no handshaking. Human readable instructions are used, the same goes for status and error messages. Conversion to the VSP protocol is done by firmware, stored in an Atmel AVR RISC processor. When the MiniMasterMux is split into the MasterMux and USA15Mux, the processor will be located in the USA15Mux.

Serial commands	
L237	Switch RasLed on at USA15Mux channel 2, MasterMux channel 3, RasMux output 7. Address 8 on the RasMux disables the power-switch.
C237	Switch RasCam on at USA15 channel 2, MasterMux channel 3, RasMux channel 7. Address 8 on the RasMux disables the power-switch.
R	Read the RasCam settings (4 * 8 bit).
R1	Read and decode RasCam settings.
WRDDD	Write 3 * 4 bits settings to register R.
O	All power is switched off. Only the processor remains active.
S	Read the status, see below for the list.
Ddd	Delay to trigger. Range: 0…FF, times 10 ms.
V	Version, format YMD, example 02/05/02. Comment might be added.
U	Unconnected, total deselect.
All Addresses and data are hexadecimal. All commands must be terminated by CR. Using the MiniMasterMux the 2nd digit in the L and C commands is ignored.	

First the RasLed should be chosen, then the RasCam. Addressing the RasLed always returns an *OK*. When a RasCam is switched on, automatically the I^2C command for generating a continuous clock is issued. This is checked by the micro-processor. *Either clock* OK or *clock error* is generated. When the RasCam does not respond (or no RasCam is connected to the addressed channel), an acknowledge error is generated.

The R1 command translates the hexadecimal response of the RasCam into a readable response. The clock status and current measurements are added.

Example:

C 74	**F 151**	**G 1**
Course exposure time	Fine exposure time	Gain
AEC 1	**BC 0**	**AGC 1**
Automatic exposure control	Black calibration enable	Automatic gain control
Lin 1	**BL 0**	**ID 2**
Linear mode	Backlit enable	Camera identifier
CkOK	**C 195**	**L 70**
Continuous clock detected	12 plus 5V current (RasCam plus RasMux)	24 V current (RasLed)

Reading the status returns a list of values.

clock OK clock error	Checks the RasCam clock signal.
12V: 190	The combined current of 12 and 5 V outputs in mA.
24V: 70	Current of the 24 V output (LED).
I2C: 03E5C2C2 Rack error	Reading the last addressed RasCam.
2: 0048	Status of the multiplexer part of the MiniMastermux.
1: 011E	Status of the RasMux.

I^2C

RasCam register settings (WRDDD)		
Register	**Name**	**Comments**
0	(Invalid)	
1	Set-up 1	Basic functionality
2	Set-up 2	Pixel control and read
3	Coarse exposure	AEC must be 0
4	Fine exposure	AEC must be 0
5	Gain control	AGC must be 0
6	(Invalid)	
7	(Invalid)	
8	Lower exposure threshold	
9	Upper exposure threshold	
A	Analog control	
B	(Invalid)	
C	(Invalid)	
D	(Invalid)	
E	Set-up 3	Pixel synchronization
F	(Invalid)	

There is some hysteresis in the AGC/ AEC control loop. Therefore, when both are enabled, and settings are written via I^2C to the registers 3, 4 or 5 that are approximately correct, it will not be adjusted by the sensor. In this way, after switching on the power of a RasCam, one does not have to wait until the AGC/ AEC control loops stabilizes before grabbing the image.

In practice one should only set registers 3 and 5. In IcaRas (I^2C settings) these are called *coarse* and *gain*. All register settings that affect the exposure require one frame-period (40 ms) to be transferred from the I^2C interface to the internal register. The handshake (OK) from Mini-MasterMux to the serial interface takes this period into account.

Setup register_1

The setup register_1 is used to select different basic operating modes:

Setup register_1, (register 1) valid data bits: 11			
Bit	**Default**	**Function**	**Comment**
0	0	Normal/Backlit	Selects between normal and backlit exposure modes. The power-on default is normal mode. See below.
1	0	Linear mode[1]	Selects between a linear (LIN=1) or gamma corrected video signal.
2	1	Auto gain enable	When set 0, the current gain value selected is frozen. With AGC=0 a new gain value can be written to the gain register via the serial interface (header code[2] 0101).
3	0	Inhibit black calibration	Disables automatic gain control
4	1	Enable Auto exposure Control	When set 0, the current exposure value is frozen. When automatic exposure control is inhibited then automatic gain control is also disabled. With AEC=0 a new exposure value can be selected by writing to the coarse and fine exposure registers via the serial interface (header codes 0011 & 0100).
5	0	Horizontal shuffle enable	Shuffles the read out of the horizontal shift register. Even columns read out together then odd columns.
6	0	Vertical shuffle enable	Shuffles the readout of the vertical shift register. Even lines read out together then odd lines.
7	1	Force black calibration	Requests a re-calibration of the black level while bit is low.
8	0	Clock divisor DIV0	System clock division[3]: 00=÷1; 01=÷2; 10=÷4; 11=÷8
9	0	Clock divisor DIV1	
10	1	Internal Register	Must be set for correct operation.
11	0	Not used	
The backlit mode reduces the area that is used by the auto exposure algorithm from 80 to 25 % of the active area. This mode improves the contrast of the foreground objects in scenes with a bright background.			

[1] The gamma corrected mode is disabled by hardware on the sensor board. See the RasCam description under *options*.

[2] The I^2C header-code corresponds to the register number used by IcaRas.

[3] Decreasing the system clock rate proportionately increases sensor sensitivity (by increasing exposure time), but also decreases frame frequency. System clock must be x1 for standard CCIR or EIA framing.

Setup register_2
The setup register_2 is used to select read data, valid pixels and video output operating modes:

Setup register_2, (register 2) valid data bits: 12			
Bit	**default**	**Function**	**Comment**
0	0	Read mode A	Select shadow read mode, bits 0,1 are mutually exclusive.
1	0	Read mode B	
2	PVE	Pixel sample clock select.	Pixel sample clock mode. See table below. Bit 1 is set by the PVE pin level.[4]
3	0		
4	0	Not used	Must be set to 0 for correct operation.
5	0	Enable free running pixel clock	Overrides bits 3 and 2.
6	0	External pixel thresholds	Use external algorithm thresholds in exposure controller.
7	0	Not used	Must be set to 0 for correct operation.
8	0	Not used	Must be set to 0 for correct operation.
9	0	Shuffle Modes, bits 2, 1 and 0.	Video output enable control bits. See table *Shuffle Modes*
10	0		
11	0		
Bit 0 and 1 show a problem, needs further investigation (use 00 for mode A).			

Pixel sample clock mode (bits 3 and 2 of set-up register 2)			
Bit			**Pixel clock pin output.**
5	**3**	**2**	
0	0	0	Disable pixel valid clock pin output.
0	0	1	Qualify image area only (as defined for CCIR or EIA)
0	1	0	Qualify central 256 x 256 pixels (CCIR only)
0	1	1	Pixel valid active during interline periods of visible image lines only.
1	X	X	Enable free running pixel clock

Shuffle modes (bits 11, 10 and 9 of set-up register 2)						
Bit			**Area where the video output is active.**			
11	**10**	**9**				
0	0	0	All (normal operation)			
0	0	1	None. Video output in tristate.			
0	1	0	Sync only.			
0	1	1	Sync plus Q1 image.			
1	0	0	Q1	Four times 192 * 142 pixels	Q1	Q2
1	0	1	Q2			
1	1	0	Q3		Q3	Q4
1	1	1	Q4			
For more detailed information (timing etc.) see the VV5430 datasheet.						

[4]PVE is set to one by hardware on the sensor board. See the RasCam description under *options*.

Coarse and fine exposure registers.
For external exposure control (AEC = 0) the exposure value can be set via the serial interface (registers 3 and 4). The 18 bit exposure control value is formed from two 9-bit values, coarse and fine. Values written that exceed the mode dependant maximum will be ignored and the maximum will be used.

Register	Function	CCIR		EIA	
		Min	Max	Min	Max
3	Coarse, 9 bits	0	310	0	260
4	Fine, 9 bits	0	404	0	325
Bits 11:9 are not used. The RasCam is used in CCIR mode.					

Lower and upper pixel count thresholds
The lower and upper pixel count thresholds are used by the automatic exposure controller. The power-on default values for TL and TH are exposure mode and video mode dependant. If the external pixel threshold control bit (bit 6 in setup register_2) is set the internal default values for T1 and T2 are overridden by the serial interface values. Note that only the most significant nine bits of each seventeen bit threshold can be controlled.

Register	Function
8	Lower pixel count threshold, 9 bits.
9	Upper pixel count threshold, 9 bits.
Bits 11:9 are not used.	

Gain register
The gain register is used to select an external gain value when automatic gain control is inhibited (AGC = 0) and to set the gain ceiling while automatic gain control is active (AGC = 1).

Gain and gain ceiling, register 5, valid data bits: 4					
Bit				Gain	Comment
G3	G2	G1	G0		
0	0	0	0	1	Default setting
0	0	0	1	2	
0	0	1	1	4	
0	1	1	1	8	Default gain ceiling
1	1	1	1	16	Only when AGC=0
Other settings				Invalid	
Bits 11:4 are not used.					

Analogue control register
The analogue control register is used to control a number of parameters that define internal operations.

analogue control register, register A, valid data bits: 10		
Bit	**Default**	**Function**
0	1	Internal, must be set to 1 for correct operation
1	0	Internal, must be set to 0 for correct operation.
2	0	Internal, must be set to 0 for correct operation.
3	0	Disable anti-blooming protection
4	0	Internal, must be set to 0 for correct operation.
5	0	Internal, must be set to 0 for correct operation.
6	0	Enable external black reference
7	0	Enable external white threshold
8	0	Internal, must be set to 0 for correct operation.
9	0	Enable binairisation of video output. The threshold level above which a pixel is deemed to be white is set via the serial interface, header codes 1001 and 1000 (Upper and Lower Exposure Control Thresholds).

Setup register_3
The setup register_3 is used during sensor synchronization and when the pixel counter in the video timing logic is reset, either at the end of a video line or when the sensor is forced to synchronize externally.

setup register_3, register E, valid data bits: 7			
Bit	**Default**	**Function**	**Comment**
5:0	3	Video timing pixel counter offset	Variable offset that is added to the fixed pixel counter preset value when the counter is reset, at the end of a video line or when an external synchronization is applied
6		Enable SNO	Synchronizing signal to other cameras in multi-camera applications [5]
Bits 11:7 are not used			

[5] Enable SNO adjusts the timing of the FST signal (see the documentation of RasCam, the *options* section) to correctly synchronize external slave cameras. Alternatively, the synchronizing signal for all cameras can be generated externally, which may be more useful in image processing applications.

Read data

Data read from the sensor depends on the setting in Setup register, bits 1 and 0, see table *Setup register_2*.

Read mode A, 32 bits	
Bit	**Function**
3:0	Camera ID code.
4	Undefined.
5	Backlit mode. This bit only reflects the state of the BKLIT pin, not the combined result of the pin and the serial interface BKLIT control bit. This is set 0 on the RasCam.
6	Linear mode. The gamma correction mode is disabled on the RasCam.
7	Auto gain control.
8	Internal black calibration disabled.
9	Auto exposure enabled.
13:10	Gain value
22:14	Fine exposure value
31:23	Coarse exposure value

Read mode B, 32 bits	
Bit	**Function**
16:0	White pixel count.
17	Black level monitor in progress.
31:18	Undefined