

ETR 98-01

L3Cosmics: Interference test.

**A test has been performed to check
that the functionality, added to the MPC,
does not interfere with the running of L3.
The test is done by the designer of the MPC.**

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Interference test

Introduction

For the L3+Cosmics experiment the existing L3 muon chambers are used. The signals from the L3 discriminators are used to generate a trigger and to measure their relative timing. A convenient place was found at the back of the existing muon TDC crates. There the MPCs (Muon Personality Cards)¹ connect the FastBus TDCs to the first and second level muon trigger. The signals on the auxiliary connector are a copy of the discriminator signals that come in at the front panel of the TDC cards, converted to TTL signals. The function of the MPC cards is to collect hit signals from the wires during the drift-time, after the beam crossing. Every two wires are logically ORed, so the 96 input channels can set a pattern in 48 flip-flops. After the drift-time, the PCC (Personality Card Controller) reads the patterns of all MPCs in the crate. The PCC forms muon chamber cells of the patterns and counts the number of hits in a cell. This count is compared with a threshold, set for each cell. When a cell is hit the PCC generates a cell number and a hit count. This information is sent to the first and second level trigger of L3.

To make the muon chamber signals available for the L3+Cosmics experiment, the MPCs

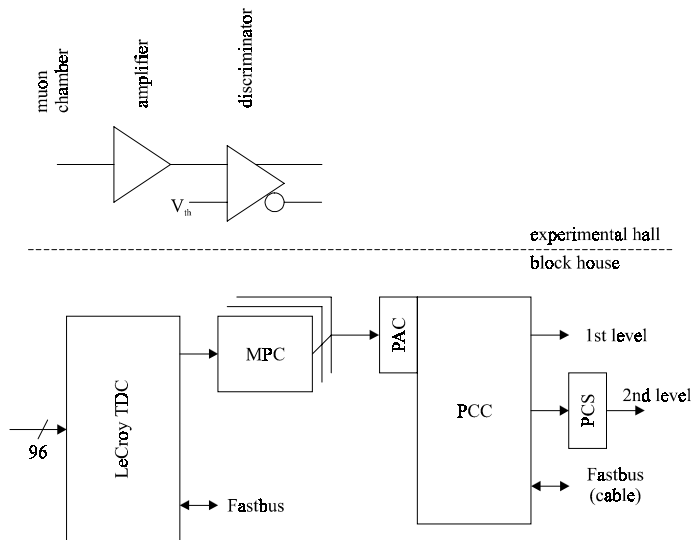


Figure 1: Signal flow from muon chambers in L3

are replaced by CPCs (Cosmic Personality Cards). On these cards the old (MPC) functionality has been redesigned to occupy less space and consume less power. The added functions are the majority logic needed for the L3+Cosmics trigger and a TDC system for time measurements independently from the existing L3 system. The majority logic stretches all input signals for $1.2 \mu\text{s}$ (The drift-time) and determines every 200 ns how many hits there are. If the count is over threshold, the information is passed to the CTT (Central Timing and Trigger), the L3+Cosmics trigger system. The 32 channel TDCs are developed at CERN². They are read out by means of an FPGA (Field Programmable Gate Array) on the CPC. Read out is started when the CTT distributes a

¹ The muon trigger interface for L3: MPC, PAC, PCC-P, PCC-Z, PCS and PCT, september 1989, H. Groenstege NIKHEF-ET.

² A 32 channel general purpose Time to Digital Converter, J. Christiansen CERN/ECP-MIC

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trigger via the FELink (Front End Link) to this FPGA. The CPC then sends a data block to the NIMROD, via the same FELink. In the NIMROD (Nikhef Muon Read Out Driver) the data from front end links of 16 CPCs is used to assemble a partial event. The NIMRODs are read out via VME by the L3+Cosmics data acquisition system. In this way the complete event is assembled.

Interference test

The test set-up

The test has been performed at NIKHEF, by the designer of the MPC. Here we have a test set-up for the MPCs. This FastBus set-up was used to test the MPC cards after production. A special module, the PCT (Personality Card Tester) was build several years ago. The PCT contains a number of sequencers and some fast memory to obtain an even higher speed then is used in practice. Now we use the same set-up for testing whether the CPCs correctly function as MPCs. Various tests are run automatically one after the other by means of a program running in the FastBus master (STR 330).

These tests are:

- Setting and resetting all memories via FastBus. Using the control register, mapped into CSR space of the LeCroy TDC, the 48 flip flop on the MPC can be set and reset. The result of the operation is checked by reading the memories through the data bus, connected to the LeCroy TDC and via the 48 bit data bus that is normally used by the PCC.
- Checking the proper functioning of the statusbits. For example, one of the bits indicates whether the MPC is controlled by FastBus (through the LeCroy TDC) or by the PCC, the interface to the L3 trigger system.
- On the 96 inputs, normally receiving a copy of the discriminator signals, various data patterns are presented. Then a read out sequence, normally initiated by the PCC, is simulated by means of a sequencer in the PCT. The patterns used are:
 - No input. After a reset from the PCC, a strobe is generated. During this strobe (in normal operation, the drift-time) no flip flop may be randomly set.
 - Running ones. Just one input is stimulated at the time. As a result just one flip-flop may be set at the time.
 - Running zeroes. All inputs are stimulated at the same time minus two (remember the logical Oring of two inputs). All memories, minus one, should be set.

All these tests are done several times and at a higher speed then used in normal operation.

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Test 1

In the first test we set-up the CPC with a low threshold for the majority logic. This set-up is done via the JTAG port of the CPC. When the MPC tests are running, this will lead to the generation of majority signals automatically. The majority signal goes to CPC test box, which then generates a trigger. This trigger is send back via the FELink to the CPC. This starts the read out of the TDCs, sitting on the CPC. The trigger and data are send trough a long cable, simulating the actual load. This set-up is very much like the actual situation when the CPC are installed in the L3 muon crates.

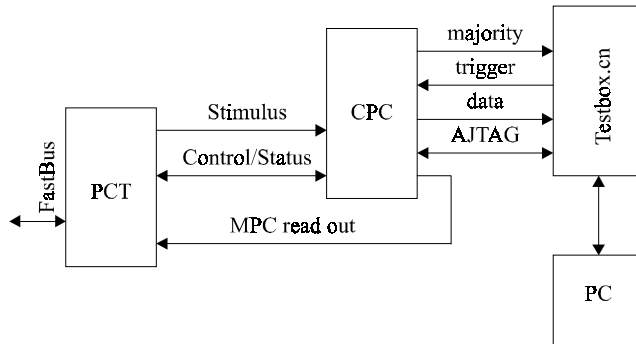


Figure 2: The test set-up

The standard sequence automatically runs the various tests as described on page 3. The sequence has been restarted until a total test time of half an hour. Not one error has been detected.

Interference test

Test 2

Since the functionality of all parts of the CPC is known exactly (being the designer of the MPC and the CPC cards) we can point our concentration to the most critical part.

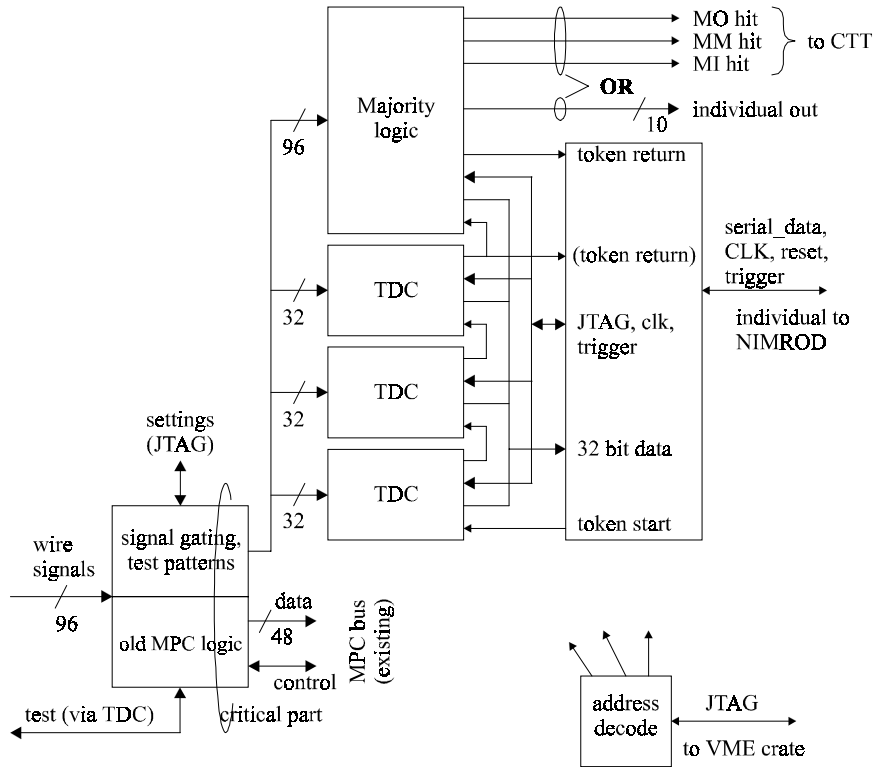


Figure 3: Signal flow on the CPC

We will have a closer look at the critical part on the next page.

Interference test

We will now concentrate on the critical part, pointed out above. This part of the CPC is contained in three MACH devices. Once programmed after production of the cards, the functionality cannot be altered by access via FastBus or JTAG. So, the user cannot change the behavior, just as the PALs, used on the MPC.

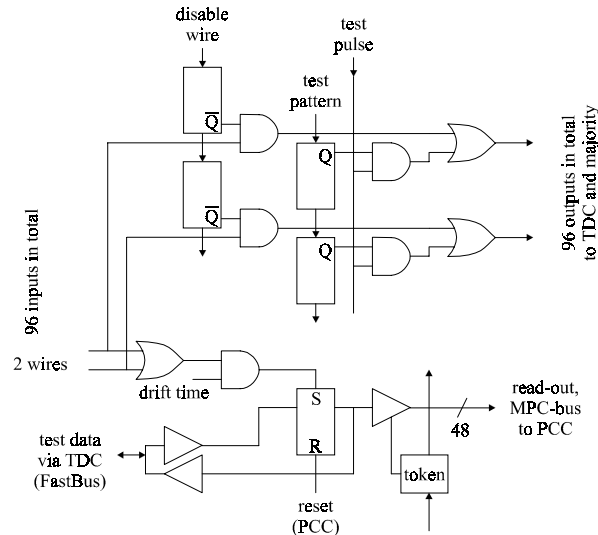


Figure 4: Combined functionality

On the bottom of figure 4 one can see the MPC part of the CPC. The logical ORing of two wires, the gating coming from the PCC, the flip flops and the test bus are programmed in the MACH devices. In the same devices the 96 input signals are buffered. Here we can disable noisy wires and inject test patterns before the signals go to the majority logic and TDCs of the L3+Cosmics system.

Via the FastBus control register, all the MPC memories were set. A number of test patterns were shifted into the devices, using the JTAG port of the CPC. Then an external test pulse enables the devices to send the patterns to the majority logic and TDCs. Again this leads to a majority signal and a trigger is generated, thus a read out cycle is started.

The patterns were:

- Even channels. 48 channels fire at the same time.
- Odd channels. 48 channels fire at the same time.
- All channels. 96 channels fire at the same time.

Each time one million pulses were given. After this the memories were checked. All bits remained intact.

The same tests were done with the memories reset, without errors.

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Conclusion

The first test resembled the actual situation in L3. Because of the speed of the test system, this testing of half an hour would in practice (using the PCC) run for a few days. Analyzing the results would not be easy, since it would require a monitoring program, checking the spy memories in the PCC. Just looking at the trigger results is not enough.

The second test concentrated on the part where L3+Cosmics taps off the input signals. Though for the user less clear, for the designer a more effective test than the first one.

So a complete set of tests have been performed with high statistics without one single error. From these results I draw the conclusion that the CPC and the electronics behind it, do not interfere with L3.