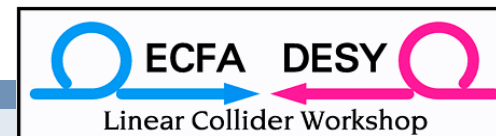


# Data Acquisition

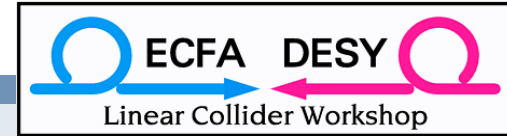


ECFA/DESY LC Workshop  
Amsterdam, Apr. 3<sup>rd</sup> 2003

## Agenda

Vertex detector readout	J. Goldstein
Silicon envelope readout	A. Savoy-Navarro
Minical/Tile-HCAL readout	V. Korbel
CALICE test beam readout	P. Dauncey
Front End card from TRIUMPF	J.P. Martin
LC DAQ guidelines	P. Le Du
Discussion	All

# Activities



- Detector readout R&D

Using existing (modified) electronics (TPC, HCAL, ...)

Developing of new front end readout chips (LCFI, SiLC, Calice, ...)

- Test systems and tools

Existing setup for TPCs in several Labs (based on STAR, ALEPH,...)

Building of a new test system for ECAL/HCAL beam tests (CMS based)

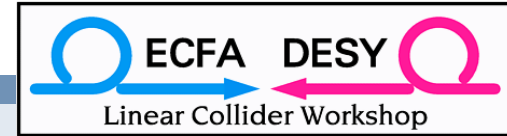
- In general

First common tools for different detectors are being prepared

Discussion on a general data handling model has started

-> need to coordinate and foster increasing number of activities

# Coordinate and Foster DAQ R&D



- To coordinate the DAQ R&D

Define building blocks and their functionalities

Identify common parts

Specify interfaces between these blocks

Identify uncovered readout R&D areas

- Foster R&D efforts

Encourage common test systems for different R&D groups

Develop tools to ease beam tests

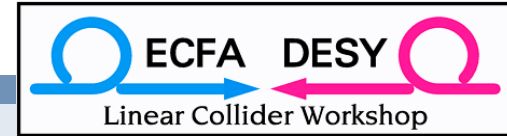
Collect and provide information on existing R&D efforts

- Prepare guidelines

Guideline document : defines functionalities and interfaces

These guidelines cannot be static, regular updates are foreseen

# Data Handling Model



- Data handling logically divided into 4 layers

Front end readout

Central data collection

Event building and processing

Permanent storage

- Between these layers interfaces are defined to

Enable parallel development of components in different R&D groups

Reduce dependencies, allow technology changes at a later stage

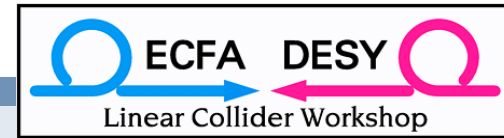
- Control and Monitoring is an essential part

Clock distribution, bunch tagging

Run control, process control, calibration, monitoring

Keep designs **Global Detector Network** aware !

# Functionality of the Layers



- Front end readout

Hardware : Preamplifier, shaper, ADC, memory, ...

Functions : zero-suppression, hit/cluster finding, buffer, multiplexing

- Central data collection

Unique intelligent interface cards (FPGA ?)

Input buffer, data formatting, data reduction (data compression?)

output buffer and standardized interface to event building

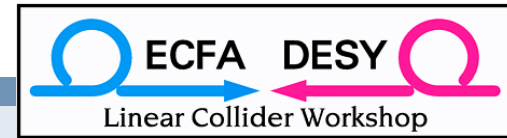
- Event building and processing

Commodity hardware : network switches, processor farm (PC?)

Full event data processing, all bunch crossings of a complete train

Software finders will tag 'bunches of interest' for permanent storage

# Interfaces between Layers



- Front end readout – central data collection

Serial (optical?) link

Intelligent driver and receiver cards for flexibility

Data buffers to desynchronize

- Central data collection – event building

Commercial network, including a standardized protocol

Several data streams in parallel ('partitioning')

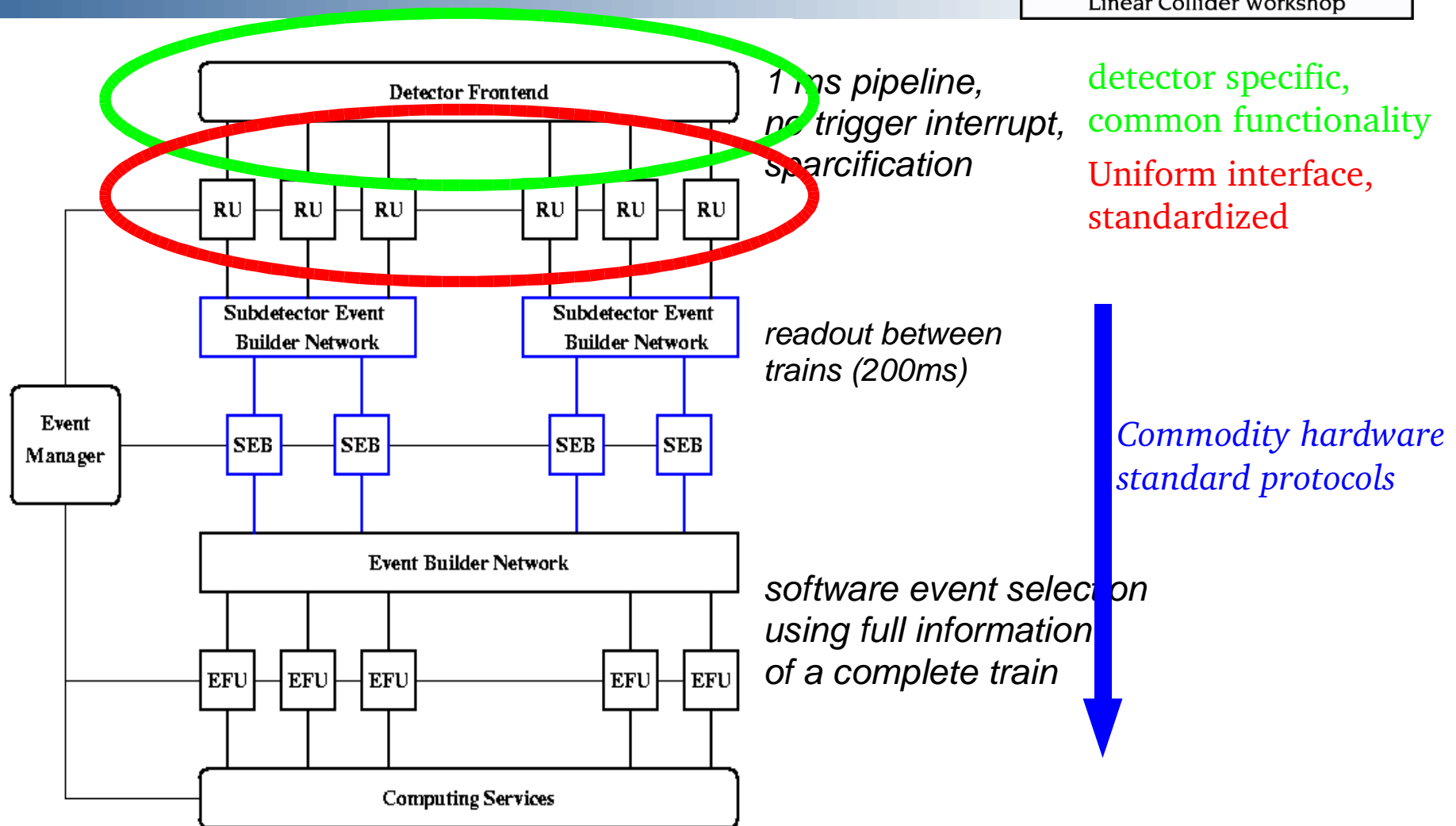
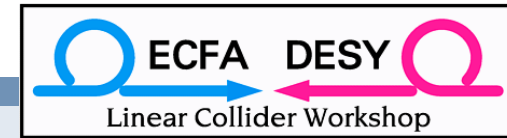
Today : 10GbitEthernet and TCP/IP (alternative : Merynet a la CMS)

- Event building - permanent storage

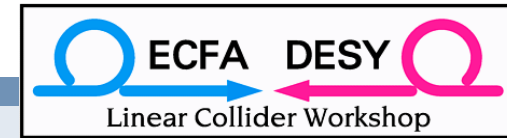
Same type of commercial network and protocol as above

physically same hardware or dedicated hardware ?

# Data Acquisition Overview



# Outlook



- Guidelines

First version of the guideline document in preparation

Detailed documents on specific parts will follow

Data handling working group needed to coordinate and foster R&D

- Working group for data handling

Keep guideline documents up to date

Develop and define standards and tools

Need input from ALL detector R&D working groups : please join !

Mailing list : [ECFA-DESY-DAQ@desy.de](mailto:ECFA-DESY-DAQ@desy.de)

To subscribe send a mail to [guenter.eckerlin@desy.de](mailto:guenter.eckerlin@desy.de)

2-3 meetings per year, next ~ Autumn '03 (next ECFA Workshop)