

LC ENVIRONNEMENTS - RF PICKUP

CHD

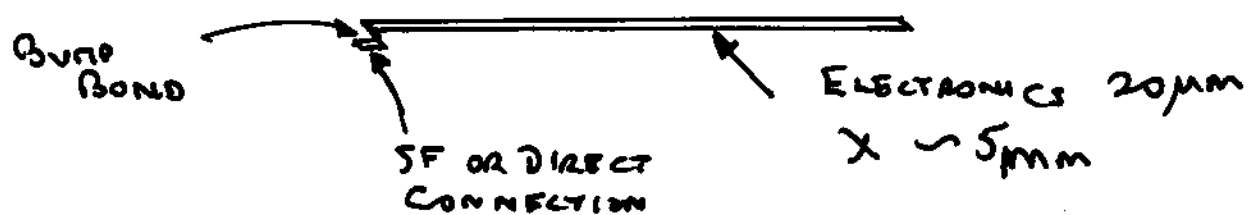
30/3/03

- BEAM-RELATED RF RADIATION THROUGH BEAM-PIPE
(EVEN 0.25 mm Be?) PRESUMABLY NEGLIGIBLE
(UNLESS IT'S CF AS IN UA1!)
- HOWEVER, FLANGES, BPM CABLES, ETC CAN
PRODUCE FEROCIOUS RADIATION
- SLD EXPERIENCE:
 - ANALOGUE SIGNALS STORED SECURELY IN CCD
BURIED CHANNEL
 - DIGITAL LOGIC (PLL IN OPTICAL LINKS) WERE
DISRUPTED - FORTUNATELY COULD BE RESTORED
WITHIN SOME μ S OF END OF BUNCH (TRAIN)
- NLC/SLC $190 @ 1.4 ns \Rightarrow 266 ns$
CLIC $154 @ 0.6 ns \Rightarrow 92 ns$ } INSTANTANEOUS
- REP RATE $120 Hz$ ($\sim 50-200 Hz$ FOR CLIC)
 $\Rightarrow$ SETTLING TIME PLUS READOUT TIME
OK FOR ALL SILICON PIXEL TECHNOLOGY
OPTIONS
- TESLA 500 GeV $2820 @ 337 ns \Rightarrow 950 \mu s$
 - READ LAYER 1 REPEATEDLY @ 50 ns DURING
TRAIN, TO SPARSIFIED INTERNAL DATA STORE

- READ DATA FROM ~ 20 FRAMES TO EXTERNAL DATA STORE DURING 200ms BETWEEN FRAMES

NB: EACH FRAME READOUT (INTERNAL) SPANS ~ 150 BUNCH CROSSINGS, SO THE ELECTRONICS IS HIT REPEATEDLY DURING READOUT BY WHATEVER RF RADIATION IS PRESENT

- FOR SLD VTX, THIS WOULD HAVE BEEN FATAL (LIKE THE BEAM PIPE OF UAI)
- MAYBE OK FOR CPCCO. CIRCUITRY IS A BIT MORE COMPACT



- BUT, AS PART OF VERIFICATION OF ANY PROTOTYPE LADDER, IN ANY TECHNOLOGY, SUGGEST TESTING IN A FINAL FOCUS LAB WHERE MACHINE BUNCHES ARE SIMULATED BY CURRENT PULSES DOWN WIRES IN THE BEAM-PIPE, & ALL OTHER FF EQUIPMENT IS INSTALLED & OPERATING.
- SUCH A FF LAB SHOULD BE BUILT WITHIN THE GAN/GDN FACILITIES

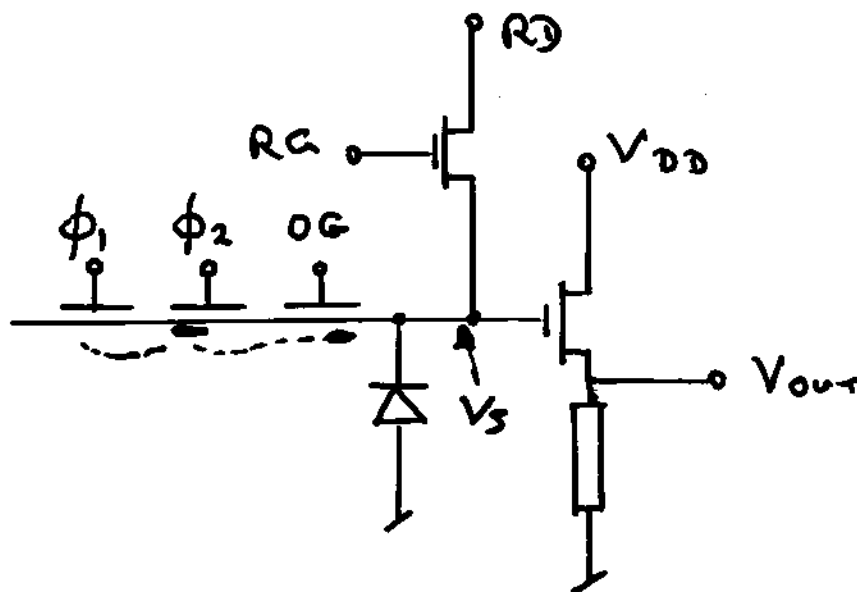
CORRELATED DOUBLE SAMPLING:

WHAT DOES IT MEAN FOR YOU?

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30/3/03

- CDS IS TERM INVENTED ORIGINALLY FOR THE FORM OF PEDESTAL SUBTRACTION ASSOCIATED WITH THE RESET NOISE IN CCD READOUT CIRCUITS



WITH $C_{DET} \sim 103$ OF fF , $Q_{NOISE} \sim 1005$ OF e^-
FROM FLUCTUATIONS IN POST-RESET NODE VOLTAGE V_s

- SIMPLEST CDS INVOLVES

RESET / MEASURE V_s / TRANSFER SIGNAL CHGE / RE-MEASURE V_s

$\Rightarrow \sim 1e^-$ READOUT NOISE

- CAN GAIN MORE. FOR GIVEN SHAPING TIME T_s , OBTAIN SOME FET-CHANNEL RELATED NOISE. EVENTUALLY, LONGER T_s DOESN'T HELP ($1/f$ NOISE).

- CAN DESIGN CCD OUTPUT TO PERMIT MULTI-SAMPLING WHERE Q_{sig} IS REPEATEDLY TRANSFERRED ON & OFF THE FET GATE

$$\text{RESIDUAL NOISE} \propto \frac{1}{\sqrt{N_{SAMPLE}}}$$

- DEPFET HAS ROBUST CDS CAPABILITY, IN LC APPLICATION.

- $\sim 50\mu s$ SIGNAL INTEGRATION

- READ PEDESTAL + SIGNAL

- RESET

- READ PEDESTAL ALONE

Δ OVER
 $\sim 20ns$

- CCD IS SIMILARLY ROBUST

- READ PEDESTAL + SIGNAL CHGE FROM EARLIER IN THE ROW

- TRANSFER SIGNAL FROM NEXT PIXEL

- READ ACCUMULATED CHGE

Δ
OVER
- 20ns

- CDS FOR MAPS INVOLVE SUBTRACTION OVER FRAME PERIOD OF 50ms OR WHATEVER.
- COULD IN PRINCIPLE BE SOLVED BY INCLUDING

(3)

1- PIXEL CCD, OF DEPFET STRUCTURE,
WITHIN THE CMOS PIXEL

- CDS WITH $\Delta T = 50 \mu s$?

SLD WAS OK IN INTER-TRAIN PERIOD
WITH $200 ns$. NO EXPERIENCE BEYOND
THIS

- MIGHT GET AWAY WITH IT AT NLC,
AFTER SOME SETTLING TIME
- MIGHT NOT WORK AT TESLA

⇒ ONE GOOD REASON FOR BUILDING THE
FF LAB SOMEWHERE